AMD Bolton FCH
Register Reference Guide

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Trademarks

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Revision History

Date	Revision	Description
May 2015	3.03	Corrected the ASF Table in Chapter 3.
May 2015	3.01	Added commands that are supported for the ASF remote control.
August 2014	3.00	Initial public release.

Chapter 1
Introduction

1.1 About This Guide

This manual serves as a register reference guide for the AMD Bolton series of fusion controller hubs (FCHs).

1.2 Nomenclature and Conventions

1.2.1 Register Description Format

All registers in this document are described with the format of the sample table below. All offsets are in hexadecimal notation, while programmed bits are in either binary or hexadecimal notation.

Latency Timer – RW – 8 bits – [Offset: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Latency Timer (R/W)	7:0	00h	This bit field is used to specify the time in number of PCI clocks, the SATA controller as a master is still allowed to control the PCI bus after its GRANT_L is deasserted. The lower three bits [0A:08] are hardwired to 0 h , resulting in a time granularity of 8 clocks.
Latency Timer. Reset Value: 00h			

Register Information	Value/Content in the Example
Register name	Latency Timer
Read / Write capability R = Readable W = Writable RW = Readable and Writable RO = Read Only	RW
Register size	8 bits
Register address(es)*	Offset: 0Dh
Field name	Latency Timer (R/W)
Field position/size	7:0
Field default value **	00h
Field description	"This bit … 8 clocks."
Field mirror information	
Brief register description	Latency Timer. Reset Value: 00h
Notes: *There may be more than one address; the convention used is as follows: **[aperName:offset]** - single mapping, to one aperture/decode and one offset **[aperName1, aperName2, …, aperNameN:offset]** - multiple mappings to different apertures/decodes but same offset **[aperName:startOffset-endOffset]** - mapped to an offset range in the same aperture/decode ** If the default value is specified, it is the hardware default value that is programmed after power up reset. The BIOS may override this value with the proper value for normal operation based on different criteria, e.g., suggested value in the Register Programming Requirements document. If the value is "xx", it denotes that the hardware will not initialize the default value after power on reset. The value will depend on either the BIOS initialization sequence or real-time value from hardware.	

Warning: Do not attempt to modify the values of registers or bit fields that are marked as "Reserved." Doing so may cause the system to behave in unexpected ways.

1.2.2 Numeric Representations

- Hexadecimal numbers are appended with “h” whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.

1.2.3 Changes Indication

Changes and additions from the previous release of this document are highlighted in red. Refer to *Revision History* at the beginning of this manual for change details.

Chapter 2
PCI Devices

Use the links below to jump to a section of interest.

2.1 SATA Registers

There is a single SATA controller in Bolton. It's Bus-0, dev17, function 0.

2.1.1 PCI Configuration Registers for SATA

These registers are accessible only when the SATA controller detects a configuration Read or Write operation, with its IDSEL asserted, on the 32-bit PCI bus.

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID/Class Code	08h
Cache Link Size	0Ch
Master Latency Timer	0Dh
Header Type	0Eh
BIST Mode Type	0Fh
Base Address 0	10h
Base Address 1	14h
Base Address 2	18h
Base Address 3	1Ch
Bus Master Interface Base Address	20h
AHCI Base Address	24h
Subsystem ID and Subsystem Vendor ID	2Ch
Capabilities Pointer	34h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min_gnt	3Eh
Max_latency	3Fh
Misc control	40h
Watch Dog Control And Status	44h
Watch Dog Counter	46h
Misc control 2	48h
	4Ch
MSI Control	50h
MSI Address	54h
MSI Upper Address	58h
MSI Data	5Ch
Power Management Capability ID	60h
Power Management Capability	62h
Power Management Control And Status	64h
Serial ATA Capability Register 0	70h
Serial ATA Capability Register 1	74h
IDP Index	78h
IDP Data	7Ch
PHY Core Control Settings (I)	80h
	84h
	88h
	8Ch
	8Eh
	90h
	94h
	96h
PHY PortX GenX Fine Tune	98h
	9Ch
	A0h
	A4h
	A8h
	A9h
Reserved	AAh

Register Name	Offset Address
Reserved	ACh
	B0h
PortX BIST Control/Status	B4h
Reserved	B6h
PortX BIST Port Select	B7h
	B8h
T-Mode BIST Transit Pattern DW1	BCh
T-Mode BIST Transit Pattern DW2	C0h
T-Mode BIST Transit Bit	C4h
	C8h
	CCh
Advanced Features Capabilitiy Register0	D0h
Advanced Features Capabilitiy Register1	D4h
	D6h
Reserved	D8h
Reserved	DCh
Reserved	DEh
PCI Target Control TimeOut Counter	E0h
	E2h
Reserved	E4h
Reserved	E8h
Reserved	ECh
Reserved	F0h
	F4h
	F5h
Reserved	F6h
	F7h
Reserved	F8h
Reserved	FCh

Vendor ID – R – 16 bits – [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Vendor Identifier. The vendor ID is 1022h for AMD.

Device ID – R – 16 bits – [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	7800h	This register holds a unique 16-bit value assigned to a device. 7800h for IDE controller, 7801h for AHCI controller, 7802h for RAID controller, 7803h for RAID 5 controller, 7804h for AMD AHCI driver. 7805h for DOT Hill Raid driver E-fuse will default/limit to non-RAID 5 controller. Note: When E-fuse ROM bit 133 is enabled, the default value of Device ID is 7803h. Reg0x40[0] (I/O Access Enable) should be set to 1, then the value of DEVICE ID can be changed. After that, if reg0x40[0] is cleared, the new value will stay and won't change to the default value of 7803h. When E-fuse ROM bit 133 is disabled, Device ID can be programmed only to 7800/7801/7802/7804/7805.h. Attempts to program Device ID with 7803h when E-fuse ROM bit 133 is disabled will result in Device ID becoming 7802h.

Command – RW – 16 bits – [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Access Enable	0	0b	This bit controls access to the I/O space registers. When this bit is 1, it enables the SATA controller to respond to PCI I/O space access.
Memory Access Enable	1	0b	This bit controls access to the memory space registers. When this bit is 1, it enables the SATA controller to respond to PCI memory space access.
Bus Master Enable	2	0b	Enable or disable the device behaving as a Bus Master. 1: Enable 0: Disable.
Special Cycle Recognition Enable	3	0b	Read Only. Hard-wired to 0 indicating no special support.
Memory Write and Invalidate Enable	4	0b	Read Only. Hard-wired to 0 indicating that Memory Write and Invalidate Enable is not supported.
VGA Palette Snoop Enable	5	0b	Read Only. Hard-wired to 0 indicating the SATA host controller does not need to snoop VGA palette cycles.
PERR# Detection Enable	6	0b	If set to 1, the IDE host controller asserts PERR# when it is the agent receiving data AND when it detects a parity error. PERR# is not asserted if this bit is 0.
Wait Cycle Enable	7	0b	Read Only. Hard-wired to 0 indicating the SATA controller does not need to insert a wait state between the address and the data on the AD lines.
SERR# Enable	8	0b	If set to 1 and bit[6] is set, the SATA controller asserts SERR# when it detects an address parity error. SERR# is not asserted if this bit is 0.
Fast Back-to-Back Enable	9	0b	Read Only. Hard-wired to 0 indicating that only Fast Back-to-Back to the same agent is allowed.
Interrupt Disable	10	0b	This bit disables the device/function from asserting INTx#. 0: Enable the assertion of the device/function's INTx# signal. 1: Disable the assertion of the device/function's INTx# signal.
Reserved	15:11	00h	Reserved.

Status – RW – 16 bits – [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0h	Reserved.
Interrupt Status	3	0b	This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is 0 and this Interrupt Status bit is 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to 1 has no effect on the state of this bit.
Capabilities List	4	1b	Read Only. Default to 1 to indicate that the Capabilities Pointer is located at 34h.
66MHz Support	5	1b	66MHz capable. This feature is supported in the SATA controller.
Reserved	6	0b	Reserved.
Fast Back-to-Back Capable	7	0b	Read Only. Hard-wired to 0 indicating that Fast Back-to-Back is incapable.

Status – RW – 16 bits – [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Data Parity Error	8	0b	Data Parity Reported. Set to 1 if SATA controller detects PERR# asserted while acting as PCI master (regardless whether PERR# was driven by SATA controller or not.) Writing a 1 clears this bit.
DEVSEL# Timing	10:9	01b	Read Only. These bits indicate DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
Signaled Target Abort	11	0b	This bit is set to 1 when the SATA controller signals Target Abort. Writing a 1 clears this bit.
Received Target Abort	12	0b	This bit is set to 1 when the SATA controller generated PCI cycle (SATA controller is the PCI master) is aborted by a PCI target. Writing a 1 clears this bit.
Received Master Abort Status	13	0b	Received Master Abort Status. Set to 1 when the SATA controller, acting as a PCI master, aborts a PCI bus memory cycle. Writing a 1 clears this bit.
SERR# Status	14	0b	SERR# status. This bit is set to 1 when the SATA controller detects a PCI address parity error. Writing a 1 clears this bit.
Detected Parity Error	15	0b	Detected Parity Error. This bit is set to 1 when the SATA controller detects a parity error. Writing a 1 clears this bit.

Revision ID/Class Code - RW – 32 bits – [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	00h	These bits default to 00h to indicate the revision level of the chip design.
Operating Mode Selection	15:8	8Fh	RW Programmable I/F. Bit[15] – Master IDE Device. Always 1. Bit[14:12] – Reserved. Always read as 0's. Bit[11] – Programmable indicator for Secondary. Always 1 to indicate that both modes are supported. Bit[10] – Operating Mode for Secondary. 0: Compatibility Mode 1: Native PCI-mode Bit[9] – Programmable indicator for Primary. Always 1 to indicate that both modes are supported. Bit[8] – Operating Mode for Primary. 0: Compatibility Mode 1: Native PCI-mode See Note 1*
Sub-Class Code	23:16	01h	Sub-Class Code. 01h to indicate an IDE Controller. See Note 2**
Class Code	31:24	01h	Class Code. These 8 bits are read only and wired to 01h to indicate a Mass-Storage Controller.

*Note 1: When Sub-Class Code is 01h, indicating an IDE controller, bits[11:8] are writable, despite of 40h[0]'s setting. All eight bits are writable when reg0x40[0] (CC_reg_wr_en) is set.

**Note 2: This field is only writable when reg0x40[0] (CC_reg_wr_en) is set.

Sub-Class Code	Program Interface:	Controller Type
01	8F	IDE
06	01	AHCI
04	00	RAID

Cache Line Size – RW – 8 bits – [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Reserved
Cache Line Size	7:4	0h	If the value is 1, cache line size is 16 DW (64 byte).

Master Latency Timer – RW – 8 bits – [PCI_Reg:0Dh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0h	Reserved
Master Latency Timer	7:3	00h	This field specifies, in units of PCI bus clocks, the guaranteed time slice allowed to IDE host controller for burst transactions.

Header Type – R – 8 bits – [PCI_Reg:0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	6:0	00h	Since the IDE host controller is a single-function device, this field contains a value of 00h.
Multi-function device	7	0b	This bit defaults to 0b to indicate single-function device.

BIST Mode Type – RW – 8 bits – [PCI_Reg:0Fh]			
Field Name	**Bits**	**Default**	**Description**
Completion Code	3:0	0h	Read Only. Indicates the completion code status of BIST. A non-zero value indicates a failure.
Reserved	5:4	0h	Reserved
Start BIST	6	0	Since bit[7] is 0, programming this bit has no effect.
BIST Capable	7	0	Read Only. Hard-wired to 0 indicating no HBA related BIST function.

Base Address 0 – RW – 32 bits – [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	2:1	0h	Reserved.
Primary IDE CS0 Base Address	31:3	0000_0000h	In IDE mode: Base address for Primary IDE Bus CS0. This register is used for native mode only. Base Address 0 is not used in compatibility mode.

Base Address 1 – RW – 32 bits – [PCI_Reg:14h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	1	0b	Reserved.
Primary IDE CS1 Base Address	31:2	0000_0000h	In IDE mode: Base address for Primary IDE Bus CS1. This register is used for native mode only. Base Address 1 is not used in compatibility mode.

Base Address 2 – RW – 32 bits – [PCI_Reg:18h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	2:1	0h	Reserved.
Secondary IDE CS0 Base Address	31:3	0000_0000h	In IDE mode: Base address for Secondary IDE Bus CS0. This register is used for native mode only. Base Address 2 is not used in compatibility mode.

Base Address 3 – RW – 32 bits – [PCI_Reg:1Ch]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to I/O space.
Reserved	1	0b	Reserved.
Secondary IDE CS1 Base Address	31:2	0000_0000h	Base address for Secondary IDE Bus CS1. This register is used for native mode only. Base Address 3 is not used in compatibility mode.

Bus Master Interface Base Address – RW – 32 bits – [PCI_Reg:20h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to I/O space.
Reserved	3:1	0h	Reserved.
Bus Master Interface Register Base Address	31:4	0000_0000h	Base address for Bus Master interface registers and correspond to AD[31:4].

AHCI Base Address – RW – 32 bits – [PCI_Reg:24h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	0b	A constant value of 0 indicates that the operational registers of the device are mapped into memory space of the main memory of the PC host system.
Reserved	10:1	000h	Reserved.
AHCI Base Address	31:11	000000h	Base address of register memory space. This represents a memory space for support of 8 ports.

Subsystem ID and Subsystem Vendor ID – RW – 32 bits – [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	Subsystem Vendor ID. Can only be written once by software.
Subsystem ID	31:16	0000h	Subsystem ID. Can only be written once by software.

Write once and read only.

Capabilities Pointer – R – 8 bits – [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	60h	The first pointer of Capability block.

Interrupt Line – RW – 8 bits – [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	Identifies which input on the interrupt controller the function's PCI interrupt request pin (as specified in its Interrupt Pin register) is routed to.

Interrupt Pin – R – 8 bits – [PCI_Reg:3Dh]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin	7:0	01h	Hard-wired to 01h.

Min_gnt – R – 8 bits – [PCI_Reg:3Eh]			
Field Name	**Bits**	**Default**	**Description**
Minimum Grant	7:0	00h	This register specifies the desired settings for how long of a burst the SATA controller needs. The value specifies a period of time in units of ¼ microseconds. Hard-wired to 0's and always read as 0's.

Max_latency – R – 8 bits – [PCI_Reg:3Fh]			
Field Name	**Bits**	**Default**	**Description**
Maximum Latency	7:0	00h	This register specifies the Maximum Latency time required before the SATA controller as a bus-master can start an access. Hard-wired to 0's and always read as 0's.

Misc Control – RW – 32 bits – [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
Subclass Code Write Enable	0	0b	Once set, Program Interface register (PCI_Reg:09h), Subclass code register (PCI_Reg:0Ah), Multiple Message Capable bits (PCI_Reg50h[19:17]) can be programmable.
Disable port0	16	0b	When set, PHY port0 is disabled, port0 clock at link/transport layer is shut down.
Disable port1	17	0b	When set, PHY port1 is disabled, port1 clock at link/transport layer is shut down.
Disable port2	18	0b	When set, PHY port2 is disabled, port2 clock at link/transport layer is shut down.
Disable port3	19	0b	When set, PHY port3 is disabled, port3 clock at link/transport layer is shut down.
Disable port4	20	0b	When set, PHY port4 is disabled, port4 clock at link/transport layer is shut down.
Disable port5	21	0b	When set, PHY port5 is disabled, port5 clock at link/transport layer is shut down.

Watch Dog Control And Status – RW – 16 bits – [PCI_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
Watchdog Enable	0	0b	Set the bit to enable the watchdog counter for all the PCI down stream transactions for SATA ports.
Watchdog Timeout Status	1	0b	Watchdog Counter Timeout Status bit. This bit indicates that the watchdog counter has expired for PCI down stream transaction, and as a result, the transaction was aborted. Software write of 1 clears the status.
Reserved	15:2	0h	Reserved.

Watch Dog Counter – RW – 16 bits – [PCI_Reg:46h]			
Field Name	**Bits**	**Default**	**Description**
Watchdog Counter	7:0	80h	Specifies the timeout retry count for PCI down stream retries. This value is used for SATA ports.
Reserved	15:8	00h	Reserved. Read/write-able.

Misc Control 2– RW – 32 bits – [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
Enable Fix For HBA Loses DPS Interrupt Lost or Sends Extra One (A12)	11	0b	When set, the fix will be enabled and HBA will not lose any DPS interrupt, nor will it send extra ones. When cleared the fix is disabled. When set, it will enable the fix of SB2583. This bit is only valid for A12
SW Disable Primary Channel	28	0b	When set, IDE Primary Channel is disabled in register level. This setting only valid when Subclass code is IDE.
SW Disable Secondary Channel	29	0b	When set, IDE Secondary Channel is disabled in register level. This setting only valid when Subclass code is IDE.
IDE DMA READ Enhancement	31	0b	When set, an enhancement is applied to IDE DMA read commands. (SB02440)

MSI Control – RW- 32 bits – [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	05h	Read Only. Capability ID, indicates this is MSI capability ID.
Capability Next Pointer	15:8	70h	Read-Only. Defaults to 70h, points to Index Data pair capability.
Message Signaled Interrupt Enable	16	0b	MSI Enable.
Multiple Message Capable	19:17	010b	Multiple Message Capable (MMC).
Multiple Message Enable	22:20	0h	Multiple Message Enable (MME).
MSI 64-bit Address	23	1b	Read Only 64-bit address supported.
Reserved	31:24	00h	Reserved.

MSI Address – RW- 32 bits – [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0h	Reserved.
MSI Address	31:2	0000_0000h	Lower 32 bits of the system specified message address. Always DW aligned.

MSI Upper Address – RW- 32 bits – [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
MSI Upper Address	31:0	0000_0000h	Upper 32 bits of the system specified message address.

MSI Data – RW- 16 bits – [PCI_Reg:5Ch]			
Field Name	**Bits**	**Default**	**Description**
MSI Data	15:0	0000h	MSI Data

Power Management Capability ID – R – 16 bits – [PCI_Reg:60h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	01h	Default = 01h. Indicates that this pointer is a PCI power management.
Capability Next Pointer	15:8	50h	Hardwired to 50h, points to MSI Capability.

Power Management Capability – R- 16 bits – [PCI_Reg:62h]			
Field Name	**Bits**	**Default**	**Description**
Version	2:0	010b	Indicates support for Revision 1.1 of the *PCI Power Management Specification.*
PME Clock	3	0b	Indicates that PCI clock is not required to generate PME#.
Reserved	4	0b	Reserved
Device Specific Initialization	5	1b	Indicates whether device-specific initialization is required. Hard wired to 1.
Aux_Current	8:6	0h	Reports the maximum Suspend well current required when in the $D3_{COLD}$ state. Hardwire to 000b.
D1_Support	9	0b	D1 state is not supported.
D2_Support	10	0b	D2 state is not supported.
PME_Support	15:11	00h	Hardwired to 00h.

PCI Power Management Control And Status – RW- 16 bits – [PCI_Reg:64h]			
Field Name	**Bits**	**Default**	**Description**
Power State	1:0	00b	This field is used both to determine the current power state of the HBA and to set a new power state. The values are: 00 – D0 state 11 – $D3_{HOT}$ state The D1 and D2 states are not supported. When in the $D3_{HOT}$ state, the configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked.
Reserved	7:2	00h	Reserved
PME Enable	8	0b	Read Only. Hardwired to 0 to indicate PME is disabled
Reserved	14:9		Reserved.
PME Status	15	0b	Read Only. Hardwired to 0 as PME is disabled

Serial ATA Capability Register 0 – R- 32 bits – [PCI_Reg:70h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	12h	Hardwired to 12h to indicate that this pointer is a Serial ATA Capability.
Capability Next Pointer	15:8	D0h	Hardwired to D0h, points to Advance Control capability.
Minor Revision	19:16	0h	Minor revision number of the SATA Capability Pointer implemented.
Major Revision	23:20	1h	Major revision number of the SATA Capability Pointer implemented.
Reserved	31:24	0h	Reserved

This set of registers, when supported, is used for the Index-Data Pair mechanism.

Serial ATA Capability Register 1 – R- 32 bits – [PCI_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**
BAR Location	3:0	1111b	Value 1111b indicates Index-Data pair is implemented in Dwords directly following SATACR1 in the PCI configuration space.
BAR Offset	23:4	000h	Indicates the offset into the BAR where the Index-Data Pair are located in Dword granularity.
Reserved	31:24	0h	Reserved.

This set of registers, when supported, is used for the Index-Data Pair mechanism.

IDP Index Register – RW- 32 bits – [PCI_Reg:78h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved.
IDP Index	10:2	000h	This register selects the Dword offset of the memory mapped AHCI register to be accessed. The IDP Index should be sized such that it can access the entire ABAR register space for the particular implementation.
Reserved	31:11	000000h	Reserved.

This set of registers, when supported, is used for the Index-Data Pair mechanism.

IDP Data Register – RW- 32 bits – [PCI_Reg:7Ch]			
Field Name	**Bits**	**Default**	**Description**
IDP Data	31:0	F722_FF85h	This register is a “window” through which data is read or written to the memory mapped register pointed to by the IDP Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by IDP Index.

All register accesses to IDP Data are Dword granularity.

PHY Core Control (I) – RW – 32 bits – [PCI_Reg:80h]			
Field Name	**Bits**	**Default**	**Description**
PHY Fine Tune Target Port	2:0	000b	**PHY.CCNTL.PN** - Write to this field to indicate which port's fine tune settings software will read/write from/to. 0h: Port 0 is selected 1h: Port 1 is selected 2h: Port 2 is selected 3h: Port 3 is selected 4h: Port 4 is selected 5h: Port 5 is selected * Note 1
Reserved	3	0b	Reserved. This field is read/write-able.
Generation I/II/III	5:4	01b	**PHY.CCNTL.GEN** - Write to this field to indicate which Generation Speed software would like the setting to be applied to. 0h: Reserved 1h: Setting is for Gen 1 2h: Setting is for Gen 2 3h: Setting is for Gen 3 *Note 1
Reserved	7:6	00b	Reserved.
Write Settings To All Ports	8	0b	**PHY.CCNTL.WRALL** - Level signal that allows simultaneously writing port-dependent PHY fine-tune settings to all ports (values in offset 0x98-0xA3). Software does not need to write individual port settings. This signal has NO effect on read and shall be used for write only. 1: Port0-Port5 fine-tune settings will be written at the same time with the same values placed into PHY.PXGX and PHY.PX fields of reg0x98. 0: Port0-Port5 PHY.PXGX and PHY.PX fields will not be changed at the same time and need to be individually entered using PHY.CCNTL.PN. *Note2
Reserved	31:9	0000_00h	Reserved.

*Note 1
Software uses these fields to read/write PHY.PXGX register to PCI_REG offset 0x98[31:0] . For example, if PHY.PXGX.TX.DRV_STR[2:0] is to be modified for port2/Gen3, then software will exercise the following sequence:
1. Write 0x2 to PHY.CCNTL.PN,
2. Write 0x3 to PHY.CCNTL.GEN
3. Write desired value to PHY.PXGX.TX.DRV_STR[2:0]

*Note 2
Software uses these fields to write PHY.PXGX and PHY.GX registers at PCI_REG offset 0x98[31:0] , and apply it across all ports.
For example, if PHY.PXGX.TX.DRV_STR[2:0] is to be modified for all ports for Gen3, then software will exercise the following sequence:
1. Write 0x3 to PHY.CCNTL.GEN
2. Write 0x1 to PHY.CCNTL.WRALL
3. Write desired value to PHY.PXGX.TX.DRV_STR[2:0]

Phy Fine Tune PortX GenX Setting - RW- 32 bits - [PCI_Reg:98h]			
Field Name	**Bits**	**Default**	**Description**
Transmitter De-emphasis	7:0	3h	Tx De-emphasis setting. Unit: dB 00h: 0 02h: 1.58 03h: 2.50 06h: 3.52 07h: 4.68 0Eh: 6.02 0Fh: 7.60 1Eh: 9.54 1Fh: 12.04 Other values: Invalid
Transmitter Driving Strength	10:8	0h	Tx drive strength control. Unit: mVppd 0h: 502 1h: 585 2h: 672 3h: 755 4h: 838 5h: 926 6h: 1011 7h: 1096

Note: The default values are generation speed dependent.
Note: The entire 0x98h register is generation speed sensitive as well as per-port sensitive, that is, all fields are accessed through PHY.CCNTL.GEN and PHY.CCNTL.PN. This implies that there will be a total of 24 sets of registers implemented for this offset internally; however, from the software point-of-view, there will be only 1 set. For example, if software wants to set PHY.PXGX.DEEMPH_STR[7:0] for Gen3, it will first set PHY.CCNTL.GEN to 2'b11, then proceed to writing the 8-bit value into PHY.PXGX.DEEMPH_STR[7:0]. Similarly, if software wants to read the Gen2 value, it will then set PHY.CCNTL.GEN to 2'b10 before reading.

PortX BIST Control/Status - RW - 16 bits - [PCI_Reg:B4h]			
Field Name	**Bits**	**Default**	**Description**
PortX Link BIST Enable	0	0b	The port that the value is witten to and read back from is determined by Portx BIST Port Sel Register (0xB7). When reading, the port is determined by the last significant bit with the value 0x1 in Portx BIST Port Sel Register (0xB7); when writing, the port is determined by the any bit with the value 0x1 in Portx BIST Port Sel Register (0xB7). Once set, PortX is put into Link BIST mode, overriding normal operation.
PortX Link BIST Pattern	5:2	0000b	0000: Pseudo-random with ALIGN insertion (when Error Count is used, must choose this pattern). 0001: D10.2 Highest frequency (for Rx eye diagram measurement). 0010: SYNC primitive (for Rx eye diagram measurement). 0011: 0100: Mid Frequency Test Pattern (MFTP) 0101: 0110: 0111: Forced T-mode Enable. Forced T-mode is defined as "Far end transmit only mode without Device initiating". In T-mode, the BIST pattern that is generated is based on the programming in the BIST Transmit Pattern Registers DW1 (reg0xBC) and DW2 (reg0xC0).
PortX BIST with disconnect Enable	11	0b	When set and a BIST Activate FIS is received from the device, the HBA will ignore all OOB signaling from the device. The HBA can exit this mode either through a hardware reset or a software initiated COMRESET. Note: This bit will not be cleared by a software initiated COMRESET.
PortX Link BIST Speed	13:12	00b	PHY PortX speed control for Link BIST mode. 2'b11 : Gen3 2'b10 : Gen2 2'b01 : Gen1 2'b00 : Gen1

Reset Condition: PCI Reset, or Power Management State transition from D3 to D0.
Note: Reset Condition for bits[15:11] is PCI Reset.

PortX BIST Port Select - RW - 8 bits - [PCI_Reg:B7h]			
Field Name	**Bits**	**Default**	**Description**
PortX BIST Port Select	7:0	00h	This register is bit significant. When the bit is set, it indicates the corresponding port software will read/write from/to during link BIST. You must set this register writing into or reading from PortX BIST Control Register (0xB4), otherwise the value may be read back from or written into an un-expected port.

Reset Condition: PCI Reset, or Power Management State transition from D3 to D0.

T-Mode BIST Transit Pattern DW1 - RW - 32 bits - [PCI_Reg:BCh]			
Field Name	**Bits**	**Default**	**Description**
T-mode BIST Transit Pattern DW1	31:0	0000_0000h	Transit Pattern DW1

Reset Condition: PCI Reset, or Power Management State transition from D3 to D0

T-Mode BIST Transit Pattern DW2 - RW - 32 bits - [PCI_Reg:C0h]			
Field Name	**Bits**	**Default**	**Description**
T-mode BIST Transit Pattern DW2	31:0	0000_0000h	Transit Pattern DW2

Reset Condition: PCI Reset, or Power Management State transition from D3 to D0

T-Mode BIST Transit Control- RW – 32 bits – [PCI_Reg:C4h]			
Field Name	**Bits**	**Default**	**Description**
T-mode A bit	0	0b	ALIGN primitives bypass mode
T-mode S bit	1	0b	Scrambling Bypass.
T-mode P bit	2	0b	The transmit primitives bit.
Reserved	31:3	0000_0000h	Reserved. Read/Write-able.

Reset Condition: PCI Reset, or Power Management State transition from D3 to D0

Advanced Features Capability Register0 – R - 32bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	13h	The value of 13h in this field identifies the function as being AF capable.
NXT_PTR	15:8	00h	Next pointer. End of list.
Length	23:16	06h	AF Structure Length (Bytes). Returns a value of 06h.
TP_CAP	24	1b	Set to 1b to indicate support for the Transactions Pending (TP) bit (reg0xA8[8]. TP must be supported if FLR is supported.
FLR_CAP	25	1b	Set to 1b to indicate support for Function Level Reset (FLR).
Reserved	31:26	00h	

Advanced Features Capability Register1 – R - 16bits - [PCI_Reg:D4h]			
Field Name	**Bits**	**Default**	**Description**
INITIATE_FLR	0	0b	A write of 1b initiates Function Level Reset (FLR). FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there. The value read by software from this bit is always 0b.
Reserved	7:1	00h	
TP	8	0b	Transactions Pending (TP): A value of 1b indicates that the Function has issued one or more non-posted transactions that have not been completed, including non-posted transactions that a target has terminated with Retry. A value of 0b indicates that all non-posted transactions have been completed.
Reserved	15:9	00h	Reserved.

PCI Target Control TimeOut Counter- RW - 16 bits - [PCI_Reg:E0h]			
Field Name	**Bits**	**Default**	**Description**
PCI Target Control TimeOut Count	7:0	80h	This register is used for programming PCI Target Control TimeOut Count used to clear any stale target commands to the hosts controller. Granularity is 15.5us (Count * 15.5 us) The counter will be disabled if the count is programmed to 0x0.
Reserved	15:8	00h	Reserved.

2.1.2 SATA I/O Registers for IDE Mode

2.1.2.1 BAR0/BAR2/BAR1/BAR3 Registers

BAR0/BAR2 uses 8 bytes of I/O space. BAR0 is used for Primary channel and BAR2 is used for Secondary channel during IDE native mode. BAR1/BAR3 uses 2 bytes of I/O space. BAR1 is used for Primary channel and BAR3 is used for Secondary channel during IDE native mode.

Address (hex)			**Name and Function**	
Compatibilty Mode		**Native Mode (Offset)**	**Read Function**	**Write Function**
IDE Command Block Registers				
Primary	**Secondary**	**BAR0/BAR2**		
1F0	170	(Primary or Secondary) Base Address 0 + 0	Data (16 bit)	Data (16 bit)
1F1	171	(Primary or Secondary) Base Address 0 + 1	Error register	Features register
1F2	172	(Primary or Secondary) Base Address 0 + 2	Sector Count	Sector Count
1F3	173	(Primary or Secondary) Base Address + 3	Sector Number	Sector Number
1F4	174	(Primary or Secondary) Base Address + 4	Cylinder Low	Cylinder Low
1F5	175	(Primary or Secondary) Base Address + 5	Cylinder High	Cylinder High
1F6	176	(Primary or Secondary) Base Address + 6	Drive/Head	Drive/Head
1F7	177	(Primary or Secondary) Base Address + 7	Status	Command
IDE Control Block Registers				
Primary	**Secondary**	**BAR1/BAR3**		
3F6	376	(Primary or Secondary) Base Address + 2	Alternate Status	Device Control

2.1.2.2 BAR4 Registers

BAR4 uses 16 bytes of I/O space. The Bus-master interface base address register (BAR4) defines the base address of the I/O space.

Register Name	Offset Address [Primary/Secondary]
Bus-master IDE Command	00h/08h
Bus-master IDE Status	02h/0Ah
Descriptor Table Pointer	04h/0Ch

Bus-master IDE Command - RW- 8 bits - [IO_Reg: BAR4 + 00/08h]			
Field Name	**Bits**	**Default**	**Description**
Bus Master IDE Start/Stop	0	0b	Bus Master IDE Start (1)/Stop (0). This bit will not be reset by interrupt from IDE device. This must be reset by software (device driver).
Reserved	2:1		Reserved.
Bus Master Read/Write	3	0b	Bus Master IDE r/w (direction) control 0: Memory -> IDE 1: IDE -> Memory This bit should not change during Bus Master transfer cycle, even if terminated by Bus Master IDE Stop.
Reserved	7:4	0h	Reserved.

Bus-master IDE Status - RW- 8 bits - [IO_Reg: BAR4 + 02/0Ah]			
Field Name	**Bits**	**Default**	**Description**
Bus Master Active	0	0b	Bus Master IDE active. This bit is set to 1 when bit[0] in the Bus Master IDE command address register is set to 1. The IDE host controller sets this bit to 0 when the last transfer for a region is performed. This bit is also set to 0 when bit 0 of the Bus Master IDE command register is set to 0.
Bus Master DMA Error	1	0b	IDE DMA error. This bit is set when the IDE host controller encounters a target abort, master abort, or parity error while transferring data on the PCI bus. Writing a 1 clears this bit.
IDE Interrupt	2	0b	IDE Interrupt. Indicates when an IDE device has asserted its interrupt line. IRQ14 is used for the primary channel, and IRQ15 is used for the secondary channel. If the Interrupt Status bit is set to 0, by writing a 1 to this bit while the interrupt line is still at the active level, this bit will remain 0 until another assertion edge is detected on the interrupt line.
Reserved	4:3		Reserved.
Master Device DMA Capable	5	0b	Device 0 (Master) DMA capable.
Slave Device DMA Capable	6	0b	Device 1 (Slave) DMA capable.
Simplex Only	7	0b	Read Only. Simplex only. This bit is hard-wired to 0.

Descriptor Table Pointer - RW- 32 bits - [IO_Reg: BAR4 + 04/0Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved.
Descriptor Table Base Address	31:2	0000_0000h	Base Address of Descriptor Table. These bits correspond to Address [31-02].

2.1.3 SATA Memory Mapped Registers for AHCI Mode

Below are the AHCI memory mapped registers, the base address is defined through the ABAR (BAR5) register.

Register Groups	Offset Address
Generic Host Control registers	00h-2Bh
Reserved registers	2Ch-9Fh
Vendor Specific registers	A0h-FFh
Port 0 port control registers	100h-17Fh
Port 1 port control registers	180h-1FFh
Port 2 port control registers	200h-27Fh
Port 3 port control registers	280h-2FFh
Port 4 port control registers	300h-37Fh
Port 5 port control registers	380h-3FFh
Enclosure Management Buffer registers	500-5FFh

2.1.3.1 Generic Host Control Registers

The following registers apply to the entire HBA.

Generic Host Control Registers	Offset Address
Host Capabilities (CAP)	00h-03h
Global Host Control (GHC)	04h-07h
Interrupt Status (IS)	08h-0Bh
Ports Implemented (PI)	0Ch-0Fh
Version (VS)	10h-13h
Command Completion Coalescing Control (CCC_CTL)	14h-17h
Command Completion Coalescing Ports (CCC_PORTS)	18h-1Bh
Enclosure Management Location (EM_LOC)	1Ch-1Fh
Enclosure Management Control (EM_CTL)	20h-23h
CAP2 (HBA Capabilities Extended)	24-27h
BIOS/OS Handoff Control and Status (BOHC)	28-2Bh
Vendor Specific registers	A0h-FFh

HBA Capabilities – R - 32bits - [Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Number of Ports	4:0	00011b	**NP** - 0's based value indicating the maximum number of ports supported by the HBA silicon. A maximum of 32 ports can be supported. A value of 0h, indicating one port, is the minimum requirement. Note that the number of ports indicated in this field may be more than the number of ports indicated in the GHC.PI register. The default value of this register is 4 ports since HBA is in IDE mode after power-on reset.
Supports External SATA	5	0b	**SXS** 1: Indicates that HBA has one or more Serial ATA ports that have a signal-only connector (i.e. power is not part of that connector) that is externally accessible. If this bit is set to 1, software may refer to the PxCMD.ESP bit to determine whether a specific port has its signal connector externally accessible as a signal-only connector. 0: Indicates that the HBA has no Serial ATA ports that have a signal-only connector externally accessible.
Enclosure Management Supported	6	0b	**EMS** 1: Indicates that HBA supports enclosure management. When enclosure management is supported, the HBA has implemented the EM_LOC and EM_CTL global HBA registers. 0: Indicates that the HBA does not support enclosure management and the EM_LOC and EM_CTL global HBA registers are not implemented.
Command Completion Coalescing Supported	7	1b	**CCCS** 1: Indicates that HBA supports command completion coalescing. When command completion coalescing is supported, HBA has implemented the CCC_CTL and the CCC_PORTS global HBA registers. 0: Indicates that HBA does not support command completion coalescing and the CCC_CTL and CCC_PORTS global HBA registers are not implemented.
Number of Command Slots	12:8	11111b	**NCS** - 0's based value indicate the number of command slots per port supported by this HBA. A minimum of 1 and a maximum of 32 slots per port can be supported. The same number of command slots is available on each implemented port.
Partial State Capable	13	1b	**PSC** - Indicates whether HBA can support transitions to the Partial state. 0: Software must not allow HBA to initiate transitions to the Partial state via agressive link power management nor the PxCMD.ICC field in each port, and the PxSCTL.IPM field in each port must be programmed to disallow device initiated Partial requests. 1: HBA and device initiated Partial requests can be supported.
Slumber State Capable	14	1b	**SSC** - Indicates whether HBA can support transitions to the Slumber state. 0: Software must not allow the HBA to initiate transitions to the Slumber state via agressive link power management nor the PxCMD.ICC field in each port, and the PxSCTL.IPM field in each port must be programmed to disallow device initiated Slumber requests. 1: HBA and device initiated Slumber requests can be supported.

HBA Capabilities – R - 32bits - [Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
PIO Multiple DRQ Block	15	1b	**PMD** 0: HBA only supports single DRQ block data transfers for the PIO command protocol. 1: HBA supports multiple DRQ block data transfers for the PIO command protocol. 0
FIS-based Switching Supported	16	1b	**FBSS** 1: Indicates HBA supports Port Multiplier FIS-based switching. 0: Indicates HBA does not support FIS-based switching. AHCI 1.0 and 1.1 HBAs will have this bit cleared to 0.
Supports Port Multiplier	17	1b	**SPM** - Indicates whether HBA can support a port multiplier. When set, a port multiplier using command-based switching is supported. When cleared to 0, a port multiplier is not supported, and a port multiplier may not be attached to this HBA.
Supports AHCI mode only	18	0b	**SAM** - The SATA controller may optionally support AHCI access mechanisms only. 0: Indicates that in addition to the native AHCI mechanism (via ABAR), the SATA controller implements a legacy, task-file based register interface such as SFF-8038i. 1: Indicates the SATA controller does not implement a legacy, task-file based register interface.
Supports Non-Zero DMA Offsets	19	0b	**SNZO** 1: Indicates HBA can support non-zero DMA offsets for DMA Setup FISes. This bit is reserved for future AHCI enhancements. AHCI 1.0 and 1.1 HBAs will have this bit cleared to 0.
Interface Speed Support	23:20	3h	**ISS** - Indicates the maximum speed HBA can support on its ports. These encodings match the system software programmable PxSCTL.DET.SPD field. Values are: **Bits Definition** 0000 Reserved 0001 Gen1 (1.5 Gbps) 0010 Gen1 and Gen2 (3 Gbps) 0011 Gen1 and Gen2 and Gen3 (6 Gbps) 0011 - 1111 Reserved
Supports Command List Override	24	1b	**SCLO** 1: HBA supports the PxCMD.CLO bit and its associated function. 0: HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.
Supports Activity LED	25	1b	**SAL** 1: HBA supports a single activity indication output pin. This pin can be connected to an LED on the platform to indicate device activity on any drive. 0: This function is not supported.
Supports Aggressive Link Power Management	26	1b	**SALP** 1: HBA can support auto-generating link requests to the Partial or Slumber states when there are no commands to process. 0: This function is not supported and software will treat the PxCMD.ALPE and PxCMD.ASP bits as reserved.
Supports Staggered Spin-up	27	0b	**SSS** 1: HBA supports staggered spin-up on its ports, for use in balancing power spikes. 0: This function is not supported. This value is loaded by the BIOS prior to OS initialization.

HBA Capabilities – R - 32bits - [Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Supports Mechanical Presence Switch	28	1b	**SMPS** 1: HBA supports mechanical presence switches on its ports for use in hot plug operations. 0; This function is not supported. This value is loaded by the BIOS prior to OS initialization.
Supports SNotification Register	29	1b	**SSNTF** 1: HBA supports the PxSNTF (SNotification) register and its associated functionality. 0: HBA does not support the PxSNTF (SNotification) register and its associated functionality.
Supports Native Command Queuing	30	1b	**SNCQ** - Indicates whether HBA supports Serial ATA native command queuing. 1: HBA can handle DMA Setup FISes natively, and can handle the auto-activate optimization through that FIS. 0: Native command queuing is not supported and software should not issue any native command queuing commands.
Supports 64-bit Addressing	31	1b	**S64A** - Indicates whether HBA can access 64-bit data structures. 1: HBA will make the 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry read/write. 0: These bits are read-only and treated as 0s by the HBA.

Global HBA Control – RW - 32bits - [Mem_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
HBA Reset	0	0b	**HR** - When set by software, this bit causes an internal reset of HBA. All state machines that relate to data transfers and queuing shall return to an idle condition, and all ports shall be re-initialized via COMRESET (if staggered spin-up is not supported). If staggered spin-up is supported, then it is the responsibility of software to spin-up each port after the reset has completed. When HBA has performed the reset action, it shall reset this bit to 0. A software write of 0 shall have no effect.
Interrupt Enable	1	0b	**IE** - This global bit enables interrupts from HBA. When cleared (reset default), all interrupt sources from all ports are disabled. When set, interrupts are enabled.
MSI Revert to Single Message	2	0b	**MRSM** - When set to 1by hardware, indicates that HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, HBA has not reverted to single MSI mode (i.e., hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: · MC.MSIE = 1 (MSI is enabled) · MC.MMC > 0 (multiple messages requested) · MC.MME > 0 (more than one message allocated) · MC.MME != MC.MMC (messages allocated not equal to number requested) When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, hardware has been programmed to use single MSI mode, and is not "reverting" to that mode. Read Only
Reserved	30:3	00000000h	Reserved.
AHCI Enable	31	0b	**AE** - When set, indicates that communication to HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. When set, software shall only communicate with HBA using AHCI. When cleared, software shall only communicate with HBA using legacy mechanisms. When cleared, FISes are not posted to memory, and no commands are sent via AHCI mechanisms. Software shall set this bit to 1 before accessing other AHCI registers.

Interrupt Status - RW -32 bits - [Mem_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pending Status	31:0	0h	**IPS** - If set, indicates that the corresponding port has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. The IPS[x] bit is only defined for ports that are implemented or for the command completion coalescing interrupt defined by CCC_CTL.INT. All other bits are reserved. Writing a 1 clear these bits.

Ports Implemented - R - 32 bits - [Mem_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Port Implemented	31:0	0000000Fh	**PI** - This register is bit significant. If a bit is set to 1, the corresponding port is available for software to use. If a bit is cleared to 0, the port is not available for software to use. The maximum number of bits set to 1 shall not exceed CAP.NP + 1, although the number of bits set in this register may be fewer than CAP.NP + 1. At least one bit should be set to 1.

This register indicates which ports are exposed by the HBA. It is loaded by the BIOS. It indicates which ports the HBA supports are available for software to use. For example, on an HBA that supports 6 ports as indicated in CAP.NP, only ports 1 and 3 could be available, with ports 0, 2, 4, and 5 being unavailable. Software must not read or write to registers within unavailable ports. The intent of this register is to allow system vendors to build platforms that support less than the full number of ports implemented on the HBA silicon.

AHCI Version - R – 32 bits - [Mem_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Minor Version Number	15:0	0300h	**MNR** - Indicates the minor version is “30”.
Major Version Number	31:16	0001h	**MJR** - Indicates the major version is “1”.

This register indicates the major and minor version of the AHCI specification that the HBA implementation supports. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h.

Command Completion Coalescing Control (CCC_CTL) - RW – 32bits - [Mem_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
CCC_CTL Enable	0	0h	When cleared to 0, the command completion coalescing feature is disabled and no CCC interrupts are generated. When set to 1, the command completion coalescing feature is enabled and CCC interrupts may be generated based on timeout or command completion conditions. Software shall only change the contents of the TV and CC fields when this bit is cleared to 0. On transition of this bit from 0 to 1, any updated values for the TV and CC fields shall take effect.
Reserved	2:1	0h	Reserved
CCC Interrupt	7:3	1Fh	**INT** - Read Only. Specifies the interrupt used by the CCC feature. This interrupt must be marked as unused in the Ports Implemented register (ABAR + 0Ch) by having the corresponding bit being set to 0. Thus, the CCC interrupt corresponds to the interrupt for an unimplemented port on the controller. When a CCC interrupt occurs, the corresponding bit of ABAR + 08h [31:0] (Interrupt Status. Interrupt Pending Status) shall be asserted to 1. This field also specifies the interrupt vector used for MSI.
Command Completions	15:8	01h	**CC** - Specifies the number of command completions that are necessary to cause a CCC interrupt. The HBA has an internal command completion counter, hCccComplete. hCccComplete is incremented by one each time a selected port has a command completion. When hCccComplete is equal to the command completions value, a CCC interrupt is signaled. The internal command completion counter is reset to 0 on the assertion of each CCC interrupt. A value of 0 for this field shall disable CCC interrupts being generated based on the number of commands completed, i.e. CCC interrupts are only generated based on the timer in this case.
Timeout Value	31:16	0001h	**TV** - The timeout value is specified in 1 millisecond intervals. The timer accuracy shall be within 5%. hCccTimer is loaded with this timeout value. hCccTimer is only decremented when commands are outstanding on selected ports. The HBA will signal a CCC interrupt when hCccTimer has decremented to 0. hCccTimer is reset to the timeout value on the assertion of each CCC interrupt. A timeout value of 0 is reserved.
This register is used to configure the command completion coalescing feature for the entire HBA. **Implementation Note:** HBA state variables (examples include hCccComplete and hCccTimer) are used to describe the required externally visible behavior. Implementations are not required to have internal state values that directly correspond to these variables.			

Command Completion Coalescing Ports - RW – 32bits - [Mem_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Ports	31:0	00000000h	**PRT** - This register is bit significant. Each bit corresponds to a particular port, where bit 0 corresponds to port 0. If a bit is set to 1, the corresponding port is part of the command completion coalescing feature. If a bit is cleared to 0, the port is not part of the command completion coalescing feature. Bits set to 1 in this register must also have the corresponding bit set to 1 in the Ports Implemented register (ABAR + 0Ch). An updated value for this field shall take effect within one timer increment (1 millisecond).
This register is used to specify the ports that are coalesced as part of the CCC feature when CCC_CTL.EN = '1'.			

Enclosure Management Location – R – 32 bits - [Mem_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
Buffer Size	15:0	0000h	**SZ** - Read-Only. Specifies the size of the transmit message buffer area in Dwords. If both transmit and receive buffers are supported, then the transmit buffer begins at ABAR[EM_LOC.OFST*4] and the receive buffer directly follows it. If both transmit and receive buffers are supported, both buffers are of the size indicated in the Buffer Size field. A value of '0' is invalid.
Offset	31:16	0000h	**OFST** - Read-Only. Specifies the offset of the message buffer in Dwords from the beginning of the ABAR.

Enclosure Management Control – RW – 32 bits - [Mem_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
Message Received	0	0b	**STS.MR** - Read & Write '1' Clear. The HBA sets this bit to a '1' when a message is completely received into the message buffer. When software detects this bit is a '1', software will read the message and perform any actions necessary. When software is finished reading the message in the buffer, software writes a '1' to this bit in order to clear it. A write of '0' to this bit by software has no effect.
Reserved	7:1	0b	Read-Only.
Transmit Message	8	0b	**CTL.TM** - Read & Write '1' Set. When set to '1' by software, the HBA shall transmit the message contained in the message buffer. When the message is completely sent, the HBA shall clear this bit to '0'. A write of '0' to this bit by software shall have no effect. Software shall not change the contents of the message buffer while CTL.TM is set to '1'.
Reset	9	0b	**CTL.RST** - Read & Write '1' Set. When set to '1' by software, the HBA shall reset all enclosure management message logic and the attached enclosure processor (if applicable) and take all appropriate reset actions to ensure messages can be transmitted/received after the reset. After the HBA completes the reset operation, the HBA shall set the value to '0'. A write of '0' by software to this field shall have no effect.
Reserved	15:10	0b	Read-Only.
LED Message Types	16	0b	**SUPP.LED** - Read-Only. If set to '1', the HBA supports the LED message type.
SAF-TE Enclosure Management Messages	17	0b	**SUPP.SAFTE** - Read-Only. If set to '1', the HBA supports the SAF-TE message type.
SES-2 Enclosure Management Messages	18	0b	**SUPP.SES2** - Read-Only. If set to '1', the HBA supports the SES-2 message type.

Enclosure Management Control – RW – 32 bits - [Mem_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
SGPIO Enclosure Management Messages	19	0b	**SUPP.SGPIO** - Read-Only. If set to '1', the HBA supports the SGPIO register interface message type.
Reserved	23:20	0h	Read-Only.
Single Message Buffeer	24	0b	**ATTR.SMB** - Read-Only. If set to '1', the HBA has one message buffer that is shared for messages to transmit and messages received. In this case, unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer. If cleared to '0', there are separate receive and transmit buffers such that unsolicited messages could be supported.
Transmit Only	25	0b	**ATTR.XMT** - Read-Only. If set to '1', the HBA only supports transmit messages and does not support receive messages. If cleared to '0', the HBA supports transmit and receive messages.
Activity LED Hardware Driven	26	0b	**ATTR.ALHD** - Read-Only. If set to '1', the HBA drives the activity LED for the LED message type in hardware and does not utilize software settings for this LED. The HBA does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
Port Multiplier Support	27	0b	**ATTR.PM** - Read-Only. If set to '1', the HBA supports enclosure management messages for devices attached via a Port Multiplier. If cleared to '0', the HBA does not. When cleared to '0', software should use the Serial ATA enclosure management bridge that is built into many Port Multipliers for enclosure services with these devices.
Reserved	31:28	0b	Read-Only.

CAP2(HBA Capabilites Extended) – R - 32 bits – [Mem_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
BIOS/OS Handoff	0	0b	**BOH** - When set to 1, the HBA supports the BIOS/OS handoff mechanism. When cleared to 0, the HBA does not support the BIOS/OS handoff mechanism. When BIOS/OS handoff is supported, the HBA has implemented the BOHC global HBA register (Offset:28h). When cleared to 0, it indicates that the HBA does not support BIOS/OS handoff and the BOHC global HBA register is not implemented.
Reserved	31:1	0000h	Reserved. Read Only
This register indicates capabilities of the HBA to driver software.			

BIOS/OS Handoff Control and Status - RW - 32 bits - [Mem_Reg: 28h]			
Field Name	**Bits**	**Default**	**Description**
BIOS Owned Semaphore	0	0b	**BOS** - The BIOS sets this bit to establish ownership of the HBA controller. BIOS will clear this bit in response to a request for ownership of the HBA by system software via OOS.
OS Owned Semaphore	1	0b	**OOS** - The system software sets this bit to request ownership of the HBA controller. Ownership is obtained when this bit reads 1 and the BOS bit reads 0.
SMI on OS Ownership Change Enable	2	0b	**SOOE** - This bit, when set to 1, enables an SMI when the OOC bit has been set to 1.
OS Ownership Change	3	0b	**OOC** - This bit is set to 1 when the OOS bit transitions from 0 to 1. This bit is cleared by writing a 1 to it. Writing 0 has no effect on it.
BIOS Busy	4	0b	**BB** - This bit is used by the BIOS to indicate that it is busy cleaning up for ownership change.
Reserved	31:05	00000000h	Reserved. Read Only
This register controls various global actions of the HBA. **This register is not affected by an HBA reset.**			

2.1.3.2 Port Registers (One Set per Port)

The following registers describe the registers necessary to implement port 0. Additional ports will have the same register mapping. Port 1 starts at 180h, port 2 starts at 200h, port 3 at 280h, etc. The algorithm for software to determine the offset is as follows:

Port offset = 100h + (PI Asserted Bit Position * 80h)

Register Name	Offset Address
Port-N Command List Base Address(PNCLB)	00h-03h + Port offset
Port-N Command List Base Address Upper 32-Bits(PNCLBU)	04h-07h + Port offset
Port-N FIS Base Address(PNFB)	08h-0Bh + Port offset
Port-N FIS Base Address Upper 32-Bits(PNFBU)	0Ch-0Fh + Port offset
Port-N Interrupt Status(PNIS)	10h-13h + Port offset
Port-N Interrupt Enable(PNIE)	14h-17h + Port offset
Port-N Command and Status(PNCMD)	18h-1Bh + Port offset
Reserved	1Ch-1Fh + Port offset
Port-N Task File Data(PNTFD)	20h-23h + Port offset
Port-N Signature(PNSIG)	24h-27h + Port offset
Port-N Serial ATA Status (PNSSTS)	28h-2Bh + Port offset
Port-N Serial ATA Control (PNSCTL)	2Ch-2Fh + Port offset
Port-N Serial ATA Error (PNSERR)	30h-33h + Port offset
Port-N Serial ATA Active (PNSACT)	34h-37h + Port offset
Port-N Command Issue(PNCI)	38h-3Bh + Port offset
Port-N SNotification (PNSNTF)	3Ch-3Fh + Port offset
Reserved for FIS-based Switching Definition	40h-43h + Port offset
Reserved	44h-6Fh + Port offset
Port-N Vendor Specific(PNVS)	70h-7Fh + Port offset

*N is the port number, 0 ~ 7

Port-N Command List Base Address -RW -32 bits [Mem_reg: ABAR + port offset + 00h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	9:0	000h	Reserved.
Command List Base Address	31:10	000000h	**CLB** - Indicates the 32-bit base physical address for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1K-bytes in length. This address must be 1K-byte aligned as indicated by bits 09:00 being read only.

Port-N Command List Base Upper Address -RW - 32 bits [Mem_reg: ABAR + port offset + 04h]			
Field Name	**Bits**	**Default**	**Description**
Command List Base Address Upper	31:0	00000000h	**CLBU** - Indicates the upper 32-bits for the command list base physical address for this port. This base is used when fetching commands to execute. This register shall read only 0 for HBAs that do not support 64-bit addressing.

Port–N FIS Base Address -RW -32 bits [Mem_reg: ABAR + port offset + 08h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	00h	Reserved.
FIS Base Address:	31:8	0h	**FB** - Indicates the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256-byte aligned as indicated by bits 07:00 being read only.

Port-N FIS Base Address Upper –RW – 32 bits [Mem_reg: ABAR + port offset + 0Ch]			
Field Name	**Bits**	**Default**	**Description**
FIS Base Address Upper	31:0	0h	**FBU** - Indicates the upper 32-bits for the received FIS base physical address for this port. This register shall read only 0 for HBAs that do not support 64-bit addressing.

Port–N Interrupt Status - RW - 32 bits [Mem_reg: ABAR + port offset + 10h]			
Field Name	**Bits**	**Default**	**Description**
Device to Host Register FIS Interrupt	0	0b	**DHRS** - When the bit is set, a D2H Register FIS has been received with the 'I' bit set, and has been copied into system memory.
PIO Setup FIS Interrupt	1	0b	**PSS** - When the bit is set, A PIO Setup FIS has been received with the 'I' bit set, and it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
DMA Setup FIS Interrupt	2	0b	**DSS** - When the bit is set, a DMA Setup FIS has been received with the 'I' bit set and has been copied into system memory.
Set Device Bits Interrupt	3	0b	**SDBS** - When the bit is set, a Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.
Unknown FIS Interrupt	4	0b	**UFS** - Read Only . When the bit is set, an unknown FIS was received with the 'I' bit set and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit (ABAR + port offset + 30h[25]) to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when that FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1, or the two bits may become out-of- sync.
Descriptor Processed	5	0b	**DPS** - When the bit is set, a PRD with the 'I' bit set has transferred all of its data.
Port Connect Change Status	6	0b	**PCS** - Read Only 0: No change in *Current Connect Status*. This bit reflects the state of PxSERR.DIAG.X (ABAR + port offset + 30h[26]). This bit is only cleared when PxSERR.DIAG.X is cleared. 1: Change in *Current Connect Status*.
Device Mechanical Presence Status	7	0b	**DMPS** - When set, indicates that a mechanical presence switch attached to this port has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid if both CAP.SMPS(ABAR + 00h[28]) and PxCMD.MPSP (ABAR+port offset+18h[19]) are set to 1.
Reserved	21:8	00h	Reserved
PhyRdy Change Status	22	0b	**PRCS** - Read Only When set to 1 indicates the internal PhyRdy signal changed state. This bit reflects the state of P0SERR.DIAG.N (ABAR + port offset + 30h[16]). To clear this bit, software must clear P0SERR.DIAG.N to 0.
Incorrect Port Multiplier Status	23	0b	**IPMS** - Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. The IPMS bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.

Port–N Interrupt Status - RW - 32 bits [Mem_reg: ABAR + port offset + 10h]			
Field Name	**Bits**	**Default**	**Description**
Overflow Status	24	0b	**OFS** - Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
Reserved	25	0b	Reserved
Interface Non-fatal Error Status	26	0b	**INFS** - Indicates that the HBA encountered an error on the Serial ATA interface and was able to continue operation.
Interface Fatal Error Status	27	0b	**IFS** - Indicates that the HBA encountered an error on the Serial ATA interface, which caused the transfer to stop.
Host Bus Data Error Status	28	0b	**HBDS** - Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
Host Bus Fatal Error Status	29	0b	**HBFS** - Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, it indicates a target or master abort.
Task File Error Status	30	0b	**TFES** - This bit is set whenever the status register is updated by the device and the error bit (bit 0) is set.
Cold Port Detect Status	31	0b	**CPDS** - When set, a device status has changed as detected by the cold presence detect logic. This bit can either be set due to a non-connected port receiving a device, or a connected port having its device removed. This bit is only valid if the port supports cold presence detect as indicated by PxCMD.CPD (ABAR + port offset +18h [20]) set to 1.

Writing a 1 clears these status bits

Port-N Interrupt Enable - RW - 32 bits [Mem_reg: ABAR + port offset + 14h]			
Field Name	**Bits**	**Default**	**Description**
Device to Host Register FIS Interrupt Enable	0	0b	**DHRE** - When set, and if both GHC.IE (ABAR + 04h [1]) and PxIS.DHRS (ABAR+port offset+10h[0]) are set, the HBA will generate an interrupt.
PIO Setup FIS Interrupt Enable	1	0b	**PSE** - When set, if both GHC.IE and PxIS.PSS (ABAR+port offset+10h[1]) are set, the HBA will generate an interrupt.
DMA Setup FIS Interrupt Enable	2	0b	**DSE** - When set, if both GHC.IE and PxIS.DSS (ABAR+port offset+10h[2]) are set, the HBA will generate an interrupt.
Set Device Bits FIS Interrupt Enable	3	0b	**SDBE** - When set, if both GHC.IE and PxIS.SDBS (ABAR+port offset+10h[3]) are set, the HBA will generate an interrupt.
Unknown FIS Interrupt Enable	4	0b	**UFE** - When set, if both GHC.IE and PxIS.UFS (ABAR+port offset+10h[4]) are set to 1, the HBA will generate an interrupt.
Descriptor Processed Interrupt Enable	5	0b	**DPE** - When set, the HBA will generate an interrupt if both GHC.IE and PxIS.DPS (ABAR+port offset+10h[5]) are set.
Port Change Interrupt Enable	6	0b	**PCE** - When set, the HBA will generate an interrupt if both GHC.IE and PxIS.PCS (ABAR+port offset+10h[6]) are set.
Device Mechanical Presence Enable	7	0b	**DMPE** - When set, the HBA will generate an interrupt if both GHC.IE and P0IS.DMPS (ABAR+port offset+10h[7]) are set. For systems that do not support a mechanical presence switch, this bit will be read-only and will return a 0.
Reserved	21:8	000h	Reserved
PhyRdy Change Interrupt Enable	22	0b	**PRCE** - When set, the HBA will generate an interrupt if both GHC.IE and P0IS.PRCS (ABAR+port offset+10h[22]) are set to 1.
Incorrect Port Multiplier Enable	23	0b	**IPME** - When set, the HBA will generate an interrupt if both GHC.IE and P0IS.IPMS (ABAR+port offset+10h[23]) are set.
Overflow Enable	24	0b	**PFE** - When set, the HBA will generate an interrupt if both GHC.IE and P0IS.OFS (ABAR+port offset+10h[24]) are set.
Reserved	25		Reserved
Interface Non-fatal Error Enable	26	0b	**INFE** - When set, the HBA will generate an interrupt if both GHC.IE and P0IS.INFS (ABAR+port offset+10h[26]) are set.

Port-N Interrupt Enable - RW - 32 bits [Mem_reg: ABAR + port offset + 14h]			
Field Name	**Bits**	**Default**	**Description**
Interface Fatal Error Enable	27	0b	**IFE** - When set, the HBA will generate an interrupt if both GHC.IE and P0IS.IFS (ABAR+port offset+10h[27]) are set.
Host Bus Data Error Enable	28	0b	**HBDE** - When set, the HBA will generate an interrupt if both GHC.IE and P0IS.HBDS (ABAR+port offset+10h[28]) are set.
Host Bus Fatal Error Enable	29	0b	**HBFE** - When set, the HBA will generate an interrupt if both GHC.IE and P0IS.HBFS (ABAR+port offset+10h[29]) are set.
Task File Error Enable	30	0b	**TFEE** - When set, the HBA will generate an interrupt if both GHC.IE and P0S.TFES (ABAR+port offset+10h[30]) are set.
Cold Presence Detect Enable	31	0b	**CPDE** - When set, the HBA will generate an interrupt if both GHC.IE and P0S.CPDS (ABAR+port offset+10h[31]) are set. For systems that do not support cold presence detect, this bit will be a read-only and will return a 0.

Port-N Command and Status - RW - 32 bits [Mem_reg: ABAR + port offset + 18h]			
Field Name	**Bits**	**Default**	**Description**
Start	0	0b	**ST** - RW When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI register (ABAR+port offset+38h) is cleared by the HBA upon the HBA putting the controller into an idle state. This bit will only be set to 1 by software after PxCMD.FRE (ABAR+port offset+18h[4]) has been set to 1.
Spin-Up Device	1	1b	**SUD** - This bit is read/write for HBAs that support staggered spin-up via CAP.SSS (ABAR+00h[27]). This bit reads 1 only for HBAs that do not support staggered spin-up. On an edge detect from 0 to 1, the HBA shall start a COMRESET initialization sequence to the device. Clearing this bit does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET (ABAR+port offset+2Ch[3:0])=0h, the HBA will enter listen mode.
Power On Device	2	1b	**POD** - This bit is read/write for HBAs that support cold presence detection on this port as indicated by PxCMD.CPD (ABAR+port offset+18h[20]) set to 1. This bit reads 1 only for HBAs that do not support cold presence detect. When set, the HBA sets the state of a pin on the HBA to 1 so that it may be used to provide power to a cold-presence detectable port.
Command List Override	3	0b	**CLO** - RW Setting this bit to 1 causes PxTFD.STS.BSY(ABAR + port offset + 20h[7]) and PxTFD.STS.DRQ (ABAR + port offset + 20h[3]) to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect. This bit shall only be set to 1 immediately prior to setting the PxCMD.ST bit (bit 0) to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and will result in indeterminate behavior. Software must wait for CLO to be cleared to 0 before setting PxCMD.ST to 1.

Port-N Command and Status - RW - 32 bits [Mem_reg: ABAR + port offset + 18h]			
Field Name	**Bits**	**Default**	**Description**
FIS Receive Enable	4	0b	**FRE** - When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB (ABAR + port offset + 08h) (and for 64-bit HBAs, PxFBU (ABAR + port offset + 0Ch)). When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. System software must not set this bit until PxFB (PxFBU) have been programmed with a valid pointer to the FIS receive area, and if software wishes to move the base, this bit must first be cleared, and software must wait for the FR bit in this register to be cleared.
Reserved	7:5	0h	Reserved
Current Command Slot	12:8	00h	**CCS** - This field is valid when P0CMD.ST (bit 0) is set to 1 and shall be set to the command slot value of the command that is currently being issued by the HBA. When P0CMD.ST transitions from 1 to 0, this field shall be reset to 0. After P0CMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is P0CMD.CCS + 1. For example, after the HBA has issued its first command, if CCS = 0h and P0CI is set to 3h, the next command that will be issued is from command slot 1.
Mechanical Presence Switch State	13	1b	**MPSS** - The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS(ABAR + 00h[28]) and PxCMD.MPSP (ABAR+port offset+18h[19]) are set to 1.
FIS Receive Running	14	0b	**FR** - When set, the FIS Receive DMA engine for the port is running.
Command List Running	15	0b	**CR** - When this bit is set, the command list DMA engine for the port is running.
Cold Presence State	16	0b	**CPS** - The CPS bit reports whether a device is currently detected on this port via cold presence detection. If CPS is set to 1, then the HBA detects via cold presence that a device is attached to this port. If CPS is cleared to 0, then the HBA detects via cold presence that there is no device attached to this port.
Port Multiplier Attached	17	0b	**PMA** - This bit is read/write for HBAs that support a Port Multiplier (CAP.SPM (ABAR+00h[17])= 1). This bit is read-only for HBAs that do not support a port Multiplier (CAP.SPM = 0). When set to 1 by software, a Port Multiplier is attached to the HBA for this port. When cleared to 0 by software, a Port Multiplier is not attached to the HBA for this port. Software is responsible for detecting whether a Port Multiplier is present; hardware does not auto-detect the presence of a Port Multiplier.
Hot Plug Capable Port	18	0b	**HPCP** - When set to 1, it indicates that this port's signal and power connectors are externally accessible via a joint signal and power connector for blindmate device hot plug. When cleared to 0, it indicates that this port's signal and power connectors are not externally accessible via a joint signal and power connector.

Port-N Command and Status - RW - 32 bits [Mem_reg: ABAR + port offset + 18h]			
Field Name	**Bits**	**Default**	**Description**
Mechanical Presence Switch Attached to Port	19	0b	**MPSP** - If set to 1, the platform supports an mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port. When this bit is set to 1, P0CMD.HPCP (bit 18) should also be set to 1.
Cold Presence Detection	20	0b	**CPD** - If set to 1, the platform supports cold presence detection on this port. If cleared to 0, the platform does not support cold presence detection on this port. When this bit is set to 1, P0CMD.HPCP (bit 18) should also be set to 1.
External SATA Port	21	0b	**ESP** - When set to 1, it indicates that this port's signal connector is externally accessible on a signal only connector. When set to 1, CAP.SXS (ABAR + 00h[5]) shall be set to 1. When cleared to 0, it indicates that this port's signal connector is not externally accessible on a signal only connector. ESP is mutually exclusive with the HPCP bit in this register.
FIS-based Switching Capable Port	22	1b	**FBSCP** - When set to 1, it indicates that this port supports Port Multiplier FIS-based switching. When cleared to 0, it indicates that thisport does not support FIS-based switching. This bit may only be set to 1 if both CAP.SPM (ABAR + 00h[17]) and CAP.FBSS (ABAR + 00h[16]) are set to 1.
Reserved	23	0h	Reserved
Device is ATAPI	24	0b	**ATAPI** - RW When set to 1, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
Drive LED on ATAPI Enable	25	0b	**DLAE** - RW When set to 1, the HBA shall drive the LED pin active for commands regardless of the state of P0CMD.ATAPI (ABAR + port offset + 18h[24]). When cleared, the HBA shall only drive the LED pin active for commands if P0CMD.ATAPI is set to 0.
Aggressive Link Power Management Enable	26	0b	**ALPE** - RW When set to 1, the HBA shall aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. Software shall only set this bit to 1 if CAP.SALP (ABAR+00h[26]) is set to 1; if CAP.SALP is cleared to 0 software shall treat this bit as reserved.
Aggressive Slumber / Partial	27	0b	**ASP** - RW When set to 1, and ALPE (bit 26) is set, the HBA shall aggressively enter the Slumber state when it clears the PxCI register (ABAR + port offset + 38h) and the PxSACT register (ABAR + port offset + 34h) is cleared or when it clears the PxSACT register and PxCI is cleared. When cleared, and ALPE is set, the HBA shall aggressively enter the Partial state when it clears the PxCI register and the PxSACT register is cleared or when it clears the PxSACT register and PxCI is cleared. If CAP.SALP(ABAR+00h[26]) is cleared to 0 software shall treat this bit as reserved.

<table>
<tr><th colspan="4">Port-N Command and Status - RW - 32 bits [Mem_reg: ABAR + port offset + 18h]</th></tr>
<tr><th>Field Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>Interface Communication Control</td><td>31:28</td><td>0h</td><td>
ICC - RW

This field is used to control power management states of the interface. If the Link layer is currently in the L_IDLE state, writing to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writing to this field shall have no effect.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>Fh - 7h</td><td>Reserved</td></tr>
<tr><td>6h</td><td>Slumber: This shall cause the HBA to request a transition of the interface to the Slumber state. The SATA device may reject the request and the interface shall remain in its current state.</td></tr>
<tr><td>5h - 3h</td><td>Reserved</td></tr>
<tr><td>2h</td><td>Partial: This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state.</td></tr>
<tr><td>1h</td><td>Active: This shall cause the HBA to request a transition of the interface into the active state.</td></tr>
<tr><td>0h</td><td>No-Op / Idle: When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not have occurred yet.</td></tr>
</table>
When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h).
If software writes to this field to change the state to a state the link is already in (i.e. interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state.
</td></tr>
</table>

<table>
<tr><th colspan="4">Port-N Task Fike Data – R – 32 bits [Mem_reg: ABAR + port offset + 20h]</th></tr>
<tr><th>Field Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>Status</td><td>7:0</td><td>7Fh</td><td>STS - Contains the latest copy of the task file status register. Fields of note in this register that affect AHCI hardware operation are:
<table>
<tr><th>Bit</th><th>Field</th><th>Definition</th></tr>
<tr><td>7</td><td>BSY</td><td>Indicates the interface is busy</td></tr>
<tr><td>6:4</td><td>cs</td><td>Command specific</td></tr>
<tr><td>3</td><td>DRQ</td><td>Indicates a data transfer is requested</td></tr>
<tr><td>2:1</td><td>cs</td><td>Command specific</td></tr>
<tr><td>0</td><td>ERR</td><td>Indicates an error during the transfer.</td></tr>
</table>
</td></tr>
<tr><td>ERROR</td><td>15:8</td><td>00h</td><td>Contains the latest copy of the task file error register.</td></tr>
<tr><td>Reserved</td><td>31:16</td><td>0000h</td><td>Reserved</td></tr>
</table>

<table>
<tr><th colspan="4">Port-N Signature – R – 32 bits [Mem_reg: ABAR + port offset + 24h]</th></tr>
<tr><th>Field Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>Signature</td><td>31:0</td><td>FFFFFFFFh</td><td>SIG - Contains the signature received from a device on the first D2H Register FIS. The bit order is as follows:
<table>
<tr><th>Bit</th><th>Field</th></tr>
<tr><td>31:24</td><td>LBA High Register</td></tr>
<tr><td>23:16</td><td>LBA Mid Register</td></tr>
<tr><td>15:08</td><td>LBA Low Register</td></tr>
<tr><td>07:00</td><td>Sector Count Register</td></tr>
</table>
</td></tr>
<tr><td colspan="4">This register is updated once after each reset sequence.</td></tr>
</table>

Port-N Serial ATA Status – R – 32 bits [Mem_reg: ABAR + port offset + 28h]			
Field Name	**Bits**	**Default**	**Description**
Device Detection	3:0	0h	**DET** - Indicates the interface device detection and PHY state. 0h: No device detected and PHY communication not established. 1h: Device presence detected but PHY communication not established. 3h: Device presence detected and PHY communication established. 4h: PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values are reserved. Read Only.
Current Interface Speed	7:4	0h	**SPD**-Indicates the negotiated interface communication speed. 0h: Device not present or communication not established 1h: Generation 1 communication rate negotiated 2h: Generation 2 communication rate negotiated 3h: Generation 3 communication rate negotiated All other values are reserved. Read Only.
Interface Power Management	11:8	0h	**IPM** - Indicates the current interface state: 0h: Device not present or communication not established. 1h: Interface in Active state. 2h: Interface in Partial power management state. 6h: Interface in Slumber power management state. All other values are reserved. Read Only.
Reserved	31:12	00000h	Reserved

Port-N Serial ATA Control – RW – 32 bits [Mem_reg: ABAR + port offset + 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Device Detection Initialization	3:0	0h	**DET** - Controls the HBA's device detection and interface initialization. 0h: No device detection or initialization action requested 1h: Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h: Disable the Serial ATA interface and put PHY in offline mode. All other values are reserved. This field may only be modified when P0CMD.ST (ABAR + port offset + 18[0]) is 0. Changing this field while the P0CMD.ST bit is set to 1 results in undefined behavior. When P0CMD.ST is set to 1, this field should have a value of 0h. Note: It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when DET=1h.

Port-N Serial ATA Control – RW – 32 bits [Mem_reg: ABAR + port offset + 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Speed Allowed	7:4	0h	**SPD** - Indicates the highest allowable speed of the interface. 0h: No speed negotiation restrictions. 1h: Limit speed negotiation to Generation 1 communication rate. 2h: Limit speed negotiation to a rate not greater than Generation 2 communication rate. 3h: Limit speed negotiation to a rate not greater than Generation 3 communication rate. All other values are reserved.
Interface Power Management Transitions Allowed	11:8	0h	**IPM** - Indicates which power states the HBA is allowed to transition to. If an interface power management state is disabled, the HBA is not allowed to initiate that state and the HBA must $PMNAK_P$ any request from the device to enter that state. 0h: No interface restrictions 1h: Transitions to the Partial state disabled 2h: Transitions to the Slumber state disabled 3h: Transitions to both Partial and Slumber states disabled All other values are reserved.
Select Power Management	15:12	0h	**SPM** - This field is not used by AHCI. Read-Only.
Port Multiplier Port	19:16	0h	**PMP** - This field is not used by AHCI. Read-Only.
Reserved	31:20	000h	Reserved

Port-N Serial ATA Error – RW – 32 bits [Mem_reg: ABAR + port offset + 30h]			
Field Name	**Bits**	**Default**	**Description**
ERROR	15:0	0000h	The ERR field contains error information for use by host software in determining the appropriate response to the error condition. Write 1 to clear. 15:12 - **Reserved** 11 **- Internal Error (E):** The host bus adapter experienced an internal error that caused the operation to fail and may have put the host bus adapter into an error state. The internal error may include a master or target abort when attempting to access system memory, an elasticity buffer overflow, a primitive mis-alignment, a synchronization FIFO overflow, and other internal error conditions. Typically, when an internal error occurs, a non-fatal or fatal status bit in the PxIS register (ABAR + port offset + 10) will also be set to give software guidance on the recovery mechanism required. 10 - **Protocol Error (P):** A violation of the Serial ATA protocol was detected. 9 - **Persistent Communication or Data Integrity Error (C):** A communication error that was not recovered occurred and is expected to be persistent. Persistent communication errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 - **Transient Data Integrity Error (T):** A data integrity error occurred that was not recovered by the interface. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b8b decoding error. 7:2 - **Reserved** 1 - **Recovered Communications Error (M):** Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of PHY synchronization, or from other causes and may be derived from the PhyNRdy signal between the PHY and Link layers. 0 - **Recovered Data Integrity Error (I):** A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b/8b decoding error.

Port-N Serial ATA Error – RW – 32 bits [Mem_reg: ABAR + port offset + 30h]			
Field Name	**Bits**	**Default**	**Description**
Diagnostics	31:16	0000h	**DIAG** - Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes: 31:27 - **Reserved** 26 - **Exchanged (X):** When set to 1 this bit indicates a COMINIT signal was received. This bit is reflected in the P0IS.PCS bit. 25 - **Unknown FIS Type (F):** Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized/known. 24 - **Transport state transition error (T):** Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. This bit is always 0 in the current implementation. 23 - **Link Sequence Error (S):** Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. This bit is always 0 in the current implementation. 22 - **Handshake Error (H):** Indicates that one or more R_ERR handshake responses were received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 - **CRC Error (C):** Indicates that one or more CRC errors occurred with the Link Layer. 20 - **Disparity Error (D):** *This field is not used by AHCI.* This bit is always 0 in the current implementation. 19 - **10b to 8b Decode Error (B):** Indicates that one or more 10b to 8b decoding errors has occurred. 18 - **Comm Wake (W):** Indicates that a Comm Wake signal was detected by the PHY. 17 - **Phy Internal Error (I):** Indicates that the PHY detected some internal error. This bit is always 0 in the current implementation. 16 - **PhyRdy Change (N):** Indicates that the PhyRdy signal changed state. This bit is reflected in the P0IS.PRCS bit (Mem_reg: ABAR + port offset + 10h[22]). Write 1 to clear.

Port-N Serial ATA Active [Mem_reg: ABAR + port offset + 34h]			
Field Name	**Bits**	**Default**	**Description**
Device Status	31:0	00000000h	**DS** - This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. This field is set by software prior to issuing a native queued command for a particular command slot. Prior to writing PxCI[TAG] to 1, software will set DS[TAG] to 1 to indicate that a command with that TAG is outstanding. The device clears bits in this field by sending a Set Device Bits FIS to the host. The HBA clears bits in this field that are set to 1 in the SActive field of the Set Device Bits FIS. The HBA only clears bits that correspond to native queued commands that have completed successfully. Software should only write this field when PxCMD.ST (ABAR+port offset+18h[0]) is set to 1. This field is cleared when PxCMD.ST is written from a 1 to a 0 by software. This field is not cleared by a COMRESET or a software reset.

Port-N Command Issue – RW – 32 bits [Mem_reg: ABAR + port offset + 38h]			
Field Name	**Bits**	**Default**	**Description**
Commands Issued	31:0	00000000h	**CI** - This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when PxCMD.ST (ABAR+port offset+18h[0]) is set to 1. This field is also cleared when PxCMD.ST is written from a 1 to a 0 by software.

Port- N SNotification – RWC – 32 bits [Mem_reg: ABAR + port offset + 3Ch]			
Field Name	**Bits**	**Default**	**Description**
PM Notify	15:0	0000h	**PMN** - This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the host with the Notification bit set. PM Port 0h sets bit 0 … PM Port Fh sets bit 15 Individual bits are cleared by software writing 1's to the corresponding bit positions. This field is reset to default on a HBA Reset, but it is not reset by COMRESET or software reset.
Reserved	31:16	0000h	Reserved

Port-N FIS-based Switching Control – RW – 32 bits [Mem_reg: ABAR + port offset + 40h]			
Field Name	**Bits**	**Default**	**Description**
Enable	0	0	**EN** - When set to 1, a Port Multiplier is attached and the HBA shall use FIS-based switching to communicate with it. When cleared to 0, FIS-based switching is not being used. Software shall only change the value of the EN bit when PxCMD.ST (ABAR+port offset+18h[0]) is cleared to 0.
Device Error Clear	1	0	**DEC** - When set to 1 by software, the HBA shall clear the device-specific error condition and the HBA shall flush any commands outstanding for the device that experienced the error, including clearing the PxCI (ABAR+port offset+38h) and PxSACT bits for that device to 0. When hardware has completed error recovery actions, hardware shall clear the bit to 0. A write of 0 to this bit by software shall have no effect. Software shall only set this bit to 1 if PxFBS.EN (bit 0) is set to 1 and PxFBS.SDE (bit 2) is set to 1.
Single Device Error	2	0	**SDE** - When set to 1 and a fatal error condition has occurred, hardware believes the error is localized to one device such that software's first error recovery step should be to utilize the PxFBS.DEC (bit 1) functionality. When cleared to 0 and a fatal error condition has occurred, the error applies to the entire port and to clear the error PxCMD.ST (ABAR+port offset+18h[0]) shall be cleared to 0 by software. This bit is cleared on PxFBS.DEC being set to 1 or on PxCMD.ST (ABAR+port offset+18h[0]) being cleared to 0.
Reserved	7:3	0h	Reserved
Device To Issue	11:8	0h	**DEV** - Set by software to the Port Multiplier port value of the next command to issue. This field enables hardware to know the port the command is to be issued to without fetching the command header. Software shall not issue commands to multiple Port Multiplier ports on the same write of the PxCI (ABAR+port offset+38h) register.
Active Device Optimization	15:12	2h	**ADO** - This register exposes the number of active devices that the FIS-based switching implementation has been optimized for. When there are more devices active than indicated in this field, throughput of concurrent traffic may degrade. For optimal performance, software should limit the number of active devices based on this value. The minimum value for this field shall be 2h, indicating that at least two devices may be active with high performance maintained.
Device With Error	19:16	0h	**DWE** - Set by hardware to the value of the Port Multiplier port number of the device that experienced a fatal error condition. This field is only valid when PxFBS.SDE (bit 2) = 1.
Reserved	31:20	000h	Reserved

2.1.3.3 Enclosure Buffer Management Register Set

The following registers belong to Enclosure Buffer Management, starting from ABAR + EMB.OFST*4 + 00h to ABAR + EMB.OFST*4 + FFh.

Message Header – RW – 32 bits [Mem_reg: ABAR + EMB.OFST*4 + 00h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	00h	**Read-only** This field is reserved.
Message Size	15:8	00h	**MSIZE** - **Read/Write** Specifies the size of the message in bytes. The message size does not include the one Dword header. A value of ‘0’ is invalid. To reduce complexity, current hardware implementation treats this field as don’t-care. It is defined for future use.
Data Size	23:16	00h	**DSIZE** - **Read/Write** Specifies the data size in bytes. If the message (enclosure services command) has a data buffer that is associated with it that is transferred, the size of that data buffer is specified in this field. If there is no separate data buffer, this field shall have a value of ‘0’. The data directly follows the message in the message buffer. To reduce complexity, current hardware implementation treats this field as don’t-care. It is defined for future use.
Message Type	27:24	00h	**MTYPE** - **Read/Write** Specifies the type of the message.The message types are: 0h – LED 1h – SAF-TE 2h – SES-2 3h – SGPIO (register based interface) All other values reserved. To reduce complexity, current hardware implementation treats this field as don’t-care. It is defined for future use.
Reserved	31:28	00h	**Read-only** This field is reserved.

Write SGPIO Register Request I – RW – 32 bits [Mem_reg: ABAR + EMB.OFST*4 + 04h]			
Field Name	**Bits**	**Default**	**Description**
Frame Type	7:0	00h	**FRAME_TYPE** - **Read/Write** To be compatible with existing SGPIO-aware software, this field shall be set to 40h when performing any command issued to SGPIO targets. However, to reduce complexity, current hardware implementation treats this field as don't-care.
Function	15:8	00h	**FUNC** - **Read/Write** To be compatible with existing SGPIO-aware software, this field shall be set to 82h when performing any command issued to SGPIO targets. However, to reduce the complexity, current hardware implementation treats this field as don't-care.
Register Type	23:16	00h	**REG_TYPE** - **Read/Write** Specifies the bank of registers to write. Currently supported Register Types are: 00h: SGPIO Configuration 03h: Transmit 04h: General Purpose Transmit C0h: AMD Configuration All other values are reserved It is software's responsibility to make sure the type of register that it attempts to access is valid and supported, as hardware does not provide a mechanism to return a status to software indicating that the current operation fails. This field has a second functionality when combined with ABAR + F4h[1:0]. It serves as the MUX select to read out the designated internal SGPIO registers to locations starting from (ABAR + EMB.OFST*4 + 0Ch).
Register Index	31:24	00h	**REG_INDX** - **Read/Write** Specifies the index of the first register in the bank to write. Currently supported index range is: REG_TYPE=00h: 0 to1 REG_TYPE=03h: 0 REG_TYPE=04h: 0 to7 REG_TYPE=0Ch: 0 It is software's responsibility to make sure the index of which the first register it attempts to access is valid and supported, as hardware does not provide a mechanism to return a status to software indicating that the current operation fails. An out-of-range index for a specific type of register will be treated as don't care and none of the data for such index will be written.

Write SGPIO Register Request II – RW – 32 bits [Mem_reg: ABAR + EMB.OFST*4 + 08h]			
Field Name	**Bits**	**Default**	**Description**
Register Count	7:0	00h	**REG_CNT** - **Read/Write** Specifies the number of registers starting with the specified index to write. Currently supported register count range is: REG_TYPE=00h: 1 to 2 REG_TYPE=03h: 1 REG_TYPE=04h: 1 to 8 REG_TYPE=0Ch: 1 It is software's responsibility to make sure the register count is valid and supported, as hardware does not provide a mechanism to return a status to software indicating that the current operation fails. An out-of-range register count for a specific type of register will be treated as don't care and none of the data for such register count will be written.
Reserved	31:8	0h	**Read-only** This field is reserved.

Write SGPIO Register Request II – RW – 32 bits [Mem_reg: ABAR + EMB.OFST*4 + 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Data Register 0-7	255:0	0h	(ABAR + EMB.OFST * 4 + 0Ch) to (ABAR + EMB.OFST * 4 + 2Bh) houses 256 bits of data registers. Once Register Type, Index, and Count are specified, the values in this field will be written to the internal copies of SGPIO register.

Reserved – R – 32 bits [Mem_reg: ABAR + EMB.OFST*4 + 2Ch to FFh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	211:0	0h	From 2Ch to FFh, these fields are reserved and read-only.

2.1.4 IDE Controller PCI Configuration Registers (Device 20, Function 1)

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID/Class Code	08h
Cache Link Size	0Ch
Master Latency Timer	0Dh
Header Type	0Eh
BIST Mode Type	0Fh
Base Address 0	10h
Base Address 1	14h
Base Address 2	18h
Base Address 3	1Ch
Bus Master Interface Base Address	20h
Reserved	24-28h
Subsystem ID and Subsystem Vendor ID	2Ch
Reserved	30h
Capabilities Pointer	34h

Register Name	Offset Address
Reserved	38h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min_gnt	3Eh
Max_latency	3Fh
IDE Internal Control	40h
Reserved	42h
Watch Dog Control And Status	44h
Watch Dog Counter	46h
Reserved	48h
IDE Internal Control 2	4Ah
Reserved	4Ch-67h
IDE MSI Programmable Weight	68h
Reserved	69-6Fh
IDE MSI Control	70h
IDE MSI Address Register	74h
IDE MSI Data Register	78h
Reserved	7C-7Fh
IDE IDP Address Register	80h
IDE IDP Data Register	84h

Vendor ID - R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Vendor Identifier. This register holds a unique 16-bit value assigned to a vendor, and combined with the device ID it identifies any PCI device

Device ID - R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	780Ch	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID it, identifies any PCI device.

Command – RW – 16 bits – [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
I/O Access Enable	0	0b	I/O Access Enable. This bit controls access to the I/O space registers. When this bit is 1, it enables access to Legacy IDE ports, and PCI bus master IDE I/O registers are enabled.
Memory Access Enable	1	0b	Memory Access Enable. This function is not implemented. This bit is always 0.
Bus Master Enable	2	0b	Master Enable. Bus master function enable. 1=enable, 0=disable.
Special Cycle Recognition Enable	3	0b	Read Only. Hard-wired to 0 indicates that no special support.
Memory Write and Invalidate Enable	4	0b	Read Only. Hard-wired to 0 indicates that memory write and invalidate command is not supported.
VGA Palette Snoop Enable	5	0b	Read Only. VGA Palette Snoop Enable- The IDE host controller does not need to snoop VGA palette cycles. This bit is always 0.
PERR# Detection Enable	6	0b	PERR- (Response) Detection Enable bit – If set to 1, the IDE host controller asserts PERR# when it is the agent receiving data AND it detects a parity error. PERR# is not asserted if this bit is 0. Default - 0.

Command – RW – 16 bits – [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
Wait Cycle Enable	7	0b	Read Only. Wait Cycle enable - The IDE host controller does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
SERR# Enable	8	0b	SERR- enable – If set to 1, the IDE host controller asserts SERR# when it detects an address parity error. SERR# is not asserted if this bit is 0. Default – 0.
Fast Back-to-Back Enable	9	0b	Read Only. Fast Back-to-back enable. The IDE host controller only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
Interrupt Disable	10	0b	Interrupt disable bit (comply to PCI 2.3 spec.)
Reserved	15:11	00h	Reserved. Always wired as 0's.

Command Register: The PCI specification defines this register to control a PCI device's ability to generate and respond to PCI cycles.

Status – RW – 16 bits – [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0b	Reserved. These bits are always read as 0.
Interrupt Status	3	0b	Interrupt status bit. It complies with the PCI 2.3 specification.
Capabilities List	4	1b	Default to 1 to indicate that the Capabilities Pointer is located at 34h.
66MHz Support	5	1b	66MHz capable. This feature is supported in the IDE host controller.
Reserved	6	0b	Reserved.
Fast Back-to-Back Capable	7	0b	Read Only. Fast Back-to-Back Capable. This feature is not implemented and this bit is always 0.
Data Parity Error	8	0b	Data Parity reported – Set to 1 if the IDE host controller detects PERR# asserted while acting as PCI master (whether PERR# was driven by IDE host controller or not.)
DEVSEL# Timing	10:9	01b	Read Only. DEVSEL# timing – Read only bits indicating DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
Signaled Target Abort	11	0b	Signaled Target Abort – This bit is set to 1, when the IDE host controller signals Target Abort.
Received Target Abort	12	0b	Received Target Abort – This bit is set to 1 when the IDE host controller-generated PCI cycle (IDE host controller is the PCI master) is aborted by a PCI target. Cleared by writing a 1 to it.
Received Master Abort Status	13	0b	Received Master Abort Status. Set to 1 when the IDE host controller acting as a PCI master, aborts a PCI bus memory cycle. Cleared by writing a 1 to this bit. Default – 0.
SERR# Status	14	0b	SERR# status. This bit is set to 1 when the IDE host controller detects a PCI address parity error.
Detected Parity Error	15	0b	Detected Parity Error. This bit is set to 1 when the IDE host controller detects a parity error.

Status Register: The PCI specification defines this register to record status information for PCI related events. This is a read/write register. However, writes can only reset bits. A bit is reset when the register is written and the data in the corresponding bit location is a 1.

Revision ID/Class Code- RW - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	00h	These bits are default to 00h to indicate the revision level of the chip design.
IDE Host Controller Operating Mode Selection	15:8	8Ah	Programmable interface. These 8 bits are read/write. Bit 15 – Master IDE Device. Always 1. Bit 14-12 – Reserved. Always read as 0's. Bit 11 – Programmable indicator for Secondary. Always 1 to indicate that both modes are supported. Bit 10 – Operating Mode for Secondary. 1 = Native PCI-mode. 0 = Compatibility Mode (Default). Bit 9 – Programmable indicator for Primary. Always 1 to indicate that both modes are supported. Bit 8 – Operating Mode for Primary. 1 = Native PCI-mode. 0 = Compatibility mode (Default).
Sub-Class Code	23:16	01h	Sub-Class Code. These 8 bits are read-only and wired to 01h to indicate an IDE Controller.
Class Code	31:24	01h	Class Code. These 8 bits are read-only and wired to 01h to indicate a Mass-Storage Controller.
Revision ID/Class Code Register: This register contains the device's revision information, generic function of a device, and the specific register level programming interface. The Base class is 01h (Mass-Storage Controller), Sub-class is 01h (IDE Controller).			

Cache Link Size – RW – 8 bits – [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Reserved
Cache Link Size Register	7:4	00h	If the value is 1, it means the cache line size is 16 DW (64 byte).

Cache Line Size Register: This register specifies cache line size and the default value is 00.

Master Latency Timer – RW – 8 bits – [PCI_Reg:0Dh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0h	Not used and wired to 0.
Master Latency Timer	7:3	00h	Master Latency Timer. This number represents the guaranteed time slice allotted to IDE host controller for burst transactions.

Master Latency Timer: This register specifies the value of Latency Timer in units of PCICLKs.

Header Type – R – 8 bits – [PCI_Reg:0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	00h	Read Only. Header Type. Since the IDE host controller is a single-function device, this register contains a value of 00h.

Header Type Register: This register identifies the IDE controller module as a single function device.

BIST Mode Type – R – 8 bits – [PCI_Reg:0Fh]			
Field Name	**Bits**	**Default**	**Description**
Built-in-Self Test Mode	7:0	00h	Read Only. Built-in-Self Test modes. Since the IDE host controller does not support BIST modes, this register is always read as 00.

BIST Mode Type Register: This register is used for control and status for Built-in-Self test. The IDE host controller has no BIST modes

Base Address 0 – RW – 32 bits – [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	2:1	00b	Reserved. Always read as 0's.
Primary IDE CS0 Base Address	31:3	0000_0000h	Base Address for Primary IDE Bus CS0. This register is used for native mode only. Base Address 0 is not used in compatibility mode.

Base Address 0 Register (Primary CS0): When Channel Select (ACPI PCI configuration offset 0xDA bit 1) is set, SATA port 4/5 uses Secondary channel. The Primary channel is un-used.

Base Address 1 – RW – 32 bits – [PCI_Reg:14h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	1	0b	Reserved. Always read as 0's.
Primary IDE CS1 Base Address	31:2	0000h	Base Address for Primary IDE Bus CS1. This register is used for native mode only. Base Address 1 is not used in compatibility mode.

Base Address 1 Register (Primary CS1): When Channel select is (ACPI PCI configuration offset 0xDA bit 1) is set, SATA port 4/5 uses Secondary channel. The Primary channel is un-used.

Base Address 2 – RW – 32 bits – [PCI_Reg:18h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	2:1	00b	Reserved. Always read as 0's.
Secondary IDE CS0 Base Address	31:3	0000_0000h	Base Address for Secondary IDE Bus CS0. This register is used for native mode only. Base Address 2 is not used in compatibility mode.

Base Address 2 Register (Secondary CS0): When Channel select is (ACPI PCI configuration offset 0xDA bit 1) is cleared, SATA port 4/5 uses Primary channel. The Secondary channel is un-used.

Base Address 3 – RW – 32 bits – [PCI_Reg:1Ch]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	1	0b	Reserved. Always read as 0's.
Secondary IDE CS1 Base Address	31:2	0000_0000h	Base Address for Secondary IDE Bus CS1. This register is used for native mode only. Base Address 3 is not used in compatibility mode.

Base Address 3 Register (Secondary CS1): When Channel select is (ACPI PCI configuration offset 0xDA bit 1) is cleared, SATA port 4/5 uses Primary channel. The Secondary channel is un-used .

Bus Master Interface Base Address – RW – 32 bits – [PCI_Reg:20h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	3:1	0h	Reserved. Always read as 0's.
Bus Master Interface Register Base Address	31:4	0000_0000h	Base Address for Bus Master interface registers and correspond to AD[31:4].

Bus Master Interface Base Address Register: This register selects the base address of a 16-byte I/O space interface for bus-master functions.

Reserved Register – R – 32 bits – [PCI_Reg:24h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	00000000h	Reserved. Always read as 0's.

Reserved Register – R – 32 bits – [PCI_Reg:28h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	00000000h	Reserved. Always read as 0's.

Subsystem ID and Subsystem Vendor ID – RW – 32 bits – [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	Subsystem Vendor ID
Subsystem ID	31:16	0000h	Subsystem ID

Subsystem ID and Subsystem Vendor ID: This subsystem ID and subsystem Vendor ID register is write once and read only.

Reserved Register – R – 32 bits – [PCI_Reg:30h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	00000000h	Reserved. Always read as 0's.

MSI Capabilities Pointer – R – 32 bits – [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	70h	The first pointer of Capability block.
Reserved	31:8	000000h	Reserved. Always read as 0's.

MSI Capabilities Pointer Register: This register will show the pci configuration register starting address and it is read-only.

Reserved Register – R – 32 bits – [PCI_Reg:38h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	00000000h	Reserved. Always read as 0's.

Interrupt Line – RW – 8 bits – [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	Identifies which input on the interrupt controller the function's PCI interrupt request pin (as specified in its Interrupt Pin register) is being routed to.

Interrupt Line Register: This register identifies which of the system interrupt controllers the device interrupt pin is connected to. The value of this register is used by device drivers.

Interrupt Pin – R – 8 bits – [PCI_Reg:3Dh]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin	7:0	02h	Default value is 02h, corresponding to use IntB#.

Interrupt Pin Register: This register identifies the interrupt pin a device uses. Since the IDE host controller uses IRQ14, this value is supposed to be 00. However, the IDE controller will generate the PCI interrupt INTB# signal on the PCI bus. Therefore, this pin register is set to 02h.

Min_gnt – R – 8 bits – [PCI_Reg:3Eh]			
Field Name	**Bits**	**Default**	**Description**
Minimum Grant	7:0	00h	Hard-wired to 0's and always read as 0's.

Min_gnt Register: This register specifies the desired settings for how long of a burst the IDE host controller needs assuming a clock rate of 33MHz. The value specifies a period of time in units of ¼ microseconds.

Max_latency – R – 8 bits – [PCI_Reg:3Fh]			
Field Name	**Bits**	**Default**	**Description**
Maximum Latency	7:0	00h	Hard-wired to 0's and always read as 0's.

Max_latency Register: This register specifies the Maximum Latency time required before the IDE host controller as a bus-master can start an accesses.

IDE Internal Control – RW- 16 bits – [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
CC_reg_wr_en	0	0b	Once set, the following registers are programmable Revion ID (PCI_Reg08h[7:0]), Capability List (PCI_Reg06h[4]), Capabilities Pointer (PCI_Reg34h[7:0]), Interrup Pin ((PCI_Reg3Dh[7:0]), MSI Capability Next Pointer (PCI_Reg70h[15:8]), Multiple Message Capable bits (PCI_Reg70h[19:17])
Primary channel enable	1	1b	This is the scratch register for AMD driver INF file to indicate the Primary channel present. It has no affect on hardware.
Secondary channel enable	2	1b	This is the scratch register for AMD driver INF file to indicate the Secondary channel present. It has no affect on hardware.
Disable the fix for MSI Interrupt enable.	3	0b	When set, MSI out put will affect by PCI_CFG 0x04[10] interrupt disable and MSI enable. If not set, MIS output is only controlled by MSI enable
Reserved	13:4	00h	Reserved for read/write enable.
SATA back door access PCI Configuration or BAR5 space	14	0b	Indicate back door access type of SATA HBA PCI configuration space or BAR 5 access. 0: PCI configuration access 1: BAR 5 access
Reserved	15	0b	Reserved for read/write enable.

Reserved Register – R – 16 bits – [PCI_Reg:42h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	0000h	Reserved. Always read as 0's.

Watch Dog Control And Status - RW - 16 bits - [PCI_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
Watchdog Enable	0	0b	Set the bit to enable the watchdog counter for all the PCI down stream transaction for PATA ports.
PATA Watchdog Timeout Status	1	0b	PATA Watchdog Counter Timeout Status bit. This bit indicates that the watchdog counter in a PATA port has expired for PCI down stream transaction and the transaction got aborted due to counter has expired. Software writes 1 to clear the status
Reserved	15:2	0b	Reserved. Read/write-able.

This register is used from preventing system hang. Reset Condition: PCI Reset, or Power Management State transition from D3 to D0.

Watch Dog Counter - RW - 16 bits - [PCI_Reg:46h]			
Field Name	**Bits**	**Default**	**Description**
Watchdog Counter	7:0	80h	Specifies the timeout retry count for PCI down stream retries. This value is used for PATA ports.
Reserved	15:8	00h	Reserved. Read/write-able.

This register is used for preventing system hangs. Reset Condition: PCI Reset, or Power Management State transition from D3 to D0.

Reserved Register 48h49h - R - 16 bits - [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	00h	Reserved. Always read as 0's

IDE Internal Control 2 - RW - 16 bits - [PCI_Reg:4Ah]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	00h	Reserved. Read/write-able.
Reserved	11:8	0h	Reserved. Read/write-able.
SW disable Primary channel	12	0b	When set, IDE Primary Channel is disabled in register level.
SW disable Secondary channel	13	0b	When set, IDE Secondary Channel is disabled in register level.
Reserved	15:14	0h	Reserved. Read/write-able.

This register is used for preventing system hangs. Reset Condition: PCI Reset, or Power Management State transition from D3 to D0.

Reserved Register – R – 224 bits – [PCI_Reg:4Ch]-- [PCI_Reg:67h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	223:0	0h	Reserved. Always read as 0's.

IDE MSI Programmable Weight - RW- 8 bits - [PCI_Reg:68h]			
Field Name	**Bits**	**Default**	**Description**
MSI Interrupt Weight	5:0	01h	MSI programmable interrupt weight.
Reserved	7:6	0h	Reserved. Always wired as 0's.

This register specifies MSI weight.

Reserved Register – R – 56 bits – [PCI_Reg:69h] -- [PCI_Reg:6Fh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	55:0	0h	Reserved. Always read as 0's.

IDE MSI Control - RW- 32 bits - [PCI_Reg:70h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	05h	Capability ID (hard_wired to 05h)
Capability Next Pointer	15:8	00h	Next Pointer (hard_wired to 00h).
Message Signaled Interrupt Enable	16	0b	MSI Enable (MSI_En)
Multiple Message Capable	19:17	0h	Multiple Message Capable (MMC).
Multiple Message Enable	22:20	0h	Multiple Message Enable (MME).
MSI 64-bit Address	23	0b	64-bit address (hard_wired to 0b)
Reserved	31:24	00h	Reserved. Always wired as 0's.

IDE MSI Control Register: This register specifies MSI Capability ID, next pointer, MSI enable, multiple message capable, multiple message enable bits.

IDE MSI Address Register - RW- 32 bits - [PCI_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**
IDE MSI Address	31:0	0000_0000h	MSI Address

IDE MSI Address Register: This register specifies MSI address.

IDE MSI Data Register - RW- 32 bits - [PCI_Reg:78h]			
Field Name	**Bits**	**Default**	**Description**
IDE MSI Data	15:0	0000h	MSI Data
Reserved	31:16	0000h	Reserved. Always wired as 0's.

IDE MSI Data Register: This register specifies MSI data.

Reserved Register – R – 32 bits – [PCI_Reg:7Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved. Always read as 0's.

IDE Index-Data-Pair (IDP) Indexing Register - RW- 32 bits - [PCI_Reg:80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved. Always wired as 0's.
IDE IDP Index	10:2	000h	Index-data-pair Address
Reserved	31:11	000000h	Reserved. Always wired as 0's.

IDE IDP Address Register: This register specifies indirect address to access SATA PCI configuration space or memory space pointed by SATA BAR 5.

IDE IDP Data Register - RW- 32 bits - [PCI_Reg:84h]			
Field Name	**Bits**	**Default**	**Description**
IDE IDP Data	31:0	0000_0000h	Index-data-pair Data This register is a "window" through which data is read or written to the memory mapped register pointed to by the IDP indexing register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers or PCI configuration registers. Since this is not a physical register, the "default" value is the same as the default value of the register pointed to by IDP indexing.

IDE IDP Data Register: This register specifies IDP data read from or write to SATA block

2.2 USB Registers

2.2.1 USB 1.1/2.0 Control Registers inside ACPI

2.2.1.1 PMIO Registers

Certain USB functions are also controlled by the PMIO registers. PMIO registers are accessed through address/data ports via IO 0xCD6 and 0xCD7 (Index is programmed into IO 0xCD6 and the data is through IO 0xCD7).

The following are such PMIO registers located inside the ACPI SmBus controller (refer to *section 3.3, "Power Management (PM) Registers," on page 3- 278* for details):

BreakEvent [PM_Reg: 80h] (see bits 21:16)
UsbGating [PM_Reg: EDh]
UsbEnable [PM_Reg:EFh]
UsbControl [PM_Reg: F0h]
UsbReset [PM_Reg: F3h]

2.2.1.2 Misc IO Registers

By default, USB interrupts are routed to PCI INTA#, B#, and C#.

The following registers are Misc IO registers located inside the ACPI Smbus controller that show all interrupt mapping information (see *section 3.17, "Interrupt Routing Registers," on page 3- 476* for details):

Pci_Intr_Index [IO_Reg: C00h]
Pci_Intr_Data [IO_Reg: C01h]

2.2.2 USB1/USB2 (Device-18/19, func-0) OHCI PCI Configuration Registers

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID / Class Code	08h
Miscellaneous	0Ch
BAR_OHCI	10h
Subsystem Vendor ID / Subsystem ID	2Ch
Capability Pointer	34h
Interrupt Line	3Ch
Config Timers / MSI Disable	40h – 41h
Port Disable Control	42h
USB PHY Battery Charger	46h
Port Force Reset	48h
OHCI Misc Control 1	50h
OHCI Misc Control 2	52h
Over Current Control 1	58h
OHCI OverCurrentPME Enable	68h
Target Timeout Control	74h
	78h
	7Ch
OHCI Spare1	80h

Register Name	Offset Address
MSI Control	D0h
MSI Address	D4h
MSI Data	D8h
HT MSI Support	E4h
Function Level Reset Capability	F0h
Function Level Reset Control	F4h

Vendor ID – R – 16 bits – [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Vendor Identifier. The vendor ID is 0x1022.

Device ID – R – 16 bits – [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	Function 0: 7807h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device.

Command – RW – 16 bits – [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Space Accesses	0	0b	0: Disable the device response. 1: Allow the device to respond to I/O Space accesses.
Memory Space Accesses	1	0b	0: Disable the device response. 1: Allow the device to respond to Memory Space accesses.
Bus Master	2	0b	0: Disable the device from generating PCI accesses. 1: Allow the device to behave as a bus master.
Special Cycle	3	0b	Hard-wired to 0, indicating no Special Cycle support.
Memory Write and Invalidate Command	4	0b	0: Memory Write must be used. 1: Masters may generate the command.
VGA Palette Register Accesses	5	0b	Hard-wired to 0, indicating the device should treat palette write accesses like all other accesses.
Parity Enable	6	0b	0: the device sets its Detected Parity Error status bit (bit [15] in the Status register) when an error is detected, but continues normal operations without asserting PERR#. 1: The device must take its normal action when a parity error is detected.
Reserved	7	0b	Hard-wired to 0 per PCI2.3 spec.
SERR# Enable	8	0b	0: Disable the SERR# driver. 1: Enable the SERR# driver. Note: Address parity errors are reported only if this bit and bit [6] are 1.
Fast Back-to-Back Enable	9	0b	0: Only fast back-to-back transactions to the same agent are allowed. 1: The master is allowed to generate fast back-to-back transactions to different agents.
Interrupt Disable	10	0b	0: Enable the assertion of the device/function's INTx# signal. 1: Disable the assertion of the device/function's INTx# signal.
Reserved	15:11		Reserved

Status – R – 16 bits – [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0		Reserved
Interrupt Status	3	0b	This bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0, and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
Capabilities List	4	1b	0: Indicates that no New Capabilities linked list is available. 1: Indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
66 MHz Capable	5	1b	Hard-wired to 1, indicating 66MHz capable.
Reserved	6		Reserved
Fast Back-to-Back Capable	7	1b	Hard-wired to 1, indicating Fast Back-to-Back capable.
Master Data Parity Error	8	0b	This bit is set when any of the following three conditions is met: (1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); (2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit (Command register) is set.
DEVSEL Timing	10:9	01b	Hard-wired to 01b – Medium timing
Signaled Target Abort	11	0b	This bit is set by a target device whenever it terminates a transaction with Target-Abort.
Received Target Abort	12	0b	This bit is set by a master device whenever its transaction is terminated with Target-Abort.
Received Master Abort	13	0b	This bit is set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort.
Signaled System Error	14	0b	This bit is set whenever the device asserts SERR#.
Detected Parity Error	15	0b	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit [6] in the Command register).

Revision ID / Class Code – R – 32 bits – [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	11h	Revision ID. The value 11h indicates revision A11.
PI	15:8	10h	Programming Interface. A constant value of 10h identifies the device being an OpenHCI Host Controller.
SC	23:16	03h	Sub Class. A constant value of 03h identifies the device being of Universal Serial Bus.
BC	31:24	0Ch	Base Class. A constant value of 0Ch identifies the device being a Serial Bus Controller.

Miscellaneous – RW – 32 bits – [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This read/write field specifies the system cache line size in units of DWORDs and must be initialized to 00h.
Latency Timer	15:8	00h	Bits [9:8] are hard-wired to 00b, resulting in a timer granularity of at least four clocks. This field specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.
Header Type	23:16	80h/00h	This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space), and also whether or not the device contains multiple functions. Function 0: Bit [23] hard-wired to 1 → the device has multiple functions. Function 1: Bit [23] hard-wired to 0 → the device is single function. Bits [22:16] hard-wired to 00h.
BIST	31:24	00h	Hard-wired to 00h, indicating no build-in BIST support.

Bar_OHCI – RW – 32 bits – [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
IND (R)	0	0b	Indicator. Read-Only. A constant value of 0 indicates that the operational registers of the device are mapped into memory space of the main memory of the PC host system.
TP (R)	2:1	0h	Type. Read-Only. A constant value of 00b indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space; i.e., lower 4 GB of the main memory of the PC host.
PM (R)	3	0b	Prefetch memory. Read-Only. A constant value of 0 indicates that there is no support for “prefetchable memory”.
Reserved	11:4	00h	These bits are read-only and hardwired to zero.
BAR	31:12	000h	Base Address. Specifies the upper 20 bits of the 32-bit starting base address. This represent a maximum of 4-kbyte addressing space for the OpenHCI’s operational registers.

Subsystem Vendor ID / Subsystem ID – RW – 32 bits – [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	1022	Can only be written once by software.
Subsystem ID	31:16	7807	Can only be written once by software.

Capability Pointer – R – 8 bits – [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capability Pointer	7:0	D0h	Address of the 1st element of capability link.

Interrupt Line – RW – 32 bits – [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	The Interrupt Line register is an eight-bit register used to communicate interrupt line routing information. The register is read/write and must be implemented by any device (or device function) that uses an interrupt pin. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value; rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.
Interrupt Pin	15:8	01h	Read-Only by default *. Hard-wired to 01h, corresponding to using INTA#
MIN_GNT	23:16	00h	Read-Only. Hardwired to 00h to indicate no major requirements for the settings of Latency Timers.
MAX_LAT	31:24	00h	Read-only. Hardwired to 00h to indicate no major requirements for the settings of Latency Timers.
* If Interrupt Backdoor Enable bit (OHCI regx50[7]) is set, this field is writable.			

Config Timers / MSI Disable – RW – 16 bits – [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
TRDY Timer	7:0	80h	Target Ready timer to timeout non-responding target.
MSI Disable	8	1b	When set, MSI capability is disabled.
Reserved	15:9	00h	Reserved

Port Disable – RW – 16 bits – [PCI_Reg:42h]			
Field Name	**Bits**	**Default**	**Description**
Port_Disable	4:0 *	00h	When these bits are set, the corresponding ports are disabled. For example, if bit [0] is set, then port-0 (its corresponding port) is disabled; if bit [1] is set, then its corresponding port (port-1) is disabled (and so on). Only value 1 can be written into the register, the bit can be cleared to 0 only by system reset (PciRst#). That is, when the bit is set to 1, the value is locked and cannot be cleared by any software write. The register can only be cleared by hardware reset.
Reserved	11:5	00h	Reserved
Reserved	15:12	Fh	Reserved
* Bit[4] in USB3 is a reserved bit.			

USB PHY Battery Charger – RW – 16 bits – [PCI_Reg:46h]			
Field Name	**Bits**	**Default**	**Description**
USB PHY Battery Charger Enable	4:0 *	00h	One bit controls one respective port. Set to 1 to enable USB PHY battery charger function.
Reserved	15:5	000h	Reserved
* Bit [4] in USB3 is a reserved bit.			

Port Force Reset – RW – 16 bits – [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
Port0 Force Reset Enable	1:0	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Port1 Force Reset Enable	3:2	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Port2 Force Reset Enable	5:4	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Port3 Force Reset Enable	7:6	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Port4 Force Reset Enable	9:8 *	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Reserved	15:10	00h	Reserved
* Bits [9:8] in USB3 are reserved bits.			

OHCI Misc Control 1 – RW – 16 bits – [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
OHCI Dynamic Power Saving Enable	0	0b	When this bit is set, Dynamic Power Saving for OHCI is enabled**.** By default, the power saving function is disabled. Note: This bit must be set to 0.
OHCIShortSimMsCount	1	0b	When enabled, loads reduced times into the millisecond counter for faster OHCI simulations.
A20 State Function	3:2	00b	Used to override how A20 State is combined from 5 OHCIs' reg0x100[8]: 00: OR 01: NAND 10: NOR 11: AND
cfg_did_vid enable	4	0b	Enable backdoor device id/vendor id modification for all the controllers.
HT MSI Support Enable	5	0b	Set to 1 to enable AMD K8 Hyper-Transport MSI support.
OHCI Cache Enable	6	1b	Enable 64 byte OHCI DMA cache.
	7		
OHCI Prefetch Cache Line Count	9:8	11b	Number of data cache lines prefetch requests for ISO out transaction. 00: Prefetch is disabled. 01: 1 cache line 10: 2 cache lines 11: 3 cache lines
OHCI Prefetch Time Out Timer	11:10	00b	Time out timer to purge the prefetch data in AB data FIFO if the data is not used. 00: 255ms 01: 511ms 10: 767ms 11: 1023ms
SMI Handshake Disable	12	1b	If this bit is set, the handshake between USB and ACPI is disabled when SMI is requested by USB
	13		
OHCIFmControl	14	0b	If this bit is enabled, the HcFmRemaining and HcFmNumber registers of OHCI Memory Mapped Registers are writable.
OHCI Disconnect Detection Time	15	0b	Set the bit to increase the OHCI disconnect (SE0 state) detection time. 0: 2.33 micro-seconds 1: 6.16 micro-seconds
This register is shared among all the OHCI controllers if the Share Register Enable bit (OHCI_Pci_config x52[12]) is set.			

OHCI Misc Control 2 – RW – 16 bits – [PCI_Reg:52h]			
Field Name	**Bits**	**Default**	**Description**
C4 Early Exit Timer	1:0	00	Timer to control the C4 exit. USB OHCI controller send C4 break up request ahead of time before the next DMA request ready. 00: 20 micro seconds 01: 30 micro seconds 10: 35 micro seconds 11: 40 micro seconds
C4 Early Exit Enable	2	0b	Set the bit to 1 to enable early C4 exit function. This bit should be set only when the system supports C4.
SOF_sync_en	3	0b	Set this bit to enable sync up SOF for all OHCI controllers

OHCI Misc Control 2 – RW – 16 bits – [PCI_Reg:52h]			
Field Name	**Bits**	**Default**	**Description**
OHCI Advance Plist Enable	4	0b	Set this bit to enable advancing Plist
	5	0b	
OHCI Packet Buffer Threshold	7:6	00b	Control the threshold of OHCI packet buffer. 00: 48 bytes 01: 128 bytes 10: 200 bytes 11: 256 bytes
OHCI Loopback Control Register Enable	8	0b	Set the bit to Enable HcLoopBackControl Register (OHCI Mem_reg xF0). The HcLoopBackControl register is hidden by default and can only be accessed by software when this bit is set.
OHCI L1 Block Disable	9	0b	OHCI L1 Block Disable 0: enable 1: disable
FLR Enable	10	0b	Set to 1 to enable FLR support.
FLR SMI Enable	11	0b	Set to 1 to enable FLR SMI and to disable HW FLR function. This is the back-door control bit that, in case HW does not behave as expected, disables HW FLR function and enables SMI on FLR to let SW handle the reset sequence. This bit will have effect only if FLR Enable (bit[10]) is set to 1.
Share Register Enable	12	1b	Set the bit to enable register sharing among all OHCI as well as all EHCI controllers. Software can write to any enabled OHCI (or EHCI) controller's share register and the same value will reflect in other OHCI (or EHCI) controllers' shared register. Software can clear the bit to disable register sharing. This means the value written to one controller won't reflect in another equivalent controller.
OHCI Hold Resume Enable	13	1b	Set the bit to enable OHCI holding resume signaling on remote resume detection.
Wake On Resume Enhancement Enable	14	1b	Set the bit to enable USB S3 wake on resume enhancement.
PME Merge Disable	15	1b	Set the bit to disable merging PMEs from all 4 USB controllers.
This register is shared among all the OHCI controllers if the Share Register Enable bit (OHCI_Pci_config x52[12]) is set.			

Over Current Control 1 – R – 32 bits – [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
HS Port0 OverCurrent Control	3:0	Fh	This register controls the OverCurrent pin mapping for port-0. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-0.
HS Port1 OverCurrent Control	7:4	Fh	This register controls the OverCurrent pin mapping for port -1. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-1.
HS Port2 OverCurrent Control	11:8	Fh	This register controls the OverCurrent pin mapping for port -2. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-2.

Over Current Control 1 – R – 32 bits – [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
HS Port3 OverCurrent Control	15:12	Fh	This register controls the OverCurrent pin mapping for port -3. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-3.
HS Port4 OverCurrent Control *	19:16	Fh	This register controls the OverCurrent pin mapping for port -4. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-4.
Reserved	31:20	0h	Reserved.
There are 8 pins that can be used for USB OverCurrent function: USB_OC0#/JTG_RST#/GEVENT12#, USB_OC1#/JTG_TDI#/GEVENT13#, USB_OC2#/JTG_TCK#/GEVENT14#, USB_OC3#/JTG_TDO#/GEVENT15#, USB_OC4#/IR_RX0/GEVENT16#, USB_OC5#/IR_TX0/GEVENT17#, USB_OC6#/IR_TX1/GEVENT6, USB_OC7#/LEDBlink/GEVENT18# Register value-to-OverCurrent pin mapping: USB_OC0# = 0000, USB_OC1# = 0001, USB_OC2# = 0010, USB_OC3# = 0011, USB_OC4# = 0100, USB_OC5# = 0101, USB_OC6# = 0110, USB_OC7# = 0111 Note: Since OverCurrent pins can be used as GPM# as well, the corresponding register bits to set the pin as OverCurrent have to be set in Smbus Controller. *: USB3 does not have Port4 so the control field has no effect, but the default is still Fh.			

OHCI OverCurrent PME Enable – RW – 16 bits – [PCI_Reg:68h]			
Field Name	**Bits**	**Default**	**Description**
OHCI OverCurrent PME Enable	4:0	00h	Writing this bit to 1 enables the respective port to be sensitive to over-current conditions as wake-up events when it is owned by OHCI.
Reserved	15:5	00h	Reserved

Target Timeout Control – RW – 32 bits – [PCI_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**
Retry Counter	7:0	FFh	Counter to control the purge of the delay queue when the downstream access cycle is not completed within certain time. The transaction is target aborted when counter expired. The retry counter can be disabled by writing 00h in this register.
Reserved	23:8	0000h	Reserved
Timeout Timer	31:24	80h	Timer to control the purge of the delay queue when the master that has initiated the access does not return to complete the transaction. After the timer expires, the queue is invalidated and the next transaction is serviced.

OHCI Spare1 – RW – 32 bits – [PCI_Reg:80h]			
Field Name	**Bits**	**Default**	**Description**
OHCI L1 Early Exit Enable	0	0b	OHCI L1 Early Exit Enable 0: disable 1: enable
OHCI L1 Early Exit Timer Select	3:1	101b	Timer to control the OHCI L1 exit. When OHCI L1 Early Exit Enable is set to 1, this field selects the amount of time before SOF that the OHCI controller will request that UMI to exit from L1. 000: 20 micro seconds 001: 30 micro seconds 010: 40 micro seconds 011 : 50 micro seconds 100: 60 micro seconds 101: 70 micro seconds 110: 80 micro seconds 111: 90 micro seconds
OHCI Arbiter Mode	5:4	0b	OHCI Arbiter Mode 00: Disable 01: Request Fix Enable 10: Grant Fix Enable 11: Request + Grant Fix Enable Set USB_ohci_arb_vld_ctl whenever Grant Fix Enable is set
OHCI Local Deep B-Link Power Saving Enable	6	0b	When enabled, OHCI B-Link clock will be gated when the list proc is idle and the cache master is idle. Note: This bit is “don't care”.
OHCI Global Deep B-Link Power Saving Enable	7	0b	When enabled, OHCI will request to stop the global B-Link clock when the list proc is idle and the cache master is idle.
USB_ohci_arb_vld_ctl	8	0b	When set, slot valid signal in OHCI ariber can be cleared per slot instead of per host. Set this bit whenever setting OHCI Arbiter Mode[1].
Reserved	9	0b	Reserved
LoadByte Sync Control	10	0b	When set, OHCI will fine tune LoadByte sync logic.
RxCrc16Match Sync	11	0b	When set, OHCI will fine tune RxCrc16Match sync logic
OHCI Resume Timer Mode	12	0b	OHCI Resume Timer Mode 0: Disable (default) 1: Enable
Reserved	13	0b	Reserved
OHCI Resume EOR Mode	14	0b	OHCI Resume EOR Mode 0: Disable (default) 1: Enable
USB Resume Hold Mode	15	0b	USB Resume Hold Mode 0: Disable (default) 1: Enable
Reserved	31:16	0h	Reserved

MSI Control – RW - 32 bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
MSI USB	7:0	05h	MSI USB ID. Read-only.
Next Item Pointer	15:8	00h/F0h*	Pointer to next capability structure
MSI Control Out	16	0b	Set to 1 to disable IRQ. Use MSI instead.
Reserved	19:17	0h	Reserved
MSI Control	22:20	0h	MSI control field
Reserved	31:23	00h	Reserved
* Note: The Next Item Pointer can be either 00h or F0h depending on whether the FLR Enable bit (OHCI0_pci_config x50[13]) is disabled or enabled respectively.			

MSI Address – RW - 32 bits - [PCI_Reg:D4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0		Reserved. Read-only.
MSI Address	31:2	0h	System-specified message address.

MSI Data – RW - 16 bits - [PCI_Reg:D8h]			
Field Name	**Bits**	**Default**	**Description**
MSI Data	15:0	0h	System-specified message.

HT MSI Support – R - 32 bits - [PCI_Reg:E4h]			
Field Name	**Bits**	**Default**	**Description**
HT MSI Support	31:0	0h *	For AMD K8 HyperTransport MSI support. Read-only.
* Note: When HT MSI Support Enable, OHCI0 Misc Control 1 x50[5], is set to 1, the default of this register will be A8030008h.			

Function Level Reset Capability – R - 32 bits - [PCI_Reg:F0h]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	13h	Read-only. The value of 13h in this field identifies that the function as being AF capable.
Next Item Pointer	15:8	00h/E4h	Read-only. Pointer to next capability structure. This is the final item on the list.
Length	23:16	06h	Read-only. AF structure length (byte).
Transaction Pending Capability	24	1b	Read-only. Transaction pending support.
Function Level Reset Capability	25	1b	Read-only. Function level reset support.
Reserved	31:26		

Function Level Reset Control – RO - 32 bits - [PCI_Reg:F4h]			
Field Name	**Bits**	**Default**	**Description**
Initiate FLR	0	0b	A write of 1 initiates Function Level Reset (FLR). The value read by software from this bit will always be 0.
Reserved	7:1		
Transaction pending	8	0b	Read-only. A value of 1b indicates that the Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. A value of 0b indicates that all non-posted transactions have been completed.
Reserved	31:9		

2.2.3 USB4 (device-20, func-5) OHCI PCI Configuration Registers

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID / Class Code	08h
Miscellaneous	0Ch
BAR_OHCI	10h
Subsystem Vendor ID / Subsystem ID	2Ch
Capability Pointer	34h
Interrupt Line	3Ch
Config Timers / MSI Disable	40h – 41h
Port Disable Control	42h
USB1.1 Pad Control	44h
Port Force Reset	48h
OHCI Misc Control 1	50h
OHCI Misc Control 2	52h
Over Current Control 1	58h
OHCI OverCurrent PME Enable	68h
Target Timeout Control	74h
	78h
	7Ch
OHCI Spare1	80h
MSI Control	D0h
MSI Address	D4h
MSI Data	D8h
	E4h
	F0h
	F4h

Vendor ID – R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Vendor Identifier. The vendor ID is 0x1022.

Device ID – R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	Function 0: 7809h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device.

Command – RW - 16 bits - [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Space Accesses	0	0b	0: Disable the device response. 1: Allow the device to respond to I/O Space accesses.
Memory Space Accesses	1	0b	0: Disable the device response. 1: Allow the device to respond to Memory Space accesses.
Bus Master	2	0b	0: Disable the device from generating PCI accesses. 1: Allow the device to behave as a bus master.
Special Cycle	3	0b	Hard-wired to 0, indicating no Special Cycle support.
Memory Write and Invalidate Command	4	0b	0: Memory Write must be used. 1: Masters may generate the command.
VGA Palette Register Accesses	5	0b	Hard-wired to 0, indicating the device should treat palette write accesses like all other accesses.
Parity Enable	6	0b	0: the device sets its Detected Parity Error status bit (bit [15] in the Status register) when an error is detected, but continues normal operations without asserting PERR#. 1: The device must take its normal action when a parity error is detected.
Reserved	7	0b	Hard-wired to 0 per PCI 2.3 spec.
SERR# Enable	8	0b	0: Disable the SERR# driver. 1: Enable the SERR# driver. Note: Address parity errors are reported only if this bit and bit [6] are 1.
Fast Back-to-Back Enable	9	0b	0: Only fast back-to-back transactions to the same agent are allowed. 1: The master is allowed to generate fast back-to-back transactions to different agents.
Interrupt Disable	10	0b	0: Enable the assertion of the device/function's INTx# signal. 1: Disable the assertion of the device/function's INTx# signal.
Reserved	15:11		Reserved

Status – R - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0		Reserved
Interrupt Status	3	0b	This bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0, and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
Capabilities List	4	1b	0: Indicates that no New Capabilities linked list is available. 1: Indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
66 MHz Capable	5	1b	Hard-wired to 1, indicating 66MHz capable.
Reserved	6		Reserved
Fast Back-to-Back Capable	7	1b	Hard-wired to 1, indicating Fast Back-to-Back capable.

Status – R - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Master Data Parity Error	8	0b	This bit is set when any of the following three conditions is met: (1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); (2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit (Command register) is set.
DEVSEL Timing	10:9	01b	Hard-wired to 01b – Medium timing
Signaled Target Abort	11	0b	This bit is set by a target device whenever it terminates a transaction with Target-Abort.
Received Target Abort	12	0b	This bit is set by a master device whenever its transaction is terminated with Target-Abort.
Received Master Abort	13	0b	This bit is set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort.
Signaled System Error	14	0b	This bit is set whenever the device asserts SERR#.
Detected Parity Error	15	0b	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit [6] in the Command register).

Revision ID / Class Code – R - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	11h	Revision ID. The value 11h indicates the reversion A11.
PI	15:8	10h	Programming Interface. A constant value of 10h identifies the device being an OpenHCI Host Controller.
SC	23:16	03h	Sub Class. A constant value of 03h identifies the device being of Universal Serial Bus.
BC	31:24	0Ch	Base Class. A constant value of 0Ch identifies the device being a Serial Bus Controller.

Miscellaneous – RW/R - 32 bits - [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This read/write field specifies the system cache line size in units of DWORDs and must be initialized to 00h.
Latency Timer	15:8	00h	Bits [9:8] are hard-wired to 00b, resulting in a timer granularity of at least four clocks. This field specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.
Header Type	23:16	80h/00h	This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space), and also whether or not the device contains multiple functions. Function 0: Bit [23] hard-wired to 1 → the device has multiple functions. Function 1: Bit [23] hard-wired to 0 → the device is single function. Bits [22:16] hard-wired to 00h.
BIST	31:24	00h	Hard-wired to 00h, indicating no build-in BIST support.

Bar_OHCI – RW - 32 bits - [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
IND	0	0b	Indicator. Read-only. A constant value of 0 indicates that the operational registers of the device are mapped into memory space of the main memory of the PC host system.
TP	2:1	0h	Type. Read-only. A constant value of 00b indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space; i.e., lower 4 GB of the main memory of the PC host.

Bar_OHCI – RW - 32 bits - [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
PM	3	0b	Prefetch memory. Read-only. A constant value of 0 indicates that there is no support for “prefetchable memory”.
Reserved	11:4	00h	These bits are read-only and hardwired to zero.
BAR	31:12	000h	Base Address. Specifies the upper 20 bits of the 32-bit starting base address. This represent a maximum of 4-kbyte addressing space for the OpenHCI’s operational registers.

Subsystem Vendor ID / Subsystem ID – RW - 32 bits - [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	1022	Can only be written once by software.
Subsystem ID	31:16	7809	Can only be written once by software.

Capability Pointer – R - 8 bits - [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capability Pointer	7:0	D0h	Address of the 1st element of capability link.

Interrupt Line – RW – 32 bits - [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	The Interrupt Line register is an eight-bit register used to communicate interrupt line routing information. The register is read/write and must be implemented by any device (or device function) that uses an interrupt pin. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value; rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.
Interrupt Pin	15:8	03h	Read-only by default *. Hard-wired to 03h, corresponding to using INTA#
MIN_GNT	23:16	00h	Read-only. Hardwired to 00h to indicate no major requirements for the settings of Latency Timers.
MAX_LAT	31:24	00h	Read-only. Hardwired to 00h to indicate no major requirements for the settings of Latency Timers.
* If Interrupt Backdoor Enable bit (OHCI regx50[7]) is set, this field is writable.			

Config Timers / MSI Disable – RW - 16 bits - [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
TRDY Timer	7:0	80h	Target Ready timer to timeout non-responding target.
MSI Disable	8	1b	When set, MSI capability will be disabled.
Reserved	15:9	00h	Reserved

Port Disable – RW* - 16 bits - [PCI_Reg:42h]			
Field Name	**Bits**	**Default**	**Description**
Port_Disable	4:0	00h	When these bits are set, the corresponding ports are disabled. For example, if bit [0] is set then port-0 (its corresponding port) is disabled; if bit [1] is set, then its corresponding port (port-1) is disabled (and so on). Only value 1 can be written into the register, the bit can be cleared to 0 by system reset (PciRst#). That is, when the bit is set to 1, the value is locked and cannot be cleared by any software write.
Reserved	11:5	00h	Reserved
Reserved	15:12	Fh	Reserved
* Only writing value 1 takes effect on the register value, software writing 0 has no effect. The register can only be cleared by hardware reset.			

USB1.1 Pad Control (USB4 OHCI only) – RW - 16 bits - [PCI_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
PMOS Driving Strength Control	2:0	001b	Driving strength for the LS/FS Port0 pad PMOS transistors
Reserved	3	0b	Reserved
NMOS Driving Strength Control	6:4	001b	Driving strength for the LS/FS Port1 pad NMOS transistors
Reserved	7	0b	Reserved
Reserved	15:8	00h	Reserved

Port Force Reset – RW - 32 bits - [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
LS/FS Port0 Force Reset Enable	1:0	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
LS/FS Port1 Force Reset Enable	3:2	00h	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Reserved	15:4	00h	Reserved

OHCI Misc Control 1 – RW - 16 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
OHCI Dynamic Power Saving Enable	0	0b	When this bit is set, Dynamic Power Saving for OHCI is enabled. By default, the power saving function is disabled.
OHCIShortSimMsCount	1	0b	When enabled, loads reduced times into the milli-second counter for faster OHCI simulations.
A20 State Function	3:2	00b	Used to override how A20 State is combined from 5 OHCIs' reg0x100[8]: 00: OR 01: NAND 10: NOR 11: AND
cfg_did_vid enable	4	0b	Enable backdoor device id/vendor id modification for all the controllers.
HT MSI Support Enable	5	0b	Set to 1 to enable AMD K8 Hyper-Transport MSI support.
OHCI Cache Enable	6	1b	Enable 64 byte OHCI DMA cache.
Interrupt Backdoor Enable	7	0b	When set, bits [15-8] of the Interrupt Line register, which are read only by default, will become writable.
OHCI Prefetch Cache Line Count	9:8	11b	The related logic may be removed as packet buffer size will be increased. Number of data cache lines prefetch requests for ISO out transaction. 00: Prefetch is disabled. 01: 1 cache line 10: 2 cache lines 11: 3 cache lines
OHCI Prefetch Time Out Timer	11:10	00b	Time out timer to purge the prefetch data in AB data FIFO if the data is not used. 00: 255ms 01: 511ms 10: 767ms 11: 1023ms
SMI Handshake Disable	12	1b	If this bit is set, the handshake between USB and ACPI is disabled when SMI is requested by USB
	13		
OHCIFmControl	14	0b	If this bit is enabled, the HcFmRemaining and HcFmNumber registers of OHCI Memory Mapped Registers are writable.
OHCI Disconnect Detection Time	15	0b	Set the bit to increase the OHCI disconnect (SE0 state) detection time. 0: 2.33 micro-seconds 1: 6.16 micro-seconds
This register is shared among all the OHCI controllers if the Share Register Enable bit (OHCI_Pci_config x52[12]) is set.			

OHCI Misc Control 2 – RW - 16 bits - [PCI_Reg:52h]			
Field Name	**Bits**	**Default**	**Description**
C4 early exit timer	1:0	00	Timer to control the C4 exit. USB OHCI controller send C4 break up request ahead of time before the next DMA request ready. 00: 20 micro seconds 01: 30 micro seconds 10: 35 micro seconds 11: 40 micro seconds
C4 early exit enable	2	0b	Set the bit to 1 to enable early C4 exit function. This bit should be set only when the system supports C4.

OHCI Misc Control 2 – RW - 16 bits - [PCI_Reg:52h]			
Field Name	**Bits**	**Default**	**Description**
SOF_sync_en	3	0b	Set this bit to enable sync up SOF for all OHCI controllers
OHCI Advance PList Enable	4	0b	Set this bit to enable advancing PList
	5	0b	
OHCI Packet Buffer Threshold	7:6	00b	Control the threshold of OHCI packet buffer. 00: 48 bytes 01: 128 bytes 10: 200 bytes 11: 256 bytes
OHCI loopback control register enable	8	0b	Set the bit to Enable HcLoopBackControl Register (OHCI Mem_reg xF0). The HcLoopBackControl register is hidden by default and can only be accessed by software when this bit is set.
OHCI L1 Block Disable	9	0b	OHCI L1 Block Disable 0: enable 1: disable
FLR Enable	10	0b	Set to 1 to enable FLR support
FLR SMI enable	11	0b	Set to 1 to enable FLR SMI and to disable HW FLR function. This is the back-door control bit that, in case HW does not behave as expected, disables HW FLR function and enables SMI on FLR to let SW handle the reset sequence. The bit will have effect only if “FLR Enable” (x52[10]) is set.
Share register Enable	12	1b	Set this bit to enable register sharing among all OHCI as well as all EHCI controllers. Software can write to any enabled OHCI (or EHCI) controller’s shared register and the same value will reflect in other OHCI (or EHCI) controllers’ shared register. Software can clear the bit to disable the register sharing. This means the value write to one controller won’t reflect in another equivalent controller.
OHCI Hold Resume Enable	13	1b	Set the bit to enable OHCI holding resume signaling on remote resume detection.
Wake On Resume Enhancement Enable	14	1b	Set the bit to enable USB S3 wake on resume enhancement.
PME Merge Disable	15	1b	Set the bit to disable merging PMEs from all 4 USB controllers.
This register is shared among all the OHCI controllers if the Share Register Enable bit (OHCI_Pci_config x52[12]) is set.			

Over Current Control 1 – R - 32 bits - [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
FS Port0 OverCurrent Control	3:0	Fh	The register is to control the OverCurrent pin mapping for full-speed port-0. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for full-speed port-0.
FS Port1 OverCurrent Control	7:4	Fh	The register is to control the OverCurrent pin mapping for full-speed port-1. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for full-speed port-1.
Reserved	31:8		Reserved
There are 8 pins that can be used as USB OverCurrent function: USB_OC0#/JTG_RST#/GEVENT12#, USB_OC1#/JTG_TDI#/GEVENT13#, USB_OC2#/JTG_TCK#/GEVENT14#, USB_OC3#/JTG_TDO#/GEVENT15#, USB_OC4#/IR_RX0/GEVENT16#, USB_OC5#/IR_TX0/GEVENT17#, USB_OC6#/IR_TX1/GEVENT6, USB_OC7#/LEDBlink/GEVENT18# Register value-to-OverCurrent pin mapping: USB_OC0# = 0000, USB_OC1# = 0001, USB_OC2# = 0010, USB_OC3# = 0011, USB_OC4# = 0100, USB_OC5# = 0101, USB_OC6# = 0110, USB_OC7# = 0111 Note: Since OverCurrent pins can be used as GPM# as well, the corresponding register bits to set the pin as OverCurrent have to be set in Smbus Controller.			

OHCI OverCurrent PME Enable – RW - 16 bits - [PCI_Reg:68h]			
Field Name	**Bits**	**Default**	**Description**
OHCI OverCurrent PME Enable	1:0	00h	Writing this bit to 1 enables the respective port to be sensitive to over-current conditions as wake-up events when it is owned by OHCI.
Reserved	15:10	00h	Reserved

Target Timeout Control – RW - 32 bits - [PCI_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**
Retry Counter	7:0	FFh	Counter to control the purge of the delay queue when the host controller does not return the ack. After the counter expires, the transaction is target aborted. The retry counter can be disabled by writing 00h in this Register.
Reserved	23:8	0000h	Reserved
Timeout Timer	31:24	80h	Timer to control the purge of the delay queue when the master that has initiated the access does not return to complete the transaction. After the timer expires the queue is invalidated and the next transaction is serviced.

OHCI Spare1 – RW - 32 bits - [PCI_Reg:80h]			
Field Name	**Bits**	**Default**	**Description**
OHCI L1 Early Exit Enable	0	0b	OHCI L1 Early Exit Enable 0: disable 1: enable
OHCI L1 Early Exit Timer Select	3:1	101b	Timer to control the OHCI L1 exit. When OHCI L1 Early Exit Enable is set to 1, this field selects the amount of time before SOF that the OHCI controller will request that UMI to exit from L1. 000: 20 micro seconds 001: 30 micro seconds 010: 40 micro seconds 011: 50 micro seconds 100: 60 micro seconds 101: 70 micro seconds 110: 80 micro seconds 111: 90 micro seconds
OHCI Arbiter Fix Enable	5:4	0b	OHCI Arbiter Fix Enable 00: Disable 01: Request Fix Enable 10: Grant Fix Enable 11: Request + Grant Fix Enable
OHCI Local Deep Blink Power Saving Enable	6	0b	When enabled, OHCI Blink clock will be gated when the list proc is idle and the cache master is idle.
OHCI Global Deep Blink Power Saving Enable	7	0b	When enabled, OHCI will request to stop the global Blink clock when the list proc is idle and the cache master is idle.
USB_ohci_arb_vld_ctl	8	0b	When set, slot valid signal in OHCI ariber can be cleared per slot instead of per host. Set this bit whenever setting OHCI Arbiter Mode[1].
Reserved	9	0b	Reserved
LoadByte Sync Control	10	0b	When set, OHCI will fine tune LoadByte sync logic.
RxCrc16Match Sync	11	0b	When set, OHCI will fine tune RxCrc16Match sync logic
OHCI Resume Timer Mode	12	0b	OHCI Resume Timer Mode 0: Disable (default) 1: Enable
Reserved	13	0b	Reserved
OHCI Resume EOR Mode	14	0b	OHCI Resume EOR Mode 0: Disable (default) 1: Enable
USB Resume Hold Mode	15	0b	USB Resume Hold Mode 0: Disable (default) 1: Enable
Reserved	31:16	0h	Reserved

MSI Control – RW - 32 bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
MSI USB	7:0	05h	MSI USB ID. Read-only.
Next Item Pointer	15:8	00h/F0h	Pointer to next capability structure
MSI Control Out	16	0b	Set to 1 to disable IRQ. Use MSI instead.
Reserved	19:17	0h	Reserved
MSI Control	22:20	0h	MSI control field
Reserved	31:23	00h	Reserved

MSI Address – RW - 32 bits - [PCI_Reg:D4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0		Reserved. Read-only.
MSI Address	31:2	0h	System-specified message address.

MSI Data – RW - 16 bits - [PCI_Reg:D8h]			
Field Name	**Bits**	**Default**	**Description**
MSI Data	15:0	0h	System-specified message.

2.2.4 USB1/USB2/USB4 (Device-18/19, func-0 & Device-20, func-5) OHCI Memory Mapped Registers

Register Name	Offset Address
HcRevision	0h
HcControl	4h
HcCommandStatus	8h
HcInterruptStatus	Ch
HcInterruptEnable	10h
HcInterruptDisable	14h
HcHCCA	18h
HcPeriodCurrentED	1Ch
HcControlHeadED	20h
HcControlCurrentED	24h
HcBulkHeadED	28h
HcBulkCurrentED	2Ch
HcDoneHead	30h
HcFmInterval	34h
HcFmRemaining	38h
HcFmNumber	3Ch
HcPeriodicStart	40h
HcLSThreshold	44h
HcRhDescriptorA	48h
HcRhDescriptorB	4Ch
HCRhStatus	50h
HcRhPortStatus[1]	54h
…	…
HcRhPortStatus[NDP]	54+4*NDP
OHCI Loop Back feature Support	F0h

HcRevision - R - 32 bits - [MEM_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
REV	7:0	10h	**Revision** This read-only field contains the version of HCI specification.
L	8	1b	**Legacy** This read-only field is 1, indicating that the legacy support registers are present in this HC.
Reserved	31:9		

HcControl - 32 bits - [MEM_Reg:04h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
CBSR	1:0	00b	RW	R	**ControlBulkServiceRatio** This specifies the service ratio between Control and Bulk Eds. Before processing any of the non-periodic lists, HC must compare the ratio specified with its internal count on how many non-empty Control Eds have been processed, in order to determine whether to continue serving another Control ED or switching to Bulk Eds. **Setting** **Service Ratio** 0 1:1 1 2:1 2 3:1 3 4.1
PLE	2	0b	RW	R	**PeriodicListEnable** This bit is set to enable the processing of the periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
IE	3	0b	RW	R	**IsochronousEnable** This bit is used by HCD to enable/disable processing of isochronous Eds. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
CLE	4	0b	RW	R	**ControlListEnable** This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.
BLE	5	0b	RW	R	**BulkListEnable** This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.

HcControl - 32 bits - [MEM_Reg:04h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
HCFS	7:6	00b	RW	RW	**HostControllerFunctionalState** for USB 00b: USBRESET 01b: USBRESUME 10b: USBOPERATIONAL 11b: USBSUSPEND A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartofFrame field of HcInterruptStatus. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
IR	8	0b	RW	R	**InterruptRouting** This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If cleared, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
RWC	9	0b	RW	RW	**RemoteWakeupConnected** This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system it is the responsibility of system firmware to set this bit during POST. HC clears the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.
RWE	10	0b	RW	R	**RemoteWakeupEnable** This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
Reserved	31:11				

HcCommandStatus - 32 bits - [MEM_Reg:08h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
HCR	0	0b	RW	RW	**HostControllerReset** This bit is set by HCD to initiate a software reset of HC.Regardless of the functional state of HC, it moves to the USBSUSPEND state in which most of the operational registers are reset except those stated otherwise; e.g., the InterruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub, and no subsequent reset signaling should be asserted to its downstream ports.
CLF	1	0b	RW	RW	**ControlListFilled** This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1, causing Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
BLF	2	0b	RW	RW	**BulkListFilled** This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1, causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
OCR	3	0b	RW	RW	**OwnershipChangeRequest** This bit is set by an OS HCD to request a change of control of the HC. When set, HC will set the OwnershipChange field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
Reserved	15:4				

HcCommandStatus - 32 bits - [MEM_Reg:08h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
SOC	17:16	00b	R	RW	**SchedulingOverrunCount** These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problems.
Reserved	31:18				

HcInterruptStatus RW - 32 bits - [MEM_Reg:0Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
SO	0	0b	RW	RW	**SchedulingOverrun** This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.
WDH	1	0b	RW	RW	**WritebackDoneHead** This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
SF	2	0b	RW	RW	**StartofFrame** This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
RD	3	0b	RW	RW	**ResumeDetected** This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRESUME state.
UE	4	0b	RW	RW	**UnrecoverableError** This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing or signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
FNO	5	0b	RW	RW	**FrameNumberOverflow** This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.
RHSC	6	0b	RW	RW	**RootHubStatusChange** This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus [NumberofDownstreamPort] has changed.
Reserved	29:7				

HcInterruptStatus RW - 32 bits - [MEM_Reg:0Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
OC	30	0b	RW	RW	**OwnershipChange** This bit is set by HC when HCD sets the OwnershipChangeRequest field in HcCommandStatus. This event, when unmasked, will always generate a System Management Interrupt (SMI) immediately. This bit is tied to 0b when the SMI pin is not implemented.
Reserved	31				

HcInterruptEnable- 32 bits - [MEM_Reg:10h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
SO	0	0b	RW	RW	**SchedulingOverrun** 0: Ignore 1: Enable interrupt generation due to Scheduling Overrun.
WDH	1	0b	RW	RW	**HcDoneHeadWriteback** 0: Ignore 1: Enable interrupt generation due to HcDoneHead Writeback.
SF	2	0b	RW	RW	**StartofFrame** 0: Ignore 1: Enable interrupt generation due to Start of Frame.
RD	3	0b	RW	W	**ResumeDetect** 0: Ignore 1: Enable interrupt generation due to Resume Detect.
UE	4	0b	RW	RW	**UnrecoverableError** 0: Ignore 1: Enable interrupt generation due to Unrecoverable Error.
FNO	5	0b	RW	RW	**FrameNumberOverflow** 0: Ignore 1: Enable interrupt generation due to Frame Number Overflow.
RHSC	6	0b	RW	RW	**RootHubStatusChange** 0: Ignore 1: Enable interrupt generation due to Root Hub Status Change.
Reserved	29:7				
OC	30	0b	RW	RW	**OwnershipChange** 0: Ignore 1: Enable interrupt generation due to Ownership Change.
MIE	31	0b	RW	R	**MasterInterruptEnable** A 0 written to this field is ignored by HC. A 1 written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.

HcInterruptDisable - 32 bits - [MEM_Reg:14h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
SO	0	0b	RW	R	**SchedulingOverrun** 0: Ignore 1: Disable interrupt generation due to Scheduling Overrun.
WDH	1	0b	RW	R	**HcDoneHeadWriteback** 0: Ignore 1: Disable interrupt generation due to HcDoneHead Writeback.
SF	2	0b	RW	R	**StartofFrame** 0: Ignore 1: Disable interrupt generation due to Start of Frame.
RD	3	0b	RW	R	**ResumeDetect** 0: Ignore 1: Disable interrupt generation due to Resume Detect.
UE	4	0b	RW	R	**UnrecoverableError** 0: Ignore 1: Disable interrupt generation due to Unrecoverable Error.
FNO	5	0b	RW	R	**FrameNumberOverflow** 0: Ignore 1: Disable interrupt generation due to Frame Number Overflow.
RHSC	6	0b	RW	R	**RootHubStatusChange** 0: Ignore 1: Disable interrupt generation due to Root Hub Status Change.
Reserved	29:7				
OC	30	0b	RW	R	**OwnershipChange** 0: Ignore 1: Disable interrupt generation due to Ownership Change.
MIE	31	0b	RW	R	**MasterInterruptEnable** A 0 written to this field is ignored by HC. A 1 written to this field disables interrupt generation due to events specified in the other bits of this register. This field is set after a hardware or software reset.

HcHCCA - 32 bits - [MEM_Reg:18h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	7:0				
HCCA	31:8	000000h	RW	R	**HostControllerCommunicationArea** This is the base address of the Host Controller Communication Area

HcPeriodCurrentED - 32 bits - [MEM_Reg:1Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
PCED	31:4	0000000h	R	RW	**PeriodCurrentED** This is used by HC to point to the head of one of the Periodic lists which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.

HcControlHeadED- 32 bits - [MEM_Reg:20h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
CHED	31:4	0000000h	RW	R	**ControlHeadED** HC traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.

HcControlCurrentED RW - 32 bits - [MEM_Reg:24h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
CCED	31:4	0000000h	RW	RW	**ControlCurrentED** This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks ControlListFilled in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to 0 to indicate the end of the Control list.

HcBulkHeadED - 32 bits - [MEM_Reg:28h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
BHED	31:4	0b	RW	R	**BulkHeadED** HC traverses the Bulk list starting with the HcBulkHeadED pointer.The content is loaded from HCCA during the initialization of HC.

HcBulkCurrentED- RW - 32 bits - [MEM_Reg:2Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
BCED	31:4	0000000h	RW	RW	**BulkCurrentED** This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to 0 to indicate the end of the Bulk list.

HcDoneHead- 32 bits - [MEM_Reg:30h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
DH	31:4	0b	R	RW	**DoneHead** When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to 0 whenever HC writes the content of this register to HCCA. It also sets WritebackDoneHead of HcInterruptStatus.

HcFmInterval - 32 bits - [MEM_Reg:34h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
FI	13:0	2EDFh	RW	R	**FrameInterval** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.
Reserved	15:14				
FSMPS	30:16	0000h	RW	R	**FSLargestDataPacket** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
FIT	31	0b	RW	R	**FrameIntervalToggle** HCD toggles this bit whenever it loads a new value to FrameInterval

HcFmRemaining - 32 bits - [MEM_Reg:38h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
FR	13:0	0000h	R	RW	**FrameRemaining** This counter is decremented at each bit time. When it reaches 0, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval field of HcFmInterval and uses the updated value from the next SOF.
Reserved	30:14				
FRT	31	0b	R	RW	**FrameRemainingToggle** This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.

HcFmNumber - 32 bits - [MEM_Reg:3Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
FN	15:0	0000h	R	RW	**FrameNumber.** This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after FFFFh. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set StartofFrame in HcInterruptStatus.
Reserved	31:16				

HcPeriodicStart - 32 bits - [MEM_Reg:40h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
PS	13:0	0000h	RW	R	**PeriodicStart** After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.
Reserved	31:14				

HcLSThreshold - 32 bits - [MEM_Reg:44h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
LST	11:0	0628h	RW	R	**LSThreshold** This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining is equal or greater than ?this field. The value is calculated by HCD with the consideration of transmission and setup overhead.
Reserved	31:12				

HcRhDescriptorA- 32 bits - [MEM_Reg:48h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
NDP	7:0	05h/02h*	R	R	**NumberDownstreamPorts** These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OpenHCI is 15. * Note: For USB1/USB2 (device-18/19, func-0), each OHCI controller owns 5 downstream ports. For USB4 (device-20, func-5), the stand-alone OHCI controller owns 2 downstream ports.
PSM	8	1b	RW	R	**PowerSwitchingMode** This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0: All ports are powered at the same time. 1: Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands **(**Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch **(**Set/ClearGlobalPower).
NPS	9	1b	RW	R	**NoPowerSwitching** These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0: Ports are power switched. 1: Ports are always powered on when the HC is powered on.
DT	10	0b	R	R	**DeviceType** This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.

HcRhDescriptorA- 32 bits - [MEM_Reg:48h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
OCPM	11	1b	RW	R	**OverCurrentProtectionMode** This field describes how the overcurrent status for the Root Hub ports are reported. At reset, this field should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0: Over-current status is reported collectively for all downstream ports. 1: Over-current status is reported on a per-port basis.
NOCP	12	0b	RW	R	**NoOverCurrentProtection** This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0: Overcurrent status is reported collectively for all downstream ports 1: No overcurrent protection supported
Reserved	23:13				
POTPGT	31:24	02h	RW	R	**PowerOnToPowerGoodTime** This field specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2 ms.

HcRhDescriptorB- 32 bits - [MEM_Reg:4Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
DR	15:0	0000h	RW	R	**DeviceRemovable** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit [0]: Reserved Bit [1]: Device attached to Port #1 Bit [2]: Device attached to Port #2 ... Bit [15]: Device attached to Port #15
PPCM	31:16	0000h	RW	R	**PortPowerControlMask** Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode=0), this field is not valid. Bit [0]: Reserved Bit [1]: Ganged-power mask on Port #1 Bit [2]: Ganged-power mask on Port #2 ... Bit [15]: Ganged-power mask on Port #15

HcRhStatus- 32 bits - [MEM_Reg:50h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
LPS	0	0b	RW	R	(Read) **LocalPowerStatus** The Root Hub does not support the local power status feature; thus, this bit is always read as 0. (Write) **ClearGlobalPower** In global power mode (PowerSwitchingMode=0), This bit is written to 1 to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a 0 has no effect.
OCI	1	0b	R	RW	**OverCurrentIndicator** This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented, this bit is always 0
Reserved	14:2				
DRWE	15	0b	RW	R	(Read) **DeviceRemoteWakeupEnable** This bit enables the ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0: ConnectStatusChange is not a remote wakeup event. 1: ConnectStatusChange is a remote wakeup event. (Write) **SetRemoteWakeupEnable** 1: Set DeviceRemoveWakeupEnable. 0: Has no effect.
LPSC	16	0b	RW	R	(Read) **LocalPowerStatusChange** The Root Hub does not support the local power status feature; thus, this bit is always read as 0. (Write) **SetGlobalPower** In global power mode (PowerSwitchingMode=0), this bit is written to 1 to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a 0 has no effect.
OCIC	17	0b	RW	RW	**OverCurrentIndicatorChange** This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a 1. Writing a 0 has no effect.
Reserved	30:18				
CRWE	31	-	W	R	(Write) **ClearRemoteWakeupEnable** Writing a 1 clears DeviceRemoveWakeupEnable. Writing a 0 has no effect.

The register *HcRhPortStatus[1 to NDP]* below represents a number of similar registers, starting with HcRhPortStatus1 through to HcRhPortStatus[NDP], where NDP represents the range of number of supported downstream ports.

HcRhPortStatus[1 to NDP] - RW - 32 bits - [MEM_Reg:50+4x(1 to NDP)h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
CCS	0	0b	RW	RW	(Read) **CurrentConnectStatus** This bit reflects the current state of the downstream port. 0: No device connected 1: Device connected (Write) **ClearPortEnable** The HCD writes a 1 to this bit to clear the PortEnableStatus bit. Writing a 0 has no effect. CurrentConnectStatus is not affected by any write. Note: This bit is always read 1b when the attached device is nonremovable (DeviceRemovable[NDP]).
PES	1	0b	RW	RW	(Read) **PortEnableStatus** This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0: Port is disabled 1: Port is enabled (Write) **SetPortEnable** The HCD sets PortEnableStatus by writing a 1. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.

HcRhPortStatus[1 to NDP] - RW - 32 bits - [MEM_Reg:50+4x(1 to NDP)h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
PSS	2	0b	RW	RW	(Read) **PortSuspendStatus** This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0: Port is not suspended 1: Port is suspended (Write) **SetPortSuspend** The HCD sets the PortSuspendStatus bit by writing a 1 to this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets **ConnectStatusChang**e. This informs the driver that it attempted to suspend a disconnected port.
POCI	3	0b	RW	RW	(Read) **PortOverCurrentIndicator** This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal 0: No overcurrent condition. 1: Overcurrent condition detected. (Write) **ClearSuspendStatus** The HCD writes a 1 to initiate a resume. Writing a 0 has no effect. A resume is initiated only if PortSuspendStatus is set.
PRS	4	0b	RW	RW	(Read) **PortResetStatus** When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0: Port reset signal is not active 1: Port reset signal is active (Write) **SetPortReset** The HCD sets the port reset signaling by writing a 1 to this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.

HcRhPortStatus[1 to NDP] - RW - 32 bits - [MEM_Reg:50+4x(1 to NDP)h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	7:5				
PPS	8	0b	RW	RW	(Read) **PortPowerStatus** This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPowerControlMask[NDP]. In global switching mode, (PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset. 0: Port power is off 1: Port power is on (Write) **SetPortPower** The HCD writes a 1 to set the PortPowerStatus bit. Writing a 0 has no effect. Note: This bit is always reads 1b if power switching is not supported.
LSDA	9	X	RW	RW	(read) **LowSpeedDeviceAttached** This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0: Full speed device attached 1: Low speed device attached (write) **ClearPortPower** The HCD clears the PortPowerStatus bit by writing a 1 to this bit. Writing a 0 has no effect.
Reserved	15:10				

HcRhPortStatus[1 to NDP] - RW - 32 bits - [MEM_Reg:50+4x(1 to NDP)h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
CSC	16	0b	RW	RW	**ConnectStatusChange** This bit is set whenever a connect or disconnect event occurs. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0: No change in CurrentConnectStatus 1: Change in CurrentConnectStatus Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
PESC	17	0b	RW	RW	**PortEnableStatusChange** This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0: No change in PortEnableStatus 1: Change in PortEnableStatus
PSSC	18	0b	RW	RW	**PortSuspendStatusChange** This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. This bit is also cleared when ResetStatusChange is set. 0: Resume is not completed 1: Resume completed
OCIC	19	0b	RW	RW	**PortOverCurrentIndicatorChange** This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0: No change in PortOverCurrentIndicator 1: PortOverCurrentIndicator has changed
PRSC	20	0b	RW	RW	**PortResetStatusChange** This bit is set at the end of the 10-ms port reset signal. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0: Port reset is not complete 1: Port reset is complete
Reserved	31:21				

HcLoopBackControl- 32 bits - [MEM_Reg:F0h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
LoopBackTestStart	0	0	RW	R	To start the Loop Back test. Software should set this bit to start the loop back test and should clear this bit to clear out all the test status before starting the next loop.
Reserved	3:1				
PortUnderTest	7:4	0	RW	R	Port Under Test. Software selects the port under test through these bits. Software should only program the port number to the range of # of ports that OHCI supports. 0000: port-0 0001: port-1 0010: port-2 ... and so on.
LoopBackTestData	15:8	0	RW	R	1-byte test data pattern for transmit and receive logic check the received data to match with this data pattern.
	30:16				
LoopBackTestDone	31	0	R	W	Read-only. Host Controller sets the bit when loop back is done. The bit is cleared when software clears the "LoopBackTestStart" bit.

OHCI LOOPBACK Feature Support Register. This register is not accessible when the OHCI PCI_Reg x52[8] is set to "0".

2.2.4.1 Legacy Support Registers

Four operational registers are used to provide legacy support. Each of these registers is located on a 32-bit boundary. The offset of these registers is relative to the base address of the Host Controller operational registers with HceControl located at offset 100h.

Offset	Register	Description
100h	HceControl	Used to enable and control the emulation hardware and report various status information.
104h	HceInput	Emulation side of the legacy Input Buffer register.
108h	HceOutput	Emulation side of the legacy Output Buffer register where keyboard and mouse data are to be written by software.
10Ch	HceStatus	Emulation side of the legacy Status register.

2.2.4.1.1 Emulated Registers

Three of the operational registers (HceStatus, HceInput, HceOutput) are accessible at I/O address 60h and 64h when emulation is enabled. Reads and writes to the registers using I/O addresses have side effects as outlined in the table below.

I/O Address	Cycle Type	Register Contents Accessed/Modified	Side Effects
60h	IN	HceOutput	IN from port 60h will set OutputFull in HceStatus to 0
60h	OUT	HceInput	OUT to port 60h will set InputFull to 1 and CmdData to 0 in HceStatus.
64h	IN	HceStatus	IN from port 64h returns current value of HceStatus with no other side effect.
64h	OUT	HceInput	OUT to port 64h will set InputFull to 0 and CmdData in HceStatus to 1.

HceInput –RW - 32 bits			
Field Name	**Bits**	**Default**	**Description**
InputData	7:0	00h	This register holds data that is written to I/O ports 60h and 64h.
Reserved	31:8		
I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the Host Controller's operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.			

HceOutput –RW - 32 bits			
Field Name	**Bits**	**Default**	**Description**
OutputData	7:0	00h	This register hosts data that is returned when an I/O read of port 60h is performed by application software.
Reserved	31:8		
The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.			

HceStatus –RW - 32 bits			
Field Name	**Bits**	**Default**	**Description**
OutputFull	0	0b	The HC sets this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists.
InputFull	1	0b	Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
Flag	2	0b	Nominally used as a system flag by software to indicate a warm or cold boot.
CmdData	3	0b	The HC sets this bit to 0 on an I/O write to port 60h and to 1 on an I/O write to port 64h.
Inhibit Switch	4	0b	This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
AuxOutputFull	5	0b	IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.
Time-out	6	0b	Used to indicate a time-out
Parity	7	0b	Indicates parity error on keyboard/mouse data.
Reserved	31:8		
The contents of the HceStatus Register are returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Accessing this register through its memory address produces no side effects.			

HceControl - 32 bits			
Field Name	**Bits**	**Reset**	**Description**
EmulationEnable	0	0b	When set to 1, the HC is enabled for legacy emulation. The HC decodes accesses to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generate s an emulation interrupt at appropriate times to invoke the emulation software.
EmulationInterrupt	1	-	Read-only. This bit is a static decode of the emulation interrupt condition.
CharacterPending	2	0b	When set, an emulation interrupt is generated when the OutputFull bit of the HceStatus register is set to 0.
IRQEn	3	0b	When set, the HC generates IRQ1 or IRQ12 as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, then IRQ1 is generated; if it is 1, then an IRQ12 is generated.
ExternalIRQEn	4	0b	When set to 1, IRQ1 and IRQ12 from the keyboard controller causes an emulation interrupt. The function controlled by this bit is independent of the setting of the EmulationEnable bit in this register.
GateA20Sequence	5	0b	Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.
IRQ1Active	6	0b	Indicates that a positive transition on IRQ1 from the keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
IRQ12Active	7	0b	Indicates that a positive transition on IRQ12 from the keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
A20State	8	0b	Indicates current state of Gate A20 on keyboard controller. Used to compare against value written to 60h when GateA20Sequence is active.
Reserved	31:9	-	Must read as 0s.

2.2.5 USB1/USB2 (Device-18/19, func-2) EHCI PCI Configuration Registers

Registers Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID / Class Code	08h
Miscellaneous	0Ch
Base Address – BAR_EHCI	10h
Subsystem ID / Subsystem Vendor ID	2Ch
Capability Pointer	34h
Interrupt Line	3Ch
EHCI Misc Control	50h
EHCI PCI Spare 1	54h
Serial Bus Release Number – SBRN	60h
Frame Length Adjustment – FLADJ	61h
	62h
PME Control	C0h
PME Data / Status	C4h
MSI Control	D0h
MSI Address	D4h
MSI Data	D8h
EHCI Debug Port Support	E4h
Function Level Reset Capability	F0h

Registers Name	Offset Address
Function Level Reset Control	F4h
USB Legacy Support Extended Capability – USBLEGSUP	EECP+0h*
USB Legacy Support Control/Status - USBLEGCTLSTS	EECP+4h*
*The EECP field is in the read-only HCCPARAMS register [MEM_Reg: 08h] with the value of A0h.	

Vendor ID – R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Vendor Identifier. The vendor ID is 0x1022.

Device ID – R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	Function 0: 7808h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device.

Command – RW - 16 bits - [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Space Accesses	0	0b	0: Disable the device response. 1: Allow the device to respond to I/O Space accesses.
Memory Space Accesses	1	0b	0: Disable the device response. 1: Allow the device to respond to Memory Space accesses.
Bus Master	2	0b	0: Disable the device from generating PCI accesses. 1: Allow the device to behave as a bus master.
Special Cycle	3	0b	Hard-wired to 0, indicating no Special Cycle support.
Memory Write and Invalidate Command	4	0b	0: Memory Write must be used. 1: Masters may generate the command.
VGA Palette Register Accesses	5	0b	Hard-wired to 0, indicating the device should treat palette write accesses like all other accesses.
Parity Enable	6	0b	0: the device sets its Detected Parity Error status bit (bit [15] in the Status register) when an error is detected, but continues normal operations without asserting PERR#. 1: The device must take its normal action when a parity error is detected.
Reserved	7	0b	Hard-wired to 0 per PCI2.3 spec.
SERR# Enable	8	0b	0: Disable the SERR# driver. 1: Enable the SERR# driver. Note: Address parity errors are reported only if this bit and bit [6] are 1.
Fast Back-to-Back Enable	9	0b	0: Only fast back-to-back transactions to the same agent are allowed. 1: The master is allowed to generate fast back-to-back transactions to different agents.
Interrupt Disable	10	0b	0: Enable the assertion of the device/function's INTx# signal. 1: Disable the assertion of the device/function's INTx# signal.
Reserved	15:11		Reserved

Status – R - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0		Reserved
Interrupt Status	3	0b	This bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
Capabilities List	4	1b	0: Indicates that no New Capabilities linked list is available. 1: Indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
66 MHz Capable	5	1b	Hard-wired to 1, indicating 66MHz capable.
Reserved	6		Reserved
Fast Back-to-Back Capable	7	1b	Hard-wired to 1, indicating Fast Back-to-Back capable.
Master Data Parity Error	8	0b	This bit is set when any of the following three conditions is met: (1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); (2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit (Command register) is set.
DEVSEL timing	10:9	01b	Hard-wired to 01b – medium timing
Signaled Target Abort	11	0b	This bit is set by a target device whenever it terminates a transaction with Target-Abort.
Received Target Abort	12	0b	This bit is set by a master device whenever its transaction is terminated with Target-Abort.
Received Master Abort	13	0b	This bit is set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort.
Signaled System Error	14	0b	This bit is set whenever the device asserts SERR#.
Detected Parity Error	15	0b	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).

Revision ID / Class Code – R - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	11h	Revision ID. The value 11h indicates the reversion A11.
PI	15:8	20h	Programming Interface. A constant value of '20h' identifies the device being an EHCI Host Controller.
SC	23:16	03h	Sub Class. A constant value of '03h' identifies the device being of Universal Serial Bus.
BC	31:24	0Ch	Base Class. A constant value of '0Ch' identifies the device being a Serial Bus Controller.

Miscellaneous – RW - 32 bits - [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This read/write field specifies the system cache line size in units of DWORDs and must be initialized to 00h.
Latency Timer	15:8	00h	Bits[9:8] are hard-wired to 00b, resulting in a timer granularity of at least four clocks. This field specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.
Header Type	23:16	00h	Read-only. This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space) and also whether or not the device contains multiple functions. EHCI has single function and bits[23:16] are hard-wired to 00h.
BIST	31:24	00h	Hard-wired to 00h, indicating no build-in BIST support.

BAR_EHCI – RW - 32 bits - [PCI_Reg : 10h]			
Field Name	**Bits**	**Default**	**Description**
IND	0	0b	Indicator. Read-only. A constant value of 0 indicates that the operational registers of the device are mapped into memory space of the main memory of the PC host system.
TP	2:1	0h	Type. Read-only. A constant value of 00b indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space; i.e., lower 4 GB of the main memory of the PC host.
PM	3	0b	Prefetch Memory. A constant value of 0 indicates that there is no support for “prefetchable memory”. Read-only.
Reserved	7:4	0h	Read-only.
BA	31:8	0h	Base Address. Corresponds to memory address signals [31:8].

BAR register. Base address used for the memory mapped capability and operational registers.

Subsystem ID / Subsystem Vendor ID – RW - 32 bits - [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	1022	Can only be written once by software.
Subsystem ID	31:16	7808	Can only be written once by software.

Capability Pointer – R - 8 bits - [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capability Pointer	7:0	C0h*	Address of the 1st element of capability link.
* If PME Capability is disabled by setting PME Disable bit (PCI Register x50[5]), then Capability Pointer contains MSI Capability Pointer DCh. If MSI Capability is disabled by setting MSI Disable bit (PCI Register x50[6]), then Capability Pointer contains Debug Port Capability Pointer xE4h.			

Interrupt Line - RW - 32 bits - [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	The Interrupt Line is a field used to communicate interrupt line routing information. The register is read/write and must be implemented by any device (or device function) that uses an interrupt pin. POST software will write the routing information into this register as it initializes and configures the system. The value in this field tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value; rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.
Interrupt Pin	15:8	02h	Read-only by default *. Hard-wired to 02h, which corresponds to using INTB#
MIN_GNT	23:16	00h	Read-only. Hard-wired to 00h to indicate no major requirements for the settings of Latency Timers.
MAX_LAT	31:24	00h	Read-only. Hard-wired to 00h to indicate no major requirements for the settings of Latency Timers.
* If Interrupt Backdoor Enable bit (OHCI regx50[7]) is set, this field is writable.			

EHCI Misc Control – RW - 32 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
D3Cold PME support	0	0b	Enable EHCI host controller PME support at D3Cold. 0: Disable 1: Enable
Disable SMI	1	0b	To disable ehci_smi sent to “USB SMI” output (to ACPI). 0: Enable 1: Disable
FLR Enable	2	0b	Set to 1 to enable FLR support.
FLR SMI Enable	3	0b	Set to 1 to enable FLR SMI and to disable HW FLR function. This is the back-door control bit that, in case HW does not behave as expected, disables HW FLR function and enables SMI on FLR to let SW handle the reset sequence. The bit will have effect only if FLR Enable (x50[2]) is set.
Ehci pme level signal by resume-wakeup enable	4	0b	Let pme be a level signal instead of pulse when resume wakeup event is detected. 1: Enable 0: Disable
PME Disable	5	0b	Set to 1 to disable PME support
MSI Disable	6	0b	Set to 1 to disable MSI support
Enable Per-Port Change Events Capability	7	0	Set to 1 to enable the support of Per-Port Change Event Capability 1: Set HCCPARAMS[18] to 1 0: Clear HCCPARAMS[18] to 0
Async Park IN Control	11:8	1h	Async Park Mode Count for IN Packet 0h: Standard count as the value in USBCMD[9:8] 1h: 8 packets 2h ~ Fh: Reserved

EHCI Misc Control – RW - 32 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
Async Park OUT Control	15:12	2h	Async Park Mode Count for OUT Packet 0h: Standard count as the value in USBCMD[9:8] 1h: 8 packets 2h ~ Fh : Reserved
	16	0b	
Async Park Cache Control	17	0b	Set to 1 to enable Async Park Cache Control
Reserved	18		
Reserved	20	0b	Reserved.
Enable IP Gap Fix	21	0b	The bit may be cleaned up after validation. Set to 1 to enable IP gap protection on starting a new transaction.
	22	0b	
AsyncPark Disable	23	0b	Set to 1 to disable async-park mode.
Async QH Cache Threshold Control	24	0b	For OUT: 0: Cache only if packet size is greater than 128 Bytes. 1: Cache only if packet size is greater than 64 Bytes. For IN: 0: Cache only if expected packet size is greater than 192 Bytes. 1: Cache only if expected packet size is greater than 96 Bytes.
Disable Async QH Cache	25	0b	Set to 1 to disable async QH/QTD cache.
Disable Async Data Cache	26	0b	Set to 1 to disable async data cache request.
Disable Periodic List Cache	27	0b	Set to 1 to disable periodic list cache.
Disable Async QH Cache Enhancement	28	0b	Set to 1 to disable async QH/QTD cache enhancement.
PHY Advance Power Saving Enable	31	1b	Set to 1 to enable the advance PHY power saving feature to save active power from USBPHY.
This register is shared among all the EHCI controllers if the Share Register Enable bit (OHCI_Pci_config x52[12]) is set.			

EHCI Spare 1 – RW - 32 bits - [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	**Description**
EHCI Delay BIF L1 Enable	0	0b	Set to 1 to enable EHCI delaying BIF on entering L1 when there are USB transactions on the controller and when USB delaying BIF L1 is enabled in AB (see AB BIF Control 0 in section 8.4).
	1	0b	
EHCI Block-C-State Enable	2	0b	Set to 1 to enable EHCI sending block-C-state signal to ACPI (A12 or later).
EHCI Empty List Mode	3	0b	EHCI Empty List Mode 0: Disable 1: Enable
LS Connection Wake up Enable	4	0b	Enable wake up from LS connection 0: Disable 1: Enable
EHCI L1 Early Exit Enable	5	0b	EHCI L1 Early Exit Enable 0: Disable 1: Enable

EHCI Spare 1 – RW - 32 bits - [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	**Description**
EHCI L1 Early Exit Mode	6	0b	Mode selection bit for EHCI L1 early exit function. 0: Exit signal active in every uframe if pdc schedule is enabled. 1: Exit signal active in current uframe when detecting next uframe has active pdc work.
EHCI L1 Early Exit Timer	9:7	101b	Timer to control EHCI L1 exit. When EHCI L1 Early Exit Enable is set to 1, this field selects the amount of time before SOF that the EHCI controller will request UMI to exit from L1. 000: 20 micro seconds 001: 30 micro seconds 010: 40 micro seconds 011: 50 micro seconds 100: 60 micro seconds 101: 70 micro seconds 110: 80 micro seconds 111: 90 micro seconds
Resume_PME_D123_En	10	0b	Resume PME in D123 Enable When set, PME Status will be set only in non-D0 state when resume occurs. 0: Disable 1: Enable
PDC Start Fix Enable	11	0b	Enable fix on PDC start with run/stop set. 0: Disable 1: Enable
hshk_rdy fix enable	12	0b	Enable fix on hshk_rdy (hshk_rdy should always be a pulse but handling of hshk_rdy under overrun in incorrect) 0: Disable 1: Enable
Framelist read fix enable	13	0b	Enable fix on delayed framelist reads causing EHCI to access memory address 0. 0: Disable 1: Enable
Reserved	14	0b	
FirstTransfer fix enable	15	0b	Enable 2nd fix on delayed Framelist reads causing EHCI to mis-behave. 0: Disable (default) 1: Enable
BLMBufferFlush fix enable	16	0b	Enable BLM buffer flush on IOC. 0: Disable (default) 1: Enable
DataCacheStop enable	17	0b	Enable async data cache stop on page-cross. 0: Disable (default) 1: Enable
XverSelect fix enable	18	0b	Enable fix on combo signal from 60MHz used directly in 480MHz. 0: Disable (default) 1: Enable
Fm_babble_fix_en	19	0b	Enable fix for frame babble on one port causes other ports also detect babble issue. 0: Disable 1: Enable
DataCacheEnhance	20	0b	Set to 1 to enable async data prefetch enhancement. 0: Disable (default) 1: Enable

EHCI Spare 1 – RW - 32 bits - [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	**Description**
NoTimeToFetchFlist fix enable	21	0b	Enable fix on no time to fetch Framelist issue. 0: Disable (default) 1: Enable
HaltedBit fix enable	22	0b	Enable fix on halted but handling issue. 0: Disable (default) 1: Enable
Reserved	23	0h	
SPT_SPEED_FIX_EN	24	0b	Enable fix on "S" bit in split token 0: Disable(default) 1: Enable
CONNECT_DET_TIMER_RST_EN	25	0b	Enable fix on connect_det timer. 0: disable the fix, we will reset the timer after prt_clr_con_sts_r have been asserted 1: enable the fix, we should reset the timer when prt_clr_con_sts_r is asserted
Reserved	26	0b	
EHCI_PME_EN	27	0b	USB PME qualified by the PME enable bits 0: USB PME not qualified by the PME enable bits 1: USB PME qualified by the PME enable bits
Async_Act_Qh_Delink_En	28	0b	Enable fix for EHCI support de-linking async active QH 0: EHCI don't support de-linking async active QH 1: EHCI support de-linking async active QH
Enable EHCI QTD with SOF	29	0b	Enable fix on EHCI QTD missing SOF 0: Disable 1:Enable
EHCI Resume Timer Mode	30	0b	EHCI Resume Timer Mode 0: Disable (default) 1: Enable
Reserved	31	0h	Reserved
This register is shared among all the EHCI controllers if the Share Register Enable bit (OHCI_Pci_config x52[12]) is set.			

SBRN – R - 8 bits - [PCI_Reg:60h]			
Field Name	**Bits**	**Default**	**Description**
SBRN	7:0	20h	**Serial Bus Release Number** Hard-wired to 20h.

FLADJ – RW - 8 bits - [PCI_Reg:61h]			
Field Name	**Bits**	**Default**	**Description**
FLADJ	5:0	20h	**Frame Length Timing Value** Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000.
Reserved	7:6		Reserved.

FLADJ Value in decimals [hexadecimal value]	Frame Length (# High Speed bit times in decimals)
0 [00h]	59488
1 [01h]	59504
2 [02h]	59520
...	...
31 [1Fh]	59984
32 [20h]	60000
...	...
62 [3Eh]	60480
63 [3Fh]	60496

PME Control – RW - 32 bits - [PCI_Reg:C0h]			
Field Name	**Bits**	**Default**	**Description**
Cap_ID	7:0	01h	Read-only. A value of 01h identifies the linked list items as being the PCI Power Management registers.
Next ItemPointer	15:8	D0h	Read-only. This field provides an offset into the function's PCI Configuration Space, pointing to the location of next item in the function's capability list. If there are no additional items in the Capabilities List, this register is set to 00h.
Version	18:16	010b	Read-only. A value of 010b indicates that this function complies with Revision 1.1 of the PCI Power Management Interface Specification.
PME clock	19	0b	Read-only. When this bit is a 0, it indicates that no PCI clock is required for the function to generate PME#.
Reserved	20		Reserved
DSI	21	0b	Read-only. This Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it.

PME Control – RW - 32 bits - [PCI_Reg:C0h]			
Field Name	**Bits**	**Default**	**Description**
Aux_Current	24:22	000b	Read-only. This 3 bit field reports the 3.3V auxiliary current requirements for the PCI function. If the Data Register has been implemented by this function, then: - Reads of this field must return a value of 000b. - The Data Register takes precedence over this field for 3.3V auxiliary current requirement reporting.?
D1_Support	25	1b	If this bit is a 1, this function supports the D1 Power Management State.
D2_Support	26	1b	If this bit is a 1, this function supports the D2 Power Management State.
PME_Support	31:27	0Fh	Read-only. This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit [31] 1XXXXb - PME# can be asserted from D3cold Bit [30] X1XXXb - PME# can be asserted from $D3_{hot}$ Bit [29] XX1XXb - PME# can be asserted from D2 Bit [28] XXX1Xb - PME# can be asserted from D1 Bit [27] XXXX1b - PME# can be asserted from D0

PME Data / Status – RW - 32 bits - [PCI_Reg:C4h]			
Field Name	**Bits**	**Default**	**Description**
PowerState	1:0	00b	This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given by: 00b: D0 01b: D1 10b: D2 11b: $D3_{hot}$ If software attempts to write an unsupported, optional state to this field, the write operation must be completed normally on the bus; however, the data is discarded and no state change occurs.
Reserved	7:2		Reserved
PME_En	8	0b	A 1 enables the function to assert PME#. When 0, PME# assertion is disabled. This bit defaults to 0 if the function does not support PME# generation from $D3_{cold}$.
Data_Select	12:9	0000b	This 4-bit field is used to select which data is to be reported through the Data register and Data_Scale field.
Data_Scale	14:13	00b	Read-only. Indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field will vary depending on which data value has been selected by the Data_Select field.
PME_Status	15	0b	This bit is set when the function would normally assert the PME# signal independent of the state of the PME_ En bit.
Reserved	21:16		Reserved

PME Data / Status – RW - 32 bits - [PCI_Reg:C4h]			
Field Name	**Bits**	**Default**	**Description**
B2_B3#	22	1b	Read-only. The state of this bit determines the action that is to occur as a direct result of programming the function to $D3_{hot}$. A 1 indicates that when the bridge function is programmed to $D3_{hot}$, its secondary bus's PCI clock will be stopped (B2).
BPCC_En	23	0b	Read-only. A 0 indicates that the bus power/clock control policies are disabled. When the Bus Power/Clock Control mechanism is disabled, the bridge's PMCSR PowerState field cannot be used by the system software to control the power or clock of the bridge's secondary bus.
Data	31:24	00h	Read-only. This field is used to report the state dependent data requested by the Data_Select field. The value of this field is scaled by the value reported by the Data_Scale field.

MSI Control – RW - 32 bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
MSI USB	7:0	05h	MSI USB ID. Read-only.
Next Item Pointer	15:8	E4h	Pointer to next capability structure.
MSI Control Out	16	0b	Set to 1 to disable IRQ. Use MSI instead.
Reserved	19:17	0h	Reserved
MSI Control	22:20	0h	MSI control field.
64-bit Address Capable	23	0b	Read-only. If EHCI is in 64-bit address mode, as specified by 64-bit Addressing Capability bit in HCCPARAMS [MEM Reg:08h], then this bit is set to 1 indicating that EHCI is capable of generating a 64-bit message address; otherwise, it is set to 0 indicating the EHCI is not capable of generating a 64-bit address.
Reserved	31:24	00h	Reserved

MSI Address – RW - 32 bits - [PCI_Reg : D4h]			
Field Name	**Bits**	**Default**	**Description**
MSI Address	31:0	0h	System-specified message address.

MSI Upper Address – RW - 32 bits - [PCI_Reg:D8h]			
Field Name	**Bits**	**Default**	**Description**
MSI Upper Address *	31:0	0h	If the Message Enable bit (bit 0 of the Message Control register) is set, the contents of this register (if non-zero) specify the upper 32-bits of a 64-bit message address (AD[63:32]). If the contents of this register are zero, the device uses the 32-bit address specified by the message address register.
* If EHCI is in 64-bit address mode, as specified by 64-bit Addressing Capability bit in HCCPARAMS [MEM Reg:08h], then xD8 contains the higher 32 bits of the MSI Address and xDC contains the MSI Data; otherwise, xD8 contains MSI Data.			

MSI Data – RW - 16 bits - [PCI_Reg:D8h/DCh]			
Field Name	**Bits**	**Default**	**Description**
MSI Data *	15:0	0h	System-specified message
* If EHCI is in 64-bit address mode, as specified by 64-bit Addressing Capability bit in HCCPARAMS [MEM Reg:08h], then xD8 contains the higher 32 bits of the MSI Address and xDC contains the MSI Data; otherwise xD8 contains MSI Data.			

Function Level Reset Capability – R - 32 bits - [PCI_Reg:F0h]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	13h	Read-only. The value of 13h in this field identifies that the function is AF capable.
Next Item Pointer	15:8	00h	Read-only. Pointer to next capability structure. This is the final item on the list.
Length	23:16	06h	Read-only. AF structure length (byte).
Transaction Pending capability	24	1b	Read-only. Transaction pending support.
Function Level Reset Capability	25	1b	Read-only. Function level reset support.
Reserved	31:26		
Note: This register is hidden if the FLR Enable bit (EHCI_pci_config x50[7]) is disabled.			

Function Level Reset Control – RW - 32 bits - [PCI_Reg:F4h]			
Field Name	**Bits**	**Default**	**Description**
Initiate FLR	0	0b	A write of 1b initiates Function Level Reset (FLR). The value read by software from this bit shall always be 0b.
Reserved	7:1		
Transaction Pending	8	0b	Read-only. A value of 1b indicates that the Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. A value of 0b indicates that all non-posted transactions have been completed.
Reserved	31:9		
Note: This register is hidden if the FLR Enable bit (EHCI_pci_config x50[7]) is disabled.			

USBLEGSUP – RW - 32 bits - [PCI_Reg:EECP+00h] *			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	01h	Read-only. This field identifies the extended capability. A value of 01h identifies the capability as Legacy Support. This extended capability requires one additional 32-bit register for control/status information, and this register is located at offset EECP+04h.
Next EHCI Extended Capability Pointer	15:8	00h	Read-only. This field points to the PCI configuration space offset of the next extended capability pointer. A value of 00h indicates the end of the extended capability list.
HC BIOS Owned Semaphore	16	0b	The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will set this bit to a 0 in response to a request for ownership of the EHCI controller by system software.
Reserved	23:17		These bits are reserved and must be set to 0.
HC OS Owned Semaphore	24	0b	System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as 0.
Reserved	31:25		These bits are reserved and must be set to 0.
* EECP is defined in HCCPARAMS[15:8] (EHCI MEM x08) and is hard-wired to xA0.			

USBLEGCTLSTS – RW - 32 bits - [PCI_Reg:EECP+04h] *			
Field Name	**Bits**	**Default**	**Description**
USB SMI Enable	0	0b	When this bit is a 1, and the SMI on USB Complete bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on USB Error Enable	1	0b	When this bit is a 1, and the SMI on USB Error bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on Port Change Enable	2	0b	When this bit is a 1, and the SMI on Port Change Detect bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on Frame List Rollover Enable ?R/W	3	0b	When this bit is a 1, and the SMI on Frame List Rollover bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on Host System Error Enable	4	0b	When this bit is a 1, and the SMI on Host System Error bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on Async Advance Enable	5	0b	When this bit is a 1, and the SMI on Async Advance bit in this register is a 1, the host controller will issue an SMI immediately.
Reserved.	12:6		These bits are reserved and must be set to 0.
SMI on OS Ownership Enable	13	0b	When this bit is a 1 and the SMI on OS Ownership Change bit in this register is 1, the host controller will issue an SMI.
SMI on PCI Command Enable	14	0b	When this bit is 1 and SMI on PCI Command in this register is 1, then the host controller will issue an SMI.
SMI on BAR Enable	15	0b	When this bit is 1 and SMI on BAR is 1, then the host controller will issue an SMI.
SMI on USB Complete	16	0b	Shadow bit of USB Interrupt (USBINT) bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the USB Interrupt bit in the USBSTS register. Read-only.

USBLEGCTLSTS – RW - 32 bits - [PCI_Reg:EECP+04h] *			
Field Name	**Bits**	**Default**	**Description**
SMI on USB Error	17	0b	Read-only. Shadow bit of USB Error Interrupt (USBERRINT) bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the USB Error Interrupt bit in the USBSTS register..
SMI on Port Change Detect.	18	0b	Read-only. Shadow bit of Port Change Detect bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the Port Change Detect bit in the USBSTS register.
SMI on Frame List Rollover	19	0b	Read-only. Shadow bit of Frame List Rollover bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the Frame List Rollover bit in the USBSTS register.
SMI on Host System Error	20	0b	Read-only. Shadow bit of Host System Error bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the Host System Error bit in the USBSTS register.
SMI on Async Advance	21	0b	Read-only. Shadow bit of the Interrupt on Async Advance bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the Interrupt on Async Advance bit in the USBSTS register.
Reserved.	28:22		These bits are reserved and must be set to 0.
SMI on OS Ownership Change	29	0b	This bit is set to 1 whenever the HC OS Owned Semaphore bit in the USBLEGSUP register transitions from 1 to 0 or 0 to 1.
SMI on PCI Command	30	0b	This bit is set to 1 whenever the PCI Command Register is written.
SMI on BAR ?R/WC	31	0b	This bit is set to 1 whenever the Base Address Register (BAR) is written.
* Note: EECP is defined in HCCPARAMS[15:8] (EHCI MEM x08) and is hard-wired to xA0.			

2.2.6 USB1/USB2/ (Device-18/19, func-2) EHCI Memory Mapped Registers

2.2.6.1 EHCI Capability Registers

This block of registers is memory-mapped. Access address is equal to the offset address plus the base address defined in BAR[PCI_Reg:10h].

Registers Name	Offset Address
Capability Register Length - CAPLENGTH	00h
Reserved	01h
Host Controller Interface Version – HCIVERSION	02h
Structural Parameters – HCSPARAMS	04h
Capability Parameters - HCCPARMAS	08h
Companion Port Route Description – HCSP-PORTROUTE	0Ch

CAPLENGTH – R - 8 bits - [MEM_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
CAPLENGTH	7:0	20h	This register is used as an offset to add to the register base to find the beginning of the Operational Register Space. Default value = 20h.

HCIVERSION – R - 16 bits - [MEM_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
HCIVERSION	15:0	0100h	This is a two-byte register containing a BCD encoding of the version number of interface to which this host controller interface conforms.

HCSPARAMS – R - 32 bits - [MEM_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
N_PORTS	3:0	5h	This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1H to FH. A 0 in this field is undefined.
Port Power Control (PPC)	4	0b	This field indicates whether the host controller implementation includes port power control. A 1 in this bit indicates the ports have port power switches. A 0 in this bit indicates the port does not have port power switches. The value of this field affects the functionality of the Port Power field in each port status and control register.
Reserved	6:5		These bits are reserved and should be set to 0.
Port Routing Rules	7	0b	This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: 0 = The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. 1 = The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTROUTE array.
Number of Ports per Companion Controller (N_PCC)	11:8	5h	This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, etc. In the previous example, the N_PCC could have been 4, where the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC.
Number of Companion Controller (N_CC)	15:12	1h	This field indicates the number of companion controllers associated with this USB 2.0 host controller. A 0 in this field indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. A value larger than 0 in this field indicates there are companion USB 1.1 host controller(s). Port-ownership hand-offs are supported. High-, Full- and Low-speed devices are supported on the host controller root ports.

HCSPARAMS – R - 32 bits - [MEM_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
Port Indicators (P_INDICATOR)	16	0b	This bit indicates whether the ports support port indicator control. When this bit is a 1, the port status and control registers include a read/writeable field for controlling the state of the port indicator.
Reserved	19:17		These bits are reserved and should be set to 0.
	23:20		
Reserved	31:24		These bits are reserved and should be set to 0.

HCCPARAMS – R - 32 bits - [MEM_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
64-bit Addressing Capability *	0	0b	This field documents the addressing range capability of this implementation. 0: Data structures using 32-bit address memory pointers 1: Data structures using 64-bit address memory pointers
Programmable Frame List Flag	1	1b	If this bit is set to 0, then system software must use a frame list length of 1024 elements with this host controller. The Frame List Size field of the USBCMD register is read-only and should be set to 0. If set to 1, then system software can specify and use a smaller frame list and configure the host controller via the Frame List Size field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
Asynchronous Schedule Park Capability	2	1b	If this bit is set to 1, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
Reserved	3		These bits are reserved and should be set to 0.
Isochronous Scheduling Threshold *	7:4	1h	This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit [7] is 0, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is 1, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
EHCI Extended Capabilities Pointer (EECP)	15:8	A0h	This optional field indicates the existence of a capabilities list. A value of 00h indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain the consistency of the PCI header defined for this class of device.
Hardware Prefetch Capability	16	0b	When set (1b) this optional field indicates the host controller supports the Hardware Prefetching capability and associated USBCMD *Fully Synchronized Prefetch, Periodic Schedule Prefetch Enable*, and *Asynchronous Schedule Prefetch Enable* fields. Note that software should treat those fields as reserved when this bit is cleared (0b).
Link Power Management Capability	17	0b	When set (1b) this optional field indicates host controller support for the Link Power Management L1 state and associated PORTSC *Suspend using L1*, *Suspend Status*, and *Device Address* fields. Note that software should treat those fields as reserved when this bit is cleared (0b).

HCCPARAMS – R - 32 bits - [MEM_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Per-Port Change Event Capability**	18	0b	When set (1b) this optional field indicates host controller support for per-port change events and associated USBCMD *Per-Port Change Event Enable*, USBSTS *Port-n Change Detect*, and USBINT *Port-n Change Interrupt Enable* fields. Note that software should treat those fields as reserved when this bit is cleared (0b).
32-Frame Periodic List Capability	19	0b	When set (1b) this optional field indicates the host controller supports a 32 frame periodic schedule as specified by using the value 11b in the USBCMD *Frame List Size* field. Software must treat a *Frame List Size* value of 11b as reserved when this bit is cleared (0b). Note that support for other programmable *Frame List Size* values (01b = 512 frames, 10b = 256 frames) continues to be indicated through the *Programmable Frame List Flag*, where this bit only indicates programmability for a 32-frame list.
Reserved	31:20		These bits are reserved and should be set to 0.
* Bits [7:4] and bit[0] are read-only but can be enabled to write through back-door register EHCI_EOR x90[1]. ** Bit[18] is read-only and the value comes from EHCI_CFG x50h[7].			

2.2.6.2 EHCI Operational Register

2.2.6.2.1 EHCI Memory Mapped Registers: Host Controller Operational Registers (EHCI_EOR 0x00 ~ 0xCC)

This block of registers is memory-mapped. The base offset, EHCI_EOR, is defined in CAPLENGTH register (MEM_Reg:00h, default value = 20h).

Registers Name	Offset Address
USB Command – USBCMD	EHCI_EOR + 00h
USB Satus – USBSTS	EHCI_EOR + 04h
USB Interrupt Enable – USBINTR	EHCI_EOR + 08h
USB Frame Index – FRINDEX	EHCI_EOR + 0Ch
4G Segment Selector – CTRLDSSEGMENT	EHCI_EOR + 10h
Frame List Base Address – PERIODICLISTBASE	EHCI_EOR + 14h
Next Asynchronous List Address – ASYNCLISTADDR	EHCI_EOR + 18h
Reserved	EHCI_EOR + (1Ch~3Fh)
Configured Flag – CONFIGFLAG	EHCI_EOR + 40h
Port Status/Control – PORTSC (1-N_PORTS)	EHCI_EOR + (44h~54h)
	EHCI_EOR + 80h
Packet Buffer Threshold Values	EHCI_EOR + 84h
USB PHY Status 0	EHCI_EOR + 88h
USB PHY Status 1	EHCI_EOR + 8Ch
USB PHY Status 2	EHCI_EOR + 90h
UTMI Control	EHCI_EOR + 94h
Loopback Test	EHCI_EOR + 98h
EOR MISC Control	EHCI_EOR + 9Ch
USB Phy Calibration	EHCI_EOR + A0h
USB Common PHY Control	EHCI_EOR + A4h
EOR Debug Purpose	EHCI_EOR + A8h
EOR Spare 1	EHCI_EOR + ACh
USB Debug Port	0E0h~0F0h

USBCMD – RW - 32 bits - [EOR_Reg:EHCI_EOR+00h]			
Field Name	**Bits**	**Default**	**Description**
Run/Stop (RS)	0	0b	1: Run 0: Stop. When set to 1, the Host Controller proceeds with execution of the schedule. The Host Controller continues execution as long as this bit is set to 1. When this bit is set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears the Run bit. The HC Halted bit in the status register indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a 1 to this field unless the host controller is in the Halted state (i.e. HCHalted in the USBSTS register is a one). Doing so will yield undefined results.

USBCMD – RW - 32 bits - [EOR_Reg:EHCI_EOR+00h]			
Field Name	**Bits**	**Default**	**Description**
Host Controller Reset (HCRESET)	1	0b	This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a 1 to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller in order to return the host controller to an operational state. This bit is set to 0 by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this register. Software should not set this bit to a 1 when the HCHalted bit in the USBSTS register is a 0. Attempting to reset an actively running host controller will result in undefined behavior.
Frame List Size	3:2	00b	Read/Write or Read-only. This field is R/W only when one or both of the Programmable Frame List Flag and 32-Frame Periodic List Capability bits in the HCCPARAMS registers are set to 1. This field specifies the size of the frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values are: 00b: 1024 frames [default] 01b: 512 frames 10b: 256 frames 11b: Reserved or 32 frames (see below) Software may only program a 32 frame list when the *32-Frame Periodic List Capability* bit in the HCCPARAMS register is set to one, and a 512 or 256 frame list when the *Programmable Frame List Flag* is set to one. Note that hardware employs a slightly different model for Frame List Rollover events when a 32 frame list is in use; see the *Frame List Rollover* field in USBSTS register for more information.
Periodic Schedule Enable	4	0b	This bit controls whether the host controller skips processing the Periodic Schedule. 0: Do not process the Periodic Schedule 1: Use the PERIODICLISTBASE register to access the Periodic Schedule.
Asynchronous Schedule Enable	5	0b	This bit controls whether the host controller skips processing the Asynchronous Schedule. 0: Do not process the Asynchronous Schedule 1: Use the ASYNCLISTADDR register to access Asynchronous Schedule.
Interrupt on Async Advance Doorbell	6	0b	This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to *ring* the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS register. If the Interrupt on Async Advance Enable bit in the USBINTR register is 1 then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to 0 after it has set the Interrupt on Async Advance status bit in the USBSTS register to 1. Software should not write a 1 to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.

USBCMD – RW - 32 bits - [EOR_Reg:EHCI_EOR+00h]			
Field Name	**Bits**	**Default**	**Description**
Light Host Controller Reset (Optional)	7	0b	This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or the relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to 0 (retaining port ownership relationships). A host software read of this bit as 0 indicates the Light Host Controller Reset has completed and it is safe for host software to re-initialize the host controller. A host software read of this bit as a 1 indicates the Light Host Controller Reset has not yet completed. If not implemented, a read of this field will always return 0.
Asynchronous Schedule Park Mode Count (Optional)	9:8	11b	Read/Write or Read-only. If the Asynchronous Park Capability bit in the HCCPARAMS register is a 1, then this field defaults to 3h and is R/W; otherwise it defaults to 0 and is read-only. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 1h to 3h. Software must not write a 0 to this bit when Park Mode Enable is a 1, as this will result in undefined behavior.
Reserved	10		This bit is reserved and should be set to 0.
Asynchronous Schedule Park Mode Enable (Optional)	11	1b	Read/Write or Read-only. If the Asynchronous Park Capability bit in the HCCPARAMS register is a 1, then this bit defaults to a 1h and is R/W. Otherwise the bit must be a 0 and is read-only. Software uses this bit to enable or disable Park mode. When this bit is 1, Park mode is enabled. When this bit is 0, Park mode is disabled.
Periodic Schedule Prefetch Enable (OPTIONAL)	12	0b	If the *Hardware Prefetch Capability* bit in the HCCPARAMS register is set (1b) then this bit is R/W; otherwise it is read-only. This bit should only be used by software – and thereby only set – when the *Fully Synchronized Prefetch* bit is enabled. Software sets this bit (1b) to enable hardware prefetching of the periodic schedule. Hardware prefetching must be disabled before software applies any changes to the periodic schedule or structures linked to this schedule. To disable hardware prefetching software must first write a 0b and then wait until a read of this field returns 0b – noting the host controller must return a value of 1b until hardware prefetching of the periodic schedule has been safely disabled. Software re-enables hardware prefetching by writing a 1b to this bit once all updates to the periodic schedule have been applied. Note that hardware prefetching of the asynchronous schedule may remain active when software is solely modifying the periodic schedule.

USBCMD – RW - 32 bits - [EOR_Reg:EHCI_EOR+00h]			
Field Name	**Bits**	**Default**	**Description**
Asynchronous Schedule Prefetch Enable (OPTIONAL)	13	0b	If the *Hardware Prefetch Capability* bit in the HCCPARAMS register is set to a one then this bit is R/W; otherwise it is read-only. This bit should only be used by software – and thereby only set – when the *Fully Synchronized Prefetch* bit is enabled. Software sets this bit (1b) to enable hardware prefetching of the asynchronous schedule. Hardware prefetching must be disabled before software applies any changes to the asynchronous schedule or structures linked to this schedule. To disable hardware prefetching software must first write a 0b and then wait until a read of this field returns 0b – noting the host controller must return a value of 1b until hardware prefetching of the asynchronous schedule has been safely disabled. Software re-enables hardware prefetching by writing a 1b to this bit once all updates to the asynchronous schedule have been applied. Note that hardware prefetching of the periodic schedule may remain active when software is solely modifying the asynchronous schedule.
Fully Synchronized Prefetch (OPTIONAL)	14	0b	If the *Hardware Prefetch Capability* bit in the HCCPARAMS register is set to a one then this bit is R/W; otherwise it is read-only. This field is used to inform hardware whether software fully supports the use of the *Asynchronous Schedule Prefetch Enable* (ASPE) and *Periodic Schedule Prefetch Enable* (PSPE) fields, where software guarantees that any and all updates to the periodic and/or asynchronous schedules by software will only occur when hardware prefetching of the associated schedule has been fully disabled as described below. Note that software should not use the ASPE and PSPE fields unless this bit is set (1b).
Per-Port Change Events Enable	15	0b	If the *Per-Port Change Event Capability* bit in the HCCPARAMS register is set to a one then this bit is R/W; otherwise it is read-only. This field is used by system software to enable the per-port change event capability as defined by the *Port-n Change Detect* field in the USBSTS register and *Port-n Change Detect Enable* field in the USBINTR register. Note that enabling per-port change events has no affect on the existing *Port Change Detect* capability. In other words, one or both of these may be enabled and used by software independently of the other, where per-port change events can be used to streamline the process for resolving which port(s) caused a given event (interrupt).
Interrupt Threshold Control	23:16	08h	This field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. 00h: Reserved 01h: 1 micro-frame 02h: 2 micro-frames 04h: 4 micro-frames 08h: 8 micro-frames (default, equates to 1 ms) 10h: 16 micro-frames (2 ms) 20h: 32 micro-frames (4 ms) 40h: 64 micro-frames (8 ms) Any other value in this register yields undefined results. Software modifications to this bit while HCHalted bit is equal to 0 results in undefined behavior.

USBCMD – RW - 32 bits - [EOR_Reg:EHCI_EOR+00h]			
Field Name	**Bits**	**Default**	**Description**
Host-Initiated Resume Duration	27:24	0h	If the *Link Power Management Capability* bit in the HCCPARAMS register is set to one then this bit is R/W; otherwise it is read-only. This field is used by system software to specify the minimum amount of time the host controller will drive the K-state during a host-initiated resume from a LPM state (e.g. L1), and is conveyed to each LPM-enabled device (via the *HIRD* bits within an LPM Token's *bmAttributes* field) upon entry into a low-power state. Use of this field by the host controller is implementation specific, however, and thus software should consider this a hint. Note the host controller is required to drive resume signaling for *at least* the amount of time specified in the *HIRD* value conveyed to the device during any proceeding host-initiated resume. Also note that the host controller is *not* required to observe this requirement during device-initiated resumes. Encoding for this field is identical to the definition for the similarly named *HIRD* field within an LPM Token, specifically: a value 0000b equals 50us and each additional increment adds 75us. For example, the value 0001b equals 125us, and a value 1111b equals 1,175us (~1.2ms).
Reserved	31:28		These bits are reserved and should be set to 0s.

USBSTS - RW - 32 bits - [EOR_Reg:EHCI_EOR+04h]			
Field Name	**Bits**	**Default**	**Description**
USBINT	0	0b	USB Interrupt. The host controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).
USBERRINT	1	0b	USB Error Interrupt. The host controller sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and the USBINT bit are set.
Port Change Detect	2	0b	The host controller sets this bit to 1 when any port for which the Port Owner bit is set to 0 has a change bit transition from a 0 to a 1 or a Force Port Resume bit transition from a 0 to a 1 as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Change being set to a 1 after system software has relinquished ownership of a connected port by writing a 0 to a port's Port Owner bit. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, over-current change, enable/disable change and connect status change).
Frame List Rollover	3	0b	The host controller sets this bit to a 1 when a frame list rollover event occurs. The exact Frame List Index value at which the rollover occurs depends on the frame list size, noting this generally occurs when FRINDEX rolls over from its maximum value to zero. For example, if the frame list size (as programmed in the Frame List Size field of the USBCMD register) is 1024, then a frame list rollover would occur every time FRINDEX[13] toggles. Similarly, a frame list rollover would occur every time FRINDEX[12] toggles for a 512 frame list, and when FRINDEX[11] toggles for a 256 frame list. Note this behavior is different for a 32 frame list where a rollover event occurs every time FRINDEX[13] toggles (same as 1024).

USBSTS - RW - 32 bits - [EOR_Reg:EHCI_EOR+04h]			
Field Name	**Bits**	**Default**	**Description**
Host System Error	4	0b	The host controller sets this bit to 1 when a serious error occurs during a host system access involving the host controller module. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the host controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
Interrupt on Async Advance	5	0b	System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
Reserved	11:6		These bits are reserved and should be set to 0.
HCHalted	12	1b	This bit is a 0 whenever the Run/Stop bit is a 1. The host controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the host controller hardware (e.g. internal error). [Read-only]
Reclamation	13	0b	This is a read-only status bit, which is used to detect an empty asynchronous schedule. [Read-only]
Periodic Schedule Status	14	0b	The bit reports the current real status of the Periodic Schedule. If this bit is a 0, then the status of the Periodic Schedule is disabled. If this bit is a 1, then the status of the Periodic Schedule is enabled. The host controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, Periodic Schedule is either enabled (1) or disabled (0). [Read-only]
Asynchronous Schedule Status	15	0b	The bit reports the current real status of the Asynchronous Schedule. If this bit is a 0, then the status of the Asynchronous Schedule is disabled. If this bit is a 1, then the status of the Asynchronous Schedule is enabled. The host controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0). [Read-only]
Port-n Change Detect	31:16	0000h	If the *Per-Port Change Event Capability* bit in the HCCPARAMS register is set to 1 then this field is R/W; otherwise it is read-only. This field should only be used by software when the *Per-Port Change Events Enable* bit within the USBCMD register is set to 1. The definition for each bit is identical to the *Port Change Detect* field (bit 2 of this register) except these bits are specific to a given port, where bit 16 = Port 1, 17 = Port 2, etc. For example, if bit 17 is set to a one then a port change event was detected on Port 2. The N_PORTS field in HCSPARAMS specifies how many ports are exposed by the host controller and thus how many bits in this field are valid. Hardware must preserve the behavior of the *Port Change Detect* and related fields even when Per-Port Change Events are enabled, noting software may choose to employ one or both of these capabilities. [Read-only or Read/Write-clear]

USBINTR –RW - 32 bits - [EOR_Reg:EHCI_EOR+08h]			
Field Name	**Bits**	**Default**	**Description**
USB Interrupt Enable	0	0b	When this bit is a 1, and the USBINT bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.
USB Error Interrupt Enable	1	0b	When this bit is a 1, and the USBERRINT bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
Port Change Interrupt Enable	2	0b	When this bit is a 1, and the Port Change Detect bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
Frame List Rollover Enable	3	0b	When this bit is a 1, and the Frame List Rollover bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
Host System Error Enable	4	0b	When this bit is a 1, and the Host System Error Status bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
Interrupt on Async Advance Enable	5	0b	When this bit is a 1, and the Interrupt on Async Advance bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
Reserved	15:6		These bits are reserved and should be 0
Port-n Change Event Enable	31:16	0000h	The definition for each bit in this field is identical to bit[2] of this register (Port Change Interrupt Enable) except these bits are specific to a given port, where bit[16] = Port 1, bit[17] = Port 2, etc. For example, if bit[17] is set (1b), then a port change event was detected on Port 2. When a bit in this field is a 1, and the corresponding Port-n Change Detect bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the *Port-n Change Detect* bit.

FRINDEX –RW - 32 bits - [EOR_Reg:EHCI_EOR+0Ch]			
Field Name	**Bits**	**Default**	**Description**
Frame Index	13:0	0h	The value in this register increments at the end of each time frame (e.g. micro-frame). Bits [N:3] are used for the Frame List Current Index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following illustrates values of *N* based on the value of the *Frame List Size* field in the USBCMD register. **USBCMD [Frame List Size]** / **Number of Elements** / **N** 00b / 1024 / 12 01b / 512 / 11 10b / 256 / 10 11b / 32 / 12 (see Note) **Note:** The host controller behaves slightly different when using a 32-frame *Frame List Size*, specifically it continues to count FRINDEX up to a full 1024 frames, transmit SOF values from 0 to 2047, and generate *Frame List Rollover* events (when enabled) every 1024 frames – exactly as if a 1024 frame list size was employed. The host controller will only reference 32 elements on the periodic schedule, however. This is accomplished by formulating the Periodic Frame List Element Address using {FRINDEX[N:3] modulo 32} rather than FRINDEX[N:3]. The same mapping should be done by system software whenever it needs to correlate the current FRINDEX value to a specific periodic schedule element. Note this new behavior only applies to a 32-frame list.
Reserved	31:14		These bits are reserved and should be 0

CTRLDSSEGMENT –RW - 32 bits - [EOR_Reg:EHCI_EOR+10h]			
Field Name	**Bits**	**Default**	**Description**
CTRLDSSEGMENT	31:0	0h	This 32-bit register corresponds to the most significant address bits [63:32] for all EHCI data structures. If the 64-bit Addressing Capability field in HCCPARAMS is a 0, then this register is not used. Software cannot write to it and a read from this register will return 0s. If the 64-bit Addressing Capability field in HCCPARAMS is a 1, then this register is used with the link pointers to construct 64-bit addresses to EHCI control data structures. This register is concatenated with the link pointer from either PERIODICLISTBASE, or ASYNCLISTADDR, or any control data structure link field to construct a 64-bit address. This register allows the host software to locate all control data structures within the same 4 Gigabyte memory segment.

PERIODICLISTBASE –RW - 32 bits - [EOR_Reg:EHCI_EOR+14h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	11:0		These bits are reserved. Must be written as 0s. During runtime, the values of these bits are undefined.
Base Address	31:12	000h	These bits correspond to memory address signals [31:12], respectively.

ASYNCLISTADDR –RW - 32 bits - [EOR_Reg:EHCI_EOR+18h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	4:0		These bits are reserved and their value has no effect on operation.
Link Pointer Low (LPL)	31:5	00h	These bits correspond to memory address signals [31:5], respectively. This field may only reference a Queue Head (QH).

CONFIGFLAG –RW - 32 bits - [EOR_Reg:EHCI_EOR+40h]			
Field Name	**Bits**	**Default**	**Description**
Configure Flag (CF)	0	0b	Host software sets this bit as the last action in its process of configuring the host controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below: 0: Port routing control logic default-routes each port to an implementation dependent classic host controller. 1: Port routing control logic default-routes all ports to this host controller.
Reserved	31:1		These bits are reserved and should be set to 0.

PORTSC (1-N_PORTS) – RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Current Connect Status	0	0b	1: Device is present on port. 0: No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (bit 1) to be set. This field is 0 if Port Power is 0. [Read-only]
Connect Status Change	1	0b	1: Change in Current Connect Status. 0: No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. This field is 0 if Port Power is 0.
Port Enabled/Disabled	2	0b	1: Enable. 0: Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this field. The host controller will only set this bit to a 1 when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled (0b), downstream propagation of data is blocked on this port, except for reset. This field is 0 if Port Power is 0.
Port Enable/Disable Change	3	0b	1: Port enabled/disabled status has changed. 0: No change. For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2. Software clears this bit by writing a 1 to it. This field is 0 if Port Power is 0.

PORTSC (1-N_PORTS) – RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Over-current Active	4	0b	1: This port currently has an over-current condition. 0: This port does not have an over-current condition. This bit will automatically transition from a 1 to a 0 when the overcurrent condition is removed.
Over-current Change	5	0b	1: This bit gets set to a 1 when there is a change to Over-current Active. Software clears this bit by writing a 1 to this bit position.
Force Port Resume	6	0b	1: Resume detected/driven on port. 0: No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend and Suspend Using L1 bits. For example, if the port is not suspended (Suspend and Enabled bits are a 1) and software transitions this bit to a 1, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a 1 because a J-to-K transition is detected, the Port Change Detect and/or Port-n Change Detect bits in the USBSTS register is also set to a 1. If software sets this bit to a 1, the host controller must not set the Port Change Detect and/or Port-n Change Detect bits. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a 1. For legacy (L2) transitions, software must appropriately time the Resume and set this bit to a 0 when the appropriate amount of time has elapsed. Writing a 0 (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a 1 until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a 0. Software does not need to time resume signaling for L1 transactions as host controller hardware will automatically enforce the necessary timing and clear this bit when the port has fully resumed. Software can influence the amount of time hardware will drive resume signaling during L1 exit via the *Host-Initiated Resume Duration* field within the USBCMD register. This field is 0 if Port Power is 0.

PORTSC (1-N_PORTS) – RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Suspend	7	0b	1: Port in suspend state. 0: Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: **Bits [Port Enabled, Suspend]** **Port State** 0X Disable 10 Enable 11 Suspend Software writes a 1 to this bit to transition a port to either the L1 or L2 suspend state. Which suspend state the host controller attempts depends on the value of the *Suspend Using L1* field. When in suspend state, downstream propagation of data is blocked on this port, except for port reset. If this bit is set to a 1 when a transaction is in progress then the blocking will not occur until the end of the current transaction. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. Addition status for L1-based transitions is provided to software via the *Suspend Status* field. A write of 0 to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a 0 when: - Software sets the Force Port Resume bit to a 0 (from a 1). - Software sets the Port Reset bit to a 1 (from a 0). - Whenever Port Power is zero. If system software sets this bit to a 1 when the port is not enabled (i.e. Port Enabled bit is a 0) the results are undefined. This field is 0 if Port Power is 0.
Port Reset	8	0b	1: Port is in Reset. 0: Port is not in Reset. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a 1, it must also write a 0 to the Port Enable bit. Note that when software writes a 0 to this bit there may be a delay before the bit status changes to a 0. The bit status will not read as a 0 until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the *Port Enable* bit to a 1). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a 1 to a 0. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a 0. The HCHalted bit in the USBSTS register should be a 0 before software attempts to use this bit. The host controller may hold Port Reset asserted to a 1 when the HCHalted bit is a 1. This field is 0 if Port Power is 0.

PORTSC (1-N_PORTS) – RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Suspend using L1	9	0b	0b = Suspend using L2; 1b = Suspend using L1 (LPM). When this bit is set to a 1, and a non-zero value is specified in the *Device Address* field, the host controller will generate an LPM Token to enter the L1 state whenever software writes a 1 to the *Suspend* bit, as well as L1 exit timing during any device- or host-initiated resume. When set to 0 the host controller will employ the legacy (L2) suspend mechanism. Software should only set this bit when the device attached immediately downstream of this root port supports L1 transitions. [Read-write]
Line Status	11:10		These bits reflect the current logical levels of the D+ (bit [11]) and D- (bit [10]) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is 0 and the current connect status bit is set to 1. The encoding of the bits are: **Bits[11:10] USB State Interpretation** 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset. This value of this field is undefined if Port Power is 0. [Read-only]
Port Power	12		Read/write or Read-only. The function of this bit depends on the value of the Port Power Control (PPC) field in the HCSPARAMS register. The behavior is as follows: **PPC PP Operation** 0b 1b R - ???Host controller does not have port power control switches. Each port is hard-wired to power. 1b 1b/0b RW - Host controller has port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (i.e., PP = 0), the port is non-functional and will not report attaches, detaches, etc. When an over-current condition is detected on a powered port and PPC = 1, the PP bit in each affected port may be transitioned by the host controller from 1 to 0 (removing power from the port).
Port Owner	13	1b	This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is 0. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a 1 to this bit when the attached device is not a high-speed device. A 1 in this bit means that a companion host controller owns and controls the port.

PORTSC (1-N_PORTS) – RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Port Indicator Control	15:14	00b	Writing to this bit has no effect if the P_INDICATOR bit in the HCSPARAMS register is 0. If P_INDICATOR is 1, then the bit encodings are as follows: **Bit Value Meaning** 00b Port indicators are off 01b Amber 10b Green 11b Undefined Refer to the USB Specification Revision 2.0 for a description on how these bits are to be used. This field is 0 if Port Power is 0.
Port Test Control	19:16	0000b	When this field is 0, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are as follows: **Bits Test Mode** 0000b Test mode not enabled 0001b Test J_STATE 0010b Test K_STATE 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE 0110b - 1111b are reserved
Wake on Connect Enable	20	0	Writing this bit to a 1 enables the port to be sensitive to device connects as wake-up events. This field is 0 if Port Power is 0.
Wake on Disconnect Enable	21	0b	Writing this bit to a 1 enables the port to be sensitive to device disconnects as wake-up events. This field is 0 if Port Power is 0.
Wake on Over-current Enable	22	0b	Writing this bit to a 1 enables the port to be sensitive to over-current conditions as wake-up events. This field is 0 if Port Power is 0.
Suspend Status	24:23	00b	These two bits are used by software to determine whether the most recent L1 suspend request was successful, specifically: **Value Meaning** 00b Success: State transition was successful (ACK) 01b Not Yet: Device was unable to enter the L1 state at this time (NYET) 10b Not Supported: Device does not support the L1 state (STALL) 11b Timeout/Error: Device failed to respond or an error occurred This field is updated by hardware immediately following the completion of an L1 transition request (via an LPM Token). To avoid any race conditions with hardware, software should only consume the contents of this field when Suspend = 0b (port no longer in L1).
Device Address	31:25	00h	The 7-bit USB device address for the device attached to and immediately downstream of the associated root port. A value of 0 indicates no device is present or support for this feature is not present. [Read-only or Read-write]

Packet Buffer Threshold Values – RW - 32 bits - [EOR_Reg:EHCI_EOR+84h]			
Field Name	**Bits**	**Default**	**Description**
IN Threshold	7:0	10h	The PCI transaction starts when threshold of internal FIFO for receive packet is reached. The value represents multiple of 8 bytes – 10h means 128 bytes. The smallest acceptable value is 08h (64 bytes).
Reserved	15:8		Reserved
OUT Threshold	23:16	40h	The transmit packet starts at UTMI interface when threshold of internal FIFO for transmit packet is reached. The value represents multiple of 8 bytes – 10h means 128 bytes. The smallest acceptable value is 08h (64 bytes).
Reserved	31:24		Reserved

USB PHY Status 0 – R - 32 bits - [EOR_Reg:EHCI_EOR+88h]			
Field Name	**Bits**	**Default**	**Description**
PORT0_PHYStatus	7:0	xxh*	PHY Status of Port0 *xx denotes non-specified
PORT1_PHYStatus	15:8	xxh	PHY Status of Port1
PORT2_PHYStatus	23:16	xxh	PHY Status of Port2
PORT3_PHYStatus	31:24	xxh	PHY Status of Port3

Note: Use the VControlModeSel (UTMI_Control register[9:7]) to select which group of status should be read back.

PORTn_PHYStatus selection is controlled via the UTMI Control register (EOR_Reg:EHCI_EOR+94h). When UTMI_Control[0]==1 the following tables specify PORTn_PHYStatus:

UTMI_Control[8:6] == 000b

Bit	Description
2:0	HSADJ2-0
5:3	DUTYADJ2-0
6	CLKOFF bit to turn off UTMI clock
7	Ebuffer error or rx error

UTMI_Control[8:6] == 001b

Bit	Description
0	Irsync
1	Istate, state of the ebuffer
2	sync from rxdec
3	latch_hseopr
6:4	rxstate
7	group3_vcontrol[0]

UTMI_Control[8:6] == 010b

Bit	Description
3:0	group1_vcontrol[3:0]
4	CONNECT_STATUS
5	VDM_SRC_EN
6	IDP_SINK_EN
7	VDAT_DET

UTMI_Control[8:6] == 011b

Bit	Description
7:0	CDREnClkStatus

UTMI_Control[8:6] == 100b

Bit	Description
0	ADISCONN
1	HS_SQUEL
3	xtion_limit_status
7:3	5'd0

When UTMI_Control[0]==0, UTMI_Control[9:7] (VControlModeSel) selects the corresponding VControl register to PORTn_PHYStatus.

VControlModeSel	Description
000b	{0, group0_vcontrol[6:0]}
001b	{0, group1_vcontrol[6:0]}
010b	{0, group2_vcontrol[6:0]}
011b	{0, group3_vcontrol[6:0]}
100b	{0, group4_vcontrol[6:0]}
101b	{0, group5_vcontrol[6:0]}
110b	{0, group6_vcontrol[6:0]}
111b	{0, group7_vcontrol[6:0]}

USB PHY Status 1 – R - 32 bits - [EOR_Reg:EHCI_EOR+8Ch]			
Field Name	**Bits**	**Default**	**Description**
PORT4_PHYStatus	7:0	xxh	PHY Status of Port4
Reserved	31:8	xxh	Reserved

UTMI Control – RW - 32 bits - [EOR_Reg:EHCI_EOR+94h]			
Field Name	**Bits**	**Default**	**Description**
VControl	6:0	24h	Control PHY setting **Group-0** (VControlModeSel=0) VControl[6:0] = { , DUTYADJ[2:0], HSADJ[2:0]} *HSADJ* : HS TX current adjustment – default 001b. Bit 0 adds 5% when set to "1" Bit 1 adds 10% when set to "1" Bit 2 adds 10% when set to "1" We'll have 000 : 0% **001 : 5%** 010 : 10% 011 : 15% 100 : 10% 101 : 15% 110 : 20% 111 : 25% *DUTYADJ*: adjust clk480 (in analog PHY) duty cycle – default 100b. 000 +8% 001 +3% 010 +5% 011 +2% **100 +1%** 101 -1% 110 -1.6% 111 -5.5% **Group-1** (VControlModeSel =1) VControl[6:0] = { , TESTMODE[3:0]}
			TESTMODE[3:0] Description 0000 Disable Test Mode
VControlModeSel	9:7	0h	The PHY control modes are divided into 4 groups. VcontrolModeSel is used to select the group.
Reserved	11:10		Reserved
VLoadB	12	1b	Update PHY control mode (active load) 0: load the new VControl value to PHY/common block 1: only VControlModeSel value to PHY will be updated for selecting different PHY status group (see PHY status registers, EOR_Reg x88 ~ x90). But VControl[6:0] value inside PHY won't get affected.
Port Number	16:13	0h	Select the corresponding port PHY or common block to load the VControl bits. 0000: port0 0001: port1 0010: port2 …… 0100: port4 0101 ~ 1110: Reserved , no effect 1111: Common block
VBusy	17	0b	Read-only. To block software write to bits[16:8] when port router is updating the field.
Reserved	31:18		Reserved

UTMI Control – RW - 32 bits - [EOR_Reg:EHCI_EOR+94h]
Note: Group1 - Group7 Vcontrol can be read back through USB PHY Status 0, USB PHY Status 1 registers. In order to read Group1 ~ Group7 Vcontrol: Set: UTMI_Control[0] = 0 UTMI_Control[9:7] = Group# UTMI_Control[16:13] = PHY Port Number Read corresponding PORTx_PHYStatus field of USB PHY Status

Loopback Test – RW - 32 bits - [EOR_Reg:EHCI_EOR+98h]			
Field Name	**Bits**	**Default**	**Description**
Received Packet Count	3:0	0h	RX data packet count. This counter defines the number (in power of 16) of RX data packet that should be checked for the loop back test.
Reserved	7:4		Reserved
Enable Loop Back Test	8	0b	Enable external USB port loopback test. The loopback test is to set one port to TX mode (Test Packet mode) and one port to RX mode (Test SE0_NAK). Refer to PORTSC [19:16] for information on the tests.
Loopback Test Status	9	0b	Read-only. 0: CRC error on loopback receiving data 1: Good CRC on loopback receiving data
Loopback Test Done	10	0b	Read-only. Indicates loopback test is done.
Reserved	11	0b	
Good Received Packet Count	19:12	--	Read-only. The number of good packets that the host controller received during the loopback test mode. These bits will be cleared by clearing bit[8] (Enable Loop Back test).
Enable PHY PowerUp State Checking	20	0b	Enable auto-checking on PHY Power Up State. There is built-in logic to check the PHY default Power Up state to detect manufacturing defects in the PHY macro.
Status of ports for PowerUp State Check	26:21	000000b	Read-only. Status bit to indicate the Power Up state auto-checking result from the individual port. Each bit maps to a corresponding port, from port-0 to port-5, i.e. bit-21 for port-0, bit-22 for port-1, and so on. The value can only be checked when the PHY PowerUp State Checking Done bit is set. 0: PHY Power Up State checking is fail. 1: PHY Power Up State checking is good.
Reserved	31:27	00000b	

EOR MISC Control – RW - 32 bits - [EOR_Reg : EHCI_EOR + 9Ch]			
Field Name	**Bits**	**Default**	**Description**
Enable Interrupt on ForcePortResume	0	0b	Enable host controller to generate interrupt on software clear ForcePortResume bit in PORTSC[6].
Interrupt route Control on ForcePortResume	1	0h	Report interrupt status to either USBINT bit or Port Change Detect bit in the USBSTS register on software clear “ForcePortResume” bit. This bit only takes effect when the Enable Interrupt on ForcePortResume bit is set. 0: Report interrupt on USBINT bit in USBSTS register 1: Report interrupt on Port Change Detect bit in USBSTS register
Reserved	3:2	0h	Reserved

EOR MISC Control – RW - 32 bits - [EOR_Reg : EHCI_EOR + 9Ch]			
Field Name	**Bits**	**Default**	**Description**
Inter-packet Gap Adjust Counter	7:4	4h	Counter used to adjust the inter-packet gap for test packet.
Reserved	10:8	00b	Reserved
Disables HS uFrame Babble detection	11	0b	Disables HS uFrame babble detection (see uhc2_rhprt: eor_disa_framebabbledet_i).
EHCI Power Saving Enable	12	1b	Enable power saving clock gating. When enabled, dynamic clock gating is enabled when EHCI is not in operational mode. The clock going to all memory modules will be gated off. Blink clock also gets gated off unless the connection interrupt is detected.
Reserved	13	0h	Reserved
EHCI Deep Blink Power Saving Enable	14	0h	Enable Deep Blink power saving clock gating. When enabled, EHCI will request to stop the Global Blink clock when the processor is idle.
Reserved	23:15	0h	Reserved
Force Txdata [7:0]	31:24	00h	Used to force txdata[7:0] when the port is in TEST_K mode. This can be used to force PHY to generate a desired output pattern for PHY debugging and characterization purposes.

USB Common PHY CAL & Control Register – RW - 32 bits - [EOR_Reg:EHCI_EOR+A0h]			
Field Name	**Bits**	**Default**	**Description**
ComCalBus	6:0		Read-only. Calibration bus value from PHY before adjustment. Default value = Don't care.
Reserved	7	0b	Reserved
NewCalBus	15:8	00h	New calibration bus signed value.
UseCommonCalibration	16	0b	If set, the PHY's calibration value in bits[6:0] is returned to the PHY ports. If cleared, the value after adjustment is returned to the PHY ports.
AddToCommonCalibration	17	1b	If set, the signed NewCalBus is added to the ComCalBus and returned to the PHY ports. Any overflow is clamped to all 1s. Any underflow is clamped to all 0s. If cleared, the signed NewCalBus replaces the ComCalBus and returns to the PHY ports.
Reserved	23:18	0000h	Read as 0.
CommonPhyCalBus	30:24	7Fh	Read-only. PHY Common Calibration Bus
Reserved	31	0b	

Note:

1. The equation for the calibration resistor value is

   Rcal = 1/ [1/59.4 + CalValue/(1.05*3.8k ohm)]

   where CalValue is the final 7 bits of calibration setting sent to PHY.

2. The total termination resistance value for HS USB D+/D- should include another 5 ohm resistance from the FS driver.

USB Common PHY Control – RW - 32 bits - [EOR_Reg:EHCI_EOR+A4h]			
Field Name	**Bits**	**Default**	**Description**
CPADJ (*)	3:0	4h	Charge Pump setting for common block PLL.
XREFADJ (*)	7:4	1h	External reference bias adjustment for common block.
IREFADJ (*)	11:8	1h	Internal reference bias adjustment for common block.
PVI (*)	15:12	2h	PLL V-I Converter Control for common block PLL.
DUTYADJ (*)	19:16	4h	CLK480 duty cycle control from 40-60% to 60-40%.
PLL Bypass	20	0b	Enable USB Common PLL bypass
Reserved	23:21	0h	Reserved

USB Common PHY Control – RW - 32 bits - [EOR_Reg:EHCI_EOR+A4h]			
Field Name	**Bits**	**Default**	**Description**
DLL Control	31:24	A0h	USB PHY DLL control {DLL_VtoI[1:0], DLL_cpump[2:0], DLL_EN_PFDphases, reserved[1:0]} DLL_VtoI: DLL gain control DLL_cpump: DLL charge pump current control DLL_EN_PFDphases: Enable DLL phase-sampling based lock detection
* Note: Common block uses 3 bits for each control function, so the 4th bit of the control doesn't have any effect on the common block.			

2.2.7 USB 3.0 Control Registers inside ACPI

2.2.7.1 ACPI PMIO Registers

USB 3.0 functions can be controlled by the PMIO registers. PMIO registers are accessed through address/data ports via IO 0xCD6 and 0xCD7 (Index is programmed into IO 0xCD6 and the data is through IO 0xCD7). The following are such PMIO registers located inside the ACPI Smbus controller.

Usb3Control - RW - 8 bits - [PM_Reg:EEh]			
Field Name	**Bits**	**Default**	**Description**
USB3 Power Select	1:0	00b	00: USB 3.0 is in S0 power rail. 01: USB 3.0 is in S3 power rail. 10: USB 3.0 is in S5 power rail. 11: USB 3.0 is in S5 power rail.

UsbControl – RW – 24 bits - [PM_Reg:F0h]			
Field Name	**Bits**	**Default**	**Description**
VCTRL_LD_POL_CTL	16	0b	Vcontrol_load Polarity Control Controls the value to which isolation cell forces vcontrol_load_n when USB 3.0 is powered down. 0: vcontrol_load_n gated to 1'b0. 1: vcontrol_load_n gated to 1'b1.
USB_TAP_LATCH_CTL	17	0b	USB Tap Latch Control Controls the time at which the USB 2.0 controller decodes the target controller id from the tap controller. 0: Command latched after decoding controller id. 1: Command latched before decoding controller id.
Reserved	18	0b	
PMIO_BLM_RST_MODE	19	0b	BLM Reset Mode 0: XHC S0 BLM won't be reset during D3 state. 1: XHC S0 BLM will be reset during D3 state.
Reserved	23:20	0h	

2.2.7.2 ACPI MMIO Registers

64 double words of ACPI MMIO space registers are used to control USB3.0 function. These registers actually reside in USB3.0 and can hold their values during S3 or S5 state if one or more XHC hosts are programmed into D3 state before enter into S3/S5 state. XHC ACPI MMIO Registers Base Address is ACPI MMIO Base + 1C00h.

The range of this space is 1C00 to 1CFF.

Register Name	Offset Address
USB3.0_ACPI_MMIO_REG00	00h
USB3.0_ACPI_MMIO_REG04	04h
USB3.0_ACPI_MMIO_REG08	08h
USB3.0_ACPI_MMIO_REG0C	0Ch
USB3.0_ACPI_MMIO_REG10	10h
USB2.0 Wake Control	20h
USB3.0_ACPI_MMIO_REG24	24h
USB3.0_ACPI_MMIO_REG28	28h
USB3.0_ACPI_MMIO_REG2C	2Ch
XHCI_1_0_ENABLE	30h
USB3.0_ACPI_MMIO_REG34	34h
USB3.0_ACPI_MMIO_REG38	38h
Port Idle Timeout	3Ch
USB3.0_ACPI_MMIO_REG40	40h
SSPHY ACPI Indirect Index	48h
SSPHY ACPI Indirect Data	4Ch
CCUSSIFREG1_OVERRIDE	50h
CCUSSIFREG2_OVERRIDE	54h
CCUSSIFREG3_OVERRIDE	58h
CCUU2IFREG1_OVERRIDE	5Ch
SSPHY Common Control 1	90h
	94h
SSPHY Common Control 3	98h
	9Ch
SPI BAR0	A0h
SPI BAR1	A4h
SPI BAR2	A8h
SPI BAR3	ACh
SPI_valid_base	B0h
SPI Misc	B4h
SPI data blocks	C0h-FFh

USB3.0_ACPI_MMIO_REG00 - RW - 32 bits - [ACPI_USB3.0_REG: 00h]			
Field Name	**Bits**	**Default**	**Description**
XHCI0_ENABLE	0	0b	XHCI0 Enable 1: Enable XHCI0.
XHCI1_ENABLE	1	0b	XHCI1 Enable 1: Enable XHCI1
Reserved	6:2	0h	
U3P_LOCK	7	0b	USB3.0 PHY PLL Lock [Read Only] 1: USB3.0 PHY PLL Locked.
U3P_PLL_RESET	8	1b	USB3.0 PHY PLL Reset 1: Reset USB3.0 PHY PLL and SSPHYIF power control logic in LFPS clock domain.
U3P_PHY_RESET	9	1b	USB3.0 PHY Reset 1: Reset SSPHYIF power control logic in 125MHz clock domain.
U3_CORE_RESET	10	1b	USB3.0 Core Reset 1: Reset the USB3.0/XHCI (XHC0 + XHC1) core logic.

USB3.0_ACPI_MMIO_REG00 - RW - 32 bits - [ACPI_USB3.0_REG: 00h]			
Field Name	**Bits**	**Default**	**Description**
XHC0_RESET	11	0b	XHC0 Reset 1: Reset XHC0 core logic
XHC1_RESET	12	0b	XHC1 Reset 1: Reset XHC1 core logic.
Reserved	20:13	0h	
XHC_SMIB_EN	21	0b	XHC SMIB Enable 1: Enable XHC_SMIB to acpi controller.
Reserved	23:22	0h	
BL_GCG_DIS	24	0b	B-Link Global Clock Gating Disable 1: Disable USB3.0 B-Link Global Clock Gating
AL_GCG_DIS	25	0b	A-Link Global Clock Gating Disable 1: Disable USB3.0 A-Link Global Clock Gating
XHC0_BLM_CG_DIS	26	0b	XHC0 BLM Clock Gating Disable 1: Disable XHC0 BLM Clock Gating
XHC1_BLM_CG_DIS	27	0b	XHC1 BLM Clock Gating Disable 1: Disable XHC1 BLM Clock Gating
FW_LOAD_MODE	28	1b	Firmware Load Mode Controls whether the firmware will execute a bootstrap routine to load firmware to instruction ram, or whether instruction ram is to be preloaded. 0: XHCI will execute bootstrap routine. 1: XHCI will not execute bootstrap routine.
FW_PRELOAD_START	29	0b	Firmware Preload Start When set from 0->1, firmware preload will be initiated. Upon completion of firmware preload (see FW_PRELOAD_COMPLETE), FW_PRELOAD_START should be set to 0 by software.
FW_PRELOAD_COMPLETE	30	0b	Firmware Preload Complete [Read Only] Hardware will set this bit when it has completed firmware preload. Hardware will clear this bit when FW_PRELOAD_START is cleared by software.
Reserved	31	0b	

USB3.0_ACPI_MMIO_REG04 - RW - 32 bits - [ACPI_USB3.0_REG: 04h]			
Field Name	**Bits**	**Default**	**Description**
XHCI_FW_ROM_ADDR	15:0	0h	XHCI Firmware ROM Address Address of the first byte of application firmware in the extermal ROM.
XHCI_FW_SIZE	31:16	0h	XHCI Firmware Size Size of the application firmware in the external ROM.

USB3.0_ACPI_MMIO_REG08 - RW - 32 bits - [ACPI_USB3.0_REG: 08h]			
Field Name	**Bits**	**Default**	**Description**
XHCI_FW_INST_RAM_ADDR	15:0	0h	XHCI Firmware Instruction RAM Address Address where the first byte of application firmware is to be stored in instruction RAM.
Reserved	31:16	0h	

USB3.0_ACPI_MMIO_REG10 - RW - 32 bits - [ACPI_USB3.0_REG: 10h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	0h	Reserved
CCU_MODE	15:8	07h	Clock Control Mode This field contains a set of bits which, when set, enable individual features of the clock control unit. Bit 0: Enable Power Control Mode Bit 1: Enable SuperSpeed Remote Wake Mode Bit 2: Enable PCLK Control Mode Bit 3: Enable Memory Sleep Sequencing. Bit 4: Enable Stop Cpu Mode
MEM_DSD_DLY	21:16	10h	RW Memory Sleep Delay Controls the delay applied during memory sleep sequencing.
Reserved	31:22	0h	Reserved

USB2.0_WAKE_CONTROL - RW - 32 bits - [ACPI_USB3.0_REG: 20h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	21:0	0h	Reserved
U2_SE1_DISCON_MODE	23:22	1h	USB2 SE1 Disconnect Mode Enables/Disables whether SE1 is considered as a disconnect. 0: Enable 1: Disable
SYS_BW	25:24	0h	System Bandwidth This field is used to provide information to the controller about the available system bandwidth.
Reserved	31:26	0h	Reserved

USB3.0_ACPI_MMIO_REG24 - RW - 32 bits - [ACPI_USB3.0_REG: 24h]			
Field Name	**Bits**		**Description**
DBESL_CTL	3:0	0h	Default Best Effort Service Latency Control Defines the Read-Only value reflected in xHCI PCI_Reg:62h bits[3:0], DBESL.
DBESLD_CTL	7:4	0h	Default Best Effort Service Latency Deep Control Defines the Read-Only value reflected in xHCI PCI_Reg:62h bits[7:4], DBESLD.
LPM_CLOCK_5US_SEL	8	0h	LPM Clock_5us Select Selects the clock source on which the 5us Hardware Controlled LPM Timer is based from either 5us or 1us. Selecting 1us clock as a base allows the Hardware LPM to properly handle times which are not a multiple of 5us. 0: 5us 1: 1us
DPP_ERR_AS_XACTERR_EN	9	0h	DPP Error as XactErr Enable Controls the way in which a DPP Error is reported. 0: Reported as Babble Error 1: Reported as Xact Error
U2IF_PME_HOLD_EN	10	0h	USB2 PME Hold En Controls whether PME is maintained asserted until the corresponding ‘Change’ bit in the PORTSC register (CSC, OCC, PLC) is cleared. 0: Disable 1: Enable

USB3.0_ACPI_MMIO_REG24 - RW - 32 bits - [ACPI_USB3.0_REG: 24h]			
Field Name	**Bits**		**Description**
U2IF_L1_RWE_MODE	11	0h	USB2 L1 Remote Wake Enable Mode Controls whether Remote Wake will cause an exit from L1 when Remote Wake Enable (RWE) is not set. 0: Exit L1 when RWE==0. 1: Do not exit L1 when RWE==0.
U2IF_S3_CSC_ENH_EN	12	0h	USB2 S3 Connect Status Change Enhancement Enable Enables an enhancement to the connect status change detection during S3. 0: Disable 1: Enable
U2IF_S3_WAKE_MODE	13	0h	USB2 S3 Wake Mode Controls whether a PME will be generated in the following two scenarios.: a. On a connected port with WDE=0, WCE=1, then entering into S3, disconnect the device and then connect a device. b. On a disconnected port with WDE=1, WCE=0, then entering into S3, connect a device and then disconnect the device 0: Set PME in below two scenarios 1: Not set PME in below two scenarios
SSIF_PME_CTL	15:14	0h	SuperSpeed PME and Link Control Controls the manner in which the SuperSpeed interface handles a link event (Connect, Disconnect, Resume) while the system is in the process of shutting down. Bit[14] 0: Disable. 1: Re-generate a PME after system is in S3 if a PME generated in S0 is not handled by SW. Bit[15] 0: Disable. 1: Delay handling of line events on detection of OS going to Sleep until OS gets out of sleep.
HS_DATA_TOGGLE_ERR_MODE	16	0h	High-Speed Data Toggle Error Mode 0: Disable 1: Enable
U2IF_LPM_TE_ST_CLR_EN	17	0h	U2IF LPM_TE_State Clear Enable Controls whether the LPM state machine will return to idle if an existing LPM request is de-asserted. 0: Disable 1: Enable
U2IF_EOR_OPMODE_SEL	18	0h	U2IF OPMODE selection during EOR period Controls the OPMODE value during device L1 Exit recovery period. 0: OPMODE is 2'b00 "NORMAL OPERATION" 1: OPMODE is 2'b10 "DISABLE BITSTUFF and NRZI"
U2IF_HOLD_RESUME_DIS	19	0h	U2IF hold resume in S3 1: Disable 0: Enable
Reserved	31:20	0h	Reserved

USB3.0_ACPI_MMIO_REG28 - RW - 32 bits - [ACPI_USB3.0_REG: 28h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

USB3.0_ACPI_MMIO_REG2C - RW - 32 bits - [ACPI_USB3.0_REG: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

XHCI_1_0_ENABLE - RW - 32 bits - [ACPI_USB3.0_REG: 30h]			
Field Name	**Bits**	**Default**	**Description**
XHCI_1_0_EN	0	0h	xHCI 1.0 Enable Global enable bit for features added in xHCI 1.0. All xHCI 1.0 features may be enabled by setting XHCI_1_0_EN, or can be individually enabled by setting the individual feature enables. 0: Disable 1: Enable all xHCI 1.0 features.
INT_BLOCK_EN	1	0h	Interrupt Blocking Enable Controls whether interrupt blocking is supported. 0: Disable 1: Enable
FSE_EN	2	0h	Force Stopped Event Enable Controls whether the xHCI 1.0 changes to FSE are supported. 0: Disable 1: Enable
SW_LPM_EN	3	0h	Software Controlled LPM Enable Enables xHCI 1.0 changes related to Software Controlled LPM. 0: Disable 1: Enable
HW_LPM_EN	4	0h	Hardware Controlled LPM Enable Enables xHCI 1.0 changes related to Hardware Controlled LPM 0: Disable 1: Enable
Reserved	5	0h	
SKIP_TRB_IOC_EVT_EN	6	0h	Skip TRB IOC Event Enable Enables xHCI 1.0 features related to the parsing of TRBs and generation of events while skipping over TRBs due to errors and short packets. 0: Disable 1: Enable
SBD_CAP_OBSOLETE	7	0b	SBD Reporting Capability Obsolete Enables xHCI 1.0 feature which makes Secondary Bandwidth Domain Reporting mandatory. 0: Disable 1: Enable
CAS_EN	8	0b	Cold Attach Status Enable Enables the xHCI 1.0 feature, the Cold Attach Status flag. 0: Disable 1: Enable

XHCI_1_0_ENABLE - RW - 32 bits - [ACPI_USB3.0_REG: 30h]			
Field Name	**Bits**	**Default**	**Description**
EP_STATE_UPDATE_CHANGE_EN	9	0h	EP State Update Change Enable Enables a clarification in xHCI 1.0 specifying that when an endpoint transitions from Stopped To Running due to a doorbell ring, the EP State shall be updated to Running before any Transfer Events are generated. 0: Disable 1: Enable
SKIP_MS_IOC_EVT_EN	10	0b	Skip Missed-Service IOC Event Enable Enables the parsing of TRBs during re-sync of an iso pipe following detection of a Missed Service Error. Always enable this bit when SKIP_TRB_IOC_EVT_EN (ACPI_USB3.0 0x30[6]) is set. 0: Disable 1: Enable
SOFT_RETRY_EN	11	0b	Soft Retry Enable Enables xHCI 1.0 feature Soft Retry. 0: Disable 1: Enable
USB2_U3EXIT_CHANGE_EN	12	0b	USB2 U3Exit Change Enable Enables the removal of the U3Exit state from USB2 Root Hub Port state machine. 0: Disable 1: Enable
USB3_LINK_CMD_VLD_ERRATA_EN	13	0b	USB3 Link Command Valid Errata Enable Enables a USB3 Errata which modifies the definition of a valid Link Command. 0: Disable 1: Enable
MSE_FRAMEID_EN	14	0	Missed Service Error on Frame ID Enable Enables a clarification in xHCI 1.0 specifying the conditions under which a Missed Service Error should be detected based on Frame ID. 0: Disable 1: Enable
HCIVERSION_1_0_EN	15	0h	Host Controller Interface Version 1.0 Enable Controls the host controller interface version number reported in the HCIVERSION register. 0: 0096h 1: 0100h
TESTMODE_CHANGE_EN	16	0h	TestMode Change Enable Enables changes to the USB2 Root Hub Port state machine regarding Test Mode. 0: Disable 1: Enable
MSE_EVT_TRB_PTR_CTL	17	0b	Missed Service Error Event TRB Pointer Control Controls the value of the TRB Pointer field in a Transfer Event TRB generated while re-synchronizing an iso pipe after a Missed Service Error if a Ring Underrun occurs. [N/A if SKIP_MS_IOC_EVT_EN==0]. 0: TRB Pointer == TRB Dequeue Pointer 1: TRB Pointer == 0
LPM_BROADCAST_DIS	18	0b	LPM Broadcast Disable Controls whether USB2 LPM packets are broadcast to all ports, or only transmitted on the port with the destination device. 0: LPM packet will be broadcast to all ports 1: Disable LPM broadcast Note: LPM_BROADCAST_DISABLE feature is not controlled by the global XHCI_1_0_EN.

XHCI_1_0_ENABLE - RW - 32 bits - [ACPI_USB3.0_REG: 30h]			
Field Name	**Bits**	**Default**	**Description**
HOST_INIT_L1EXIT_BLOCK_DIS	19	0h	Host Initiated L1 Exit Blocking Disable Disables the host controller from not initiating L1 Exit (i.e. enables a host to initiate L1 Exit) under two scenarios described in xHCI 1.0. To ping a HS Bulk Out Endpoint that has returned a NYET for an OUT. To poll an INT In Endpoint which has TD available but has responded with a NAK to a poll. 0: Prevent host initiated L1 Exit. 1: Allow host initiated L1 Exit. Note: HOST_INIT_L1EXIT_BLOCK_DIS is not controlled by the global XHCI_1_0_EN.
STREAM_STALL_MODE	20	0h	Stream Stall Mode Enables the detection of a STALL condition while in the Stream Protocol HISPSM Prime Pipe or HOSPSM Prime Pipe or No Stream state. 0 : Disable 1 : Enable Note: STREAM_STALL_MODE is not controlled by the global XHCI_1_0_EN.
NON_CSTREAM_SID_CHK_MODE	21	0h	Non CStream SID Check Mode Enables the checking for a non-CStream SID in the Move Data state to determine if the pipe shall halt with an Invalid Stream Type Error. 0 : Disable 1 : Enable Note: NON_CSTREAM_SID_CHK_MODE is not controlled by the global XHCI_1_0_EN.
NRDY_PRIME_SID_CHK_MODE	22	0h	NRDY Prime SID Check Mode Enables checking for NRDY with non-Prime SID in the Prime Pipe state. If detected, the pipe shall halt with an Invalid Stream Type Error. 0 : Disable 1 : Enable Note: NRDY_PRIME_SID_CHK_MODE is not controlled by the global XHCI_1_0_EN.
FLA_DEASSERT_EN	23	0h	Force Link PM Accept Deassert Enable Enables a Set Link Function LMP with the Force_LinkPM_Accept bit deasserted to be generated when PORTPMSC.FLA transitions from ‘1’ to ‘0’. 0 : Disable 1 : Enable
SKIP_TRB_IOC_EVT_LEN_MODE	24	0h	Skipped TRB Event Length Mode Controls the value of the TRB Transfer Length field in a Transfer Event TRB for a skipped TRB. 0: Transfer Length == 0. 1: Transfer Length == Residual number of bytes.
HW_LPM_U2ENTRY_PLS_SEL	25	0h	HW LPM U2Entry PLS Select Controls the value of PORTSC.PLS in the U2Entry Root Hub Port state under Hardware Controlled LPM. 0: U0 1: U2 Note: HW_LPM_U2ENTRY_PLS_SEL is not controlled by the global XHCI_1_0_EN.

XHCI_1_0_ENABLE - RW - 32 bits - [ACPI_USB3.0_REG: 30h]			
Field Name	**Bits**	**Default**	**Description**
LPM_BLC_SEL	26	0h	LPM BLC Select Controls the value reported in BESL LPM Capability (BLC) field, and thus the BESL/HIRD Encoding. 0: BLC=1 1: BLC=0 Note: LPM_BLC_SEL is not controlled by the global XHCI_1_0_EN.
LPM_CTRL_IMPROVE	27	0h	LPM Control Improvement Enable Enables improvements in the efficiency with which Control Endpoints are handled in Hardware-Controlled LPM. 0: Disable 1: Enable Note: LPM_CTRL_IMPROVE is not controlled by the global XHCI_1_0_EN.
NO_SFT_RTY_ON_SSTO_EN	28	0h	No Soft Retry on SuperSpeed Timeout Enable Enables a Reset Endpoint command with TSP==1 to fail for an endpoint that was halted due to a Timeout. 0: Disable 1: Enable Note: NO_SFT_RTY_ON_SSTO_EN is not controlled by the global XHCI_1_0_EN.
LPM_HOST_INIT_L1EXIT_RWE_BLK	29	0h	Host Initiated L1 Exit Remote WakeUp Block Enable 0: Disable 1: Enable Note: LPM_HOST_INIT_L1EXIT_RWE_BLK is not controlled by the global XHCI_1_0_EN.
Reserved	31:30	0h	Reserved

USB3.0_ACPI_MMIO_REG34 - RW - 32 bits - [ACPI_USB3.0_REG: 34h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

USB3.0_ACPI_MMIO_REG38 - RW - 32 bits - [ACPI_USB3.0_REG: 38h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

USB3.0_ACPI_MMIO_REG40 - RW - 32 bits - [ACPI_USB3.0_REG: 40h]			
Field Name	**Bits**	**Default**	**Description**
IP_IMPRV_YZ_GLB_EN	0	0h	Host Controller Global Feature Enable Enables a set of 31 minor design enhancements to the host controller. 0: Disable 1: Enable
IP_IMPRV_YZ_IND_DIS	31:1	0h	Host Controller Individual Feature Disable Each bit represents a disable of a minor design enhancement to the host controller, overriding the global enable (IP_IMPRV_YZ_GLB_EN). If IP_IMPRV_YZ_GLB_EN = '0', these 31 bits have no effect. 1: Disable

SSPHY ACPI Indirect Index - RW- 32 bits - [ACPI_USB3.0_REG: 48h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0h	Reserved.
Indirect Index	7:2	0h	Selects SSPHY ACPI Indirect registers. Range: 00h – FCh. Accesses to all the indirect registers are DW (32 bits).
Reserved	31:8	0h	

SSPHY ACPI Indirect Data - RW- 32 bits - [ACPI_USB3.0_REG: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
Indirect Data	31:0	0h	On read: read data from the indexed indirect register. On write: write data to the indexed indirect register.

CCUSSIFREG1_OVERRIDE - RW - 32 bits - [ACPI_USB3.0_REG: 50h]			
Field Name	**Bits**	**Default**	**Description**
CCUSSIFREG1_OVERRIDE	31:0	0h	Set the related bit to 1 to flip ccu ssifreg1 corresponding bit setting

CCUSSIFREG2_OVERRIDE - RW - 32 bits - [ACPI_USB3.0_REG: 54h]			
Field Name	**Bits**	**Default**	**Description**
CCUSSIFREG2_OVERRIDE	31:0	0h	Set the related bit to 1 to flip ccu ssifreg2 corresponding bit setting

CCUSSIFREG3_OVERRIDE - RW - 32 bits - [ACPI_USB3.0_REG: 58h]			
Field Name	**Bits**	**Default**	Description
CCUSSIFREG3_OVERRIDE	31:0	0h	Set the related bit to 1 to flip ccu ssifreg3 corresponding bit setting

CCUU2IFREG1_OVERRIDE - RW - 32 bits - [ACPI_USB3.0_REG: 5Ch]			
Field Name	**Bits**	**Default**	Description
CCUU2IFREG1_OVERRIDE	31:0	0h	Set the related bit to 1 to flip ccu u2ifreg1 corresponding bit setting

SSPHY Common Control 1 – R/W- 32 bits – [ACPI_USB3.0_REG: 90h]			
Field Name	**Bits**	**Default**	**Description**
XX_LEQ_TIME	3:0	5h	Linear equalization config controls. Refer to PHY design document for details.
XX_OC_TIME	7:4	8h	Linear equalization config controls. Refer to PHY design document for details.
XX_CDR_TIME	11:8	9h	Linear equalization config controls. Refer to PHY design document for details.
XX_FOM_TIME	15:12	7h	Linear equalization config controls. Refer to PHY design document for details.

SSPHY Common Control 1 – R/W- 32 bits – [ACPI_USB3.0_REG: 90h]			
Field Name	**Bits**	**Default**	**Description**
XX_DFE_TIME	19:16	5h	Linear equalization config controls. Refer to PHY design document for details.

SSPHY Common Control 3 – R/W- 32 bits – [ACPI_USB3.0_REG: 98h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	29:0	0h	
No_Resume_After_Disconnect_En	30	0h	Enable resume after disconnect_en
Block_LTSSM_Move_To_Polling_En	31	0h	Prevent LTSSM 125M from moving to Polling after the host goes to D0 on S3 wake

SPI BAR0 – R/W- 32 bits – [ACPI_USB3.0_REG: A0h]			
Field Name	**Bits**	**Default**	**Description**
XHC_SPI_data_type0_addr	15:0	0h	Type0 data rom address.
XHC_SPI_data_type0_size	31:16	0h	Type0 data size.

SPI BAR1 – R/W- 32 bits – [ACPI_USB3.0_REG: A4h]			
Field Name	**Bits**	**Default**	**Description**
XHC_SPI_data_type1_addr	15:0	0h	Type1 data rom address.
XHC_SPI_data_type1_size	31:16	0h	Type1 data size.

SPI BAR2 – R/W- 32 bits – [ACPI_USB3.0_REG: A8h]			
Field Name	**Bits**	**Default**	**Description**
xHc_SPI_data_type2_addr	15:0	0h	Type2 data rom address.
xHc_SPI_data_type2_size	31:16	0h	Type2 data size.

SPI BAR3 – R/W- 32 bits – [ACPI_USB3.0_REG: ACh]			
Field Name	**Bits**	**Default**	**Description**
XHC_SPI_data_type3_addr	15:0	0h	Type3 data rom address.
XHC_SPI_data_type3_size	31:16	0h	Type3 data size.

SPI Valid Base – R/W- 32 bits – [ACPI_USB3.0_REG: B0h]			
Field Name	**Bits**	**Default**	**Description**
SPI_BAR0_Vld	0	0h	SPI BAR0 Valid. 1: SPI_BAR0 register is valid
SPI_Base0	7:2	0h	SPI Base0 Offset in SPI data block of type0 data.
SPI_BAR1_Vld	8	0h	SPI BAR1 Valid 1: SPI_BAR1 register is valid.
SPI_Base1	15:10	0h	SPI Base1 Offset in SPI data block of type1 data.
SPI_BAR2_Vld	16	0h	SPI BAR2 Valid 1: SPI_BAR2 register is valid.

SPI Valid Base – R/W- 32 bits – [ACPI_USB3.0_REG: B0h]			
Field Name	**Bits**	**Default**	**Description**
SPI_Base2	23:18	0h	SPI Base2 Offset in SPI data block of type2 data.
SPI_BAR3_Vld	24	0h	SPI BAR3 Valid 1: SPI_BAR2 register is valid.
SPI_Base3	31:26	0h	SPI Base3 Offset in SPI data block of type3 data.

SPI Misc – R/W- 32 bits – [ACPI_USB3.0_REG: B4h]			
Field Name	**Bits**	**Default**	**Description**
XHC_SPI_FW_ID	15:0	0h	SPI Firmware ID Firmware Version ID
Reserved	16:26	0h	
XHC_FRAME_BABBLE_REPORTING_EN	27	0b	XHC U2IF frame babble reporting bit 0: Disable reporting 1: Report frame babble when it has been detected in USB HS/FS/LS bus
CFGA_USB20PHY_FL_SPEED_SEL	28	0b	XHC FL_SPEED selection bit. 1: New RTL implementation 0: Keep the logic that XHC_FL_SPEED_CTRL mode controls
Reserved	31:29	0h	

SPI Data Block N – R/W- 32 bits – [ACPI_USB3.0_REG: C0h/C8h/CCh/D0h/D8h/DCh/E0h/E4h/E8h/ECh/F0h/F4h/F8h/FCh]			
Field Name	**Bits**	**Default**	**Description**
XHC_SPI_Data_Block	31:0	0h	SPI Data Block

2.2.7.3 Indirect ACPI Space (60MHz)

The indirect registers range from 00h – FCh and are used for SuperSpeed PHY configurations that need to be set before XHC core is out of reset. The registers are therefore under 60MHz clock (USB2 PHY common clock). The registers are not reset in low power states. Accesses to the registers are through XHC ACPI registers, 48h/4Ch pair.

000h ~ 03Ch: Reserved for future use.
040h ~ 07Ch: SuperSpeed PHY common registers. This group of registers is shared by all USB3 PHY ports and can occupy up to 16 register locations.
080h ~ 0FCh: SuperSpeed PHY per-port registers. Registers for each port can occupy up to 16 register locations and are grouped together for future extendibility. Port 0 ranges from 080h ~ 0BCh, port 1 0C0h ~ 0FCh.

Register Name	Offset Address
	40h
	44h
SSPHY Port System Control & Power Masks	48h
	4Ch
	50h
	54h
	58h
	80h/C0h 0A0/0E0h
	84h/C4h 0A4/0E4h
	88h/C8h 0A8/0E8
	8Ch/CCh 0AC/0ECh
	90h/D0h 0B0/0F0h
	94h/D4h 0B4/0F4h
	98h/D8h 0B8/0F8h
DbC Control	100h
DbC Control	120h
	124h
DbC Control	128h

SSPHY Port System Control & Power Masks – R/W- 32 bits – [ACPI_Ind_Reg:048h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0		
D3_RST125_GATE	1	0b	125MHz Reset to SuperSpeed PHY IF gated with D3 Controls whether the SuperSpeed PHY Interface is reset during D3. When enabled, the reset is gated/blocked during D3. 0: Disable 1: Enable
Reserved	13:2		
PHYSTATUS_U1XX_EN	14	1b	PHYSTATUS U1 Exit Latency Control Controls the condition under which PHYSTATUS signals an exit from U1. When enabled, PHYSTATUS U1 Exit Latency will be reduced. 0: Disable 1: Enable.
Reserved	31:15		

DbC Control – R/W- 32 bits – [ACPI_Ind_Reg:100h]			
Field Name	**Bits**	**Default**	**Description**
DEBUG_CAP_EN	0	0h	Debug Capability Enable 0: Disable 1: Enable
DCP_HALT_RSTSM_OFF_EN	1	0h	Enable bit to turn off the function that resets the DMA sub state machines when HIT/HOT is set. 1: DbC DMA sub state machines won't be reset to IDLE state on the posedge of HIT/HOT. 0: DbC DMA sub state machines will be reset to IDLE state on the posedge of HIT/HOT.
DCP_DBC_DPH_CHK_EN	2	0h	Enable bit to check if a DPH comes before data buffer is ready and then be treated as invalid DPH by the data buffer controller. 0: Disable 1: Enable
DCP_ERDY_ON_HALT_EN	3	0h	Enable bit to support send ERDY to host machine once DbC detects HIT/HOT is set when it is in flow control. 0: Disable 1: Enable
DCP_HALT_BLOCK_EN	4	0h	Enable bit to block HIT/HOT from being seen by the logic until the current service interval is done. 0: Disable 1: Enable
Reserved	7:5	0h	
DCP_MAX_BURST_SIZE	15:8	0h	This field should be set to 0h since only single transfer is supported by DbC.
DCP_TRNS_CMP_CTL	19:16	0h	DbC transmission completion condition control. DbC IN and OUT endpoint stream info DW0 bit[29:26] is driven by this field. 0000b: Execute up to TD boundary 0001b: Execute up to Max Burst 0010b: Single transfer Others: Reserved
DCP_EVT_THROTTLE_EN	20h	0h	Enable bit for DbC event throttle. When set to ‘1’, DbC event request can not assert to request grant from the event write DMA arbitration. By this way, we can make DbC event fifo full for verification use.
DCP_EPST_CLR_EN	21	0h	Enable bit to clear EP state to DISABLE when DCR is cleared. 0: Disable 1: Enable
Reserved	31:22	0h	

DbC Control – R/W- 32 bits – [ACPI_Ind_Reg:120h]			
Field Name	**Bits**	**Default**	**Description**
DCP_U1_ENABLE	0	0h	Enable bit for U1 Entry When set to '1', enable U1 entry. When cleared to '0', disable U1 entry, link cannot enter U1.
DCP_U2_ENABLE	1	0h	Enable bit for U2 Entry When set to '1', enable U2 entry. When clear to '0', disable U2 entry, link can not enter U2.
Reserved	2	0h	
DCP_INACTIVE_TO_RXDETECT	3	0h	Enable bit to let LTSSM move to Rx.Detect from SS. Inactive when DCE transitions from '0' to '1' 1: Enable 0: Disable
Reserved	31:4	0h	

DbC Control – R/W- 32 bits – [ACPI_Ind_Reg:128h]			
Field Name	**Bits**	**Default**	**Description**
DCP_REMOTE_WAKE_EN	0	0h	DbC remote wake up 0: Disable 1: Enable
Reserved	31:1	0h	

2.2.8 USB 3.0 Registers (XHC0/XHC1, Device-16 func-0 & func-1) (Not supported on Bolton-D2)

2.2.8.1 XHCI PCI Configuration Registers

XHCI0 and XHCI1 are PCIe Root Complex Integrated Endpoints, so the PCI Configuration space includes Header, Capabilities and Extended Capabilities.

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID / Class Code	08h
Miscellaneous	0Ch
BAR_0	10h
BAR_1	14h
Subsystem Vendor ID / Subsystem ID	2Ch
Capability Pointer	34h
Interrupt Line	3Ch
IDP Index	40h
IDP DATA	44h
Indirect PCI Index	48h
Indirect PCI Data	4Ch
PME Control	50h
PME Control / Status	54h
SBRN	60h
FLADJ	61h

Register Name	Offset Address
DBESL/DBESLD	62h
MSI Control	70h
MSI Address	74h
MSI Upper Address	78h
MSI Data	7Ch
MSI Mask Bits	80h
MSI-X Control	90h
MSI-X Table Offset/Table BIR	94h
MSI-X PBA Offset/PBA BIR	98h
PCIE Capability List/Register	A0h
Device Capability Register	A4h
Device Control/Status Register	A8h
Device Capabilities 2 Register	C4h
Device Control/Status 2 Register	C8h
SP Registers [0 to 7]	E0h-FFh
LTR Extended Capability Header	100h
Max Snoop Latency Register	104h
Max No-Snoop Latency Register	106h

Vendor ID – R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Vendor Identifier.

Device ID – R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0		Device Identifier.

Command – RW - 16 bits - [PCI_Reg:04h]				
Field Name	**Bits**	**Default**	**Type**	**Description**
IO Space Accesses	0	0b	Read Only	0: Disable the device response. 1: Allow the device to respond to I/O Space accesses. Hard-wired to 0.
Memory Space Accesses	1	0b	Read/Write	0: Disable the device response. 1: Allow the device to respond to Memory Space accesses.
Bus Master	2	0b	Read/Write	0: Disable the device from generating PCI accesses. 1: Allow the device to behave as a bus master.
Special Cycle	3	0b	Read Only	Hard-wired to 0, indicating no Special Cycle support.
Memory Write and Invalidate Command	4	0b	Read Only	0: Memory Write must be used. 1: Masters may generate the command. Hard-wired to 0.
VGA Palette Register Accesses	5	0b	Read Only	Hard-wired to 0, indicating the device should treat palette write accesses like all other accesses.
Parity Enable	6	0b	Read/Write	0: the device sets its Detected Parity Error status bit (bit [15] in the Status register) when an error is detected, but continues normal operations without asserting PERR#. 1: The device must take its normal action when a parity error is detected.
Reserved	7	0b	Read Only	Hard-wired to 0 per PCI3.0 spec.

Command – RW - 16 bits - [PCI_Reg:04h]				
Field Name	**Bits**	**Default**	**Type**	**Description**
SERR# Enable	8	0b	Read/Write	0: Disable the SERR# driver. 1: Enable the SERR# driver. Note: Address parity errors are reported only if this bit and bit [6] are 1.
Fast Back-to-Back Enable	9	0b	Read Only	0: Only fast back-to-back transactions to the same agent are allowed. 1: The master is allowed to generate fast back-to-back transactions to different agents. Hard-wired to 0.
Interrupt Disable	10	0b	Read/Write	0: Enable the assertion of the device/function's INTx# signal. 1: Disable the assertion of the device/function's INTx# signal.
Reserved	15:11	0h	Read Only	Reserved

Status – R - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0		Reserved
Interrupt Status	3	0b	This bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0, and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
Capabilities List	4	1b	0: Indicates that no New Capabilities linked list is available. 1: Indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities. Hard-wired to 1.
66 MHz Capable	5	0b	This optional read-only bit indicates whether or not this device is capable of running at 66 MHz. Hard-wired to 0.
Reserved	6		Reserved.
Fast Back-to-Back Capable	7	0b	Hard-wired to 0.
Master Data Parity Error	8	0b	This bit is set when any of the following three conditions is met: (1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); (2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit (Command register) is set.
DEVSEL Timing	10:9	00b	Hard-wired to 00b.
Signaled Target Abort	11	0b	This bit is set by a target device whenever it terminates a transaction with Target-Abort.
Received Target Abort	12	0b	This bit is set by a master device whenever its transaction is terminated with Target-Abort.
Received Master Abort	13	0b	This bit is set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort.
Signaled System Error	14	0b	This bit is set whenever the device asserts SERR#.
Detected Parity Error	15	0b	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit [6] in the Command register).

Revision ID / Class Code – R - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	08h	Revision ID.
Programming Interface	15:8	30h	Programming Interface. USB 3.0 Host Controller that conforms to XHC specification.
Sub Class	23:16	03h	Sub Class. Universal Serial Bus Host Controller.
Base Class	31:24	0Ch	Base Class. Serial Bus Controller.

Miscellaneous – RW - 32 bits - [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	RW This read/write field specifies the system cache line size in units of DWORDs and must be initialized to 00h.
Latency Timer	15:8	00h	RO For PCI device, Bits [9:8] are hard-wired to 00b, resulting in a timer granularity of at least four clocks. This field specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. Hard-wired to 00h.
Header Type	23:16	00h	RO This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space), and also whether or not the device contains multiple functions. XHC0: Bit [23] hard-wired to 1b. The device has multiple functions. This field read as 80h. XHC1: Bit [23] hard-wired to 0b. This field read as 00h. Bits [22:16] hard-wired to 00h.
BIST	31:24	00h	RO Hard-wired to 00h, indicating no build-in BIST support.

Bar_0 – RW - 32 bits - [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
IND	0	0b	RO Indicator. Read Only. A constant value of 0 indicates that the operational registers of the device are mapped into memory space of the main memory of the PC host system. Hard-wired to 0b.
TP	2:1	10b	RO Type. Read Only. 00: 32bit address 10: 64bit address Hard-wired to 10b.
PM	3	0b	RO Prefetch memory. Read Only. A constant value of 0 indicates that there is no support for “prefetchable memory”. Hard-wired to 0b.
BAR_0	31:4	0h	RW Base Address.

Bar_1 – RW - 32 bits - [PCI_Reg:14h]			
Field Name	**Bits**	**Default**	**Description**
BAR_1	31:0	0h	Upper 32 bits of Base Address.

Subsystem Vendor ID / Subsystem ID – RW - 32 bits - [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	1022h	Subsystem Vendor ID
Subsystem ID	31:16	7812h	Subsystem ID

Capability Pointer – R - 8 bits - [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capability Pointer	7:0	50h	Address of the 1st element of capability link.

Interrupt Line – RW – 32 bits - [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	RW The Interrupt Line register is an eight-bit register used to communicate interrupt line routing information. The register is read/write and must be implemented by any device (or device function) that uses an interrupt pin. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value; rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.
Interrupt Pin	15:8	01h	RO The Interrupt Pin register tells which interrupt pin the device (or device function) uses. A value of 1 corresponds to INTA#.
Reserved	31:16	00h	

IDP Index Register – RW- 32 bits – [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved.
IDP Index	12:2	00h	This register selects the DWord offset of the memory mapped register to be accessed.
Reserved	31:13	000000h	Reserved.

IDP Data Register – RW- 32 bits – [PCI_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
IDP Data	31:0		This register is a “window” through which data is read or written to the memory mapped register pointed to by the IDP Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by IDP Index. All register accesses to Data are DWord granularity.

Indirect PCI Index Register – RW- 32 bits – [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved.
Indirect PCI Index	15:2	00h	The upper 2 bits (Bit[31:30]) select the Indirect space. 00: 125Mhz PCI IND space 01: 60Mhz PCI IND space. 10: Reserved 11: Reserved The lower 14 bits (Bit[15:2]) selects the Dword offset of the Indirect PCI space register to be accessed. 0000_0000h-0000_FFFFh : 125Mhz PCI IND space 4000_0000h-4000_FFFFh : 60Mhz PCI IND space
Reserved	31:16	0000h	

Indirect PCI Data Register – RW- 32 bits – [PCI_Reg:4Ch]			
Field Name	**Bits**	**Default**	**Description**
Indirect PCI Data	31:0		This register is a “window” through which data is read or written to the Indirect PCI space register pointed to by the Indirect PCI Index register. Note that a physical register is not actually implemented as the data is actually stored in the Indirect PCI space registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by Indirect PCI Index. All register accesses to Data are DWord granularity.

PME Control – RO - 32 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
Cap_ID	7:0	01h	(Read Only) A value of 01h identifies the linked list item as being the PCI Power Management registers.
Next Item Pointer	15:8	70h	(Read Only) This field provides an offset into the function’s PCI Configuration Space, pointing to the location of next item in the function’s capability list. If there are no additional items in the Capabilities List, this register is set to 00h.
Version	18:16	011b	(Read Only) A value of 011b indicates that this function complies with Revision 1.2 of the PCI Power Management Interface Specification.
PME clock	19	0b	(Read Only) When this bit is 0, it indicates that no PCI clock is required for the function to generate PME#.
Reserved	20		Reserved
DSI	21	0b	(Read Only) This Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it.

PME Control – RO - 32 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
Aux_Current	24:22	000b	(Read Only) This 3 bit field reports the 3.3V auxiliary current requirements for the PCI function. If the Data Register has been implemented by this function, then: - Reads of this field must return a value of 000b. - The Data Register takes precedence over this field for 3.3V auxiliary current requirement reporting.
D1_Support	25	0b	If this bit is a 1, this function supports the D1 Power Management State.
D2_Support	26	0b	If this bit is a 1, this function supports the D2 Power Management State.
PME_Support	31:27	19h	(Read Only) This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit [31] 1XXXXb - PME# can be asserted from D3cold Bit [30] X1XXXb - PME# can be asserted from $D3_{hot}$ Bit [29] XX1XXb - PME# can be asserted from D2 Bit [28] XXX1Xb - PME# can be asserted from D1 Bit [27] XXXX1b - PME# can be asserted from D0

PME Control / Status – RW - 32 bits - [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	Description
PowerState	1:0	00b	This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given by: 00b: D0 01b: D1 10b: D2 11b: $D3_{hot}$ If software attempts to write an unsupported, optional state to this field, the write operation must be completed normally on the bus; however, the data is discarded and no state change occurs.
Reserved	2		Reserved

PME Control / Status – RW - 32 bits - [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	Description
No_Soft_Reset	3	1b	(Read Only) When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When cleared (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 uninitialized with only PME context preserved if PME is supported and enabled.
Reserved	7:4	0000b	
PME_En	8	0b	A “1” enables the function to assert PME#. When 0, PME# assertion is disabled. This bit defaults to 0 if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
Data_Select	12:9	0000b	(Read Only) This 4-bit field is used to select which data is to be reported through the Data register and Data_Scale field.
Data_Scale	14:13	00b	(Read Only) This 2-bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field will vary depending on which data value has been selected by the Data_Select field.
PME_Status	15	0b	(RW1C) This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. Writing a “1” to this bit will clear it and cause the function to stop asserting a PME# (if enabled). Writing a “0” has no effect. This bit defaults to 0 if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
Reserved	21:16		Reserved
B2_B3#	22	0b	(Read Only) The state of this bit determines the action that is to occur as a direct result of programming the function to D3hot. A 1 indicates that when the bridge function is programmed to D3hot, its secondary bus’s PCI clock will be stopped (B2).

PME Control / Status – RW - 32 bits - [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	Description
BPCC_En	23	0b	(Read Only) A “0” indicates that the bus power/clock control policies are disabled. When the Bus Power/Clock Control mechanism is disabled, the bridge’s PMCSR PowerState field cannot be used by the system software to control the power or clock of the bridge’s secondary bus.
Data	31:24	00h	(Read Only) This field is used to report the state dependent data requested by the Data_Select field. The value of this field is scaled by the value reported by the Data_Scale field.

SBRN – RO - 8 bits - [PCI_Reg:60h]			
Field Name	**Bits**	**Default**	**Description**
SBRN	7:0	30h	Serial Bus Specification Release Number. This register contains the release of the Universal Serial Bus Specification with which this Universal Serial Bus Host Controller module is compliant. Hard-wired to 30h.

FLADJ – RW - 8 bits - [PCI_Reg:61h]			
Field Name	**Bits**	**Default**	**Description**
FLADJ	5:0	20h	Frame Length Timing Value. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF microframe length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# HS bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) … 59984 31 (1Fh) 60000 32 (20h) … 60480 62 (3Eh) 60496 63 (3Fh)
Reserved	7:6	00b	

DBESL/DBESLD – RO - 8 bits - [PCI_Reg:62h]			
Field Name	**Bits**	**Default**	**Description**
Default Best Effort Service Latency (DBESL)	3:0	0h	Vendor defined If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field.
Default Best Effort Service Latency - Deep (DBESLD)	7:4	0h	Vendor defined. If the value of this field is non-zero, it defines the recommended value for programming the PORTHLPMC register BESLD field.

MSI Control – RW - 32 bits - [PCI_Reg:70h]			
Field Name	**Bits**	**Default**	**Description**
Capability	7:0	05h	MSI USB ID. Read only.
Next Item Pointer	15:8	90h	Pointer to next capability structure
MSI Enable	16	0b	If “1”, the function is permitted to use MSI to request service and is prohibited from using its INTx# pin. System configuration software sets this bit to enable MSI. If “0”, the function is prohibited from using MSI to request service.
Multiple Message Capable	19:17	011b	(Read Only) System software reads this field to determine the number of requested messages. “011” == 8 messages requested
Multiple Message Enable	22:20	0h	System software writes to this field to indicate the number of allocated messages. Encoding # of messages allocated 000 1 001 2 010 4 011 8 100 16 101 32 110 Reserved 111 Reserved
64-bit Address Capable	23	1b	(Read Only) If “1”, the function is capable of sending a 64-bit message address. If “0”, the function is not capable of sending a 64-bit message address.
Per-vector masking capable	24	0b	(Read Only) If “1”, the function supports MSI per-vector masking. If “0”, the function does not support MSI per-vector masking.
Reserved	31:25	00h	Reserved

MSI Address – RW - 32 bits - [PCI_Reg : 74h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	2’b00	
MSI Address	31:2	0h	System-specified message address.

MSI Upper Address – RW - 32 bits - [PCI_Reg:78h]			
Field Name	**Bits**	**Default**	**Description**
MSI Upper Address	31:0	0h	System-specified message upper address. If the Message Enable bit (bit 0 of the Message Control register) is set, the contents of this register (if non-zero) specify the upper 32-bits of a 64-bit message address (AD[63:32]). If the contents of this register are zero, the device uses the 32-bit address specified by the message address register.

MSI Data – RW - 16 bits - [PCI_Reg: 7Ch]			
Field Name	**Bits**	**Default**	**Description**
MSI Data	15:0	0h	System-specified message

MSI Mask Bits – RW - 32 bits - [PCI_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Mask Bits	31:0	0h	For each Mask bit that is set, the function is prohibited from sending the associated message.

MSI-X Control – RW/RO - 32 bits - [PCI_Reg:90h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	11h	(Read Only) MSI-X capable.
Next Item Pointer	15:8	A0h	(Read Only) Pointer to next capability structure
Table Size	26:16	07h	(Read Only) System software reads this field to determine the MSI-X Table Size N, which is encoded as N-1.
Reserved	29:27	000b	
Function Mask	30	0b	(Read/Write) If 1, all of the vectors associated with the function are masked, regardless of their per-vector Mask bit states. If 0, each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per-vector Mask bits. This bit's state after reset is 0 (unmasked).
MSI-X Enable	31	0b	(Read/Write) If 1 and the MSI Enable bit in the MSI Message Control register is 0, the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin (if implemented). System configuration software sets this bit to enable MSI-X. A device driver is prohibited from writing this bit to mask a functions service request. If 0, the function is prohibited from using MSI-X to request service. This bit's state after reset is 0 (MSI-X is disabled).

MSI-X Table Offset/Table BIR – RO - 32 bits - [PCI_Reg: 94h]			
Field Name	**Bits**	**Default**	**Description**
Table BIR	2:0	000b	Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the functions MSI-X Table into Memory Space. For a 64-bit Base Address register, the Table BIR indicates the lower DWORD. BIR Value — Base Address Register 0 — 10h 1 — 14h 2 — 18h 3 — 1Ch 4 — 20h 5 — 24h 6 — Reserved 7 — Reserved
Table Offset	31:3	200h	Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower 3 Table BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset.

MSI-X PBA Offset/PBA BIR – RO - 32 bits - [PCI_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
PBA BIR	2:0	000b	Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the functions MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the MSI-X Table BIR.
PBA Offset	31:3	210h	Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset.

PCIE Capability List/Register – RO - 32 bits - [PCI_Reg:A0h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	10h	PCI Express Capability
Next Item Pointer	15:8	00h	No other items exist in the linked list of capabilities.
Capability Version	19:16	0010b	Indicates PCI-SIG defined PCI Express Capability structure version number. 2h stand for PCI Express Base Rev 2.0.
Device/Port Type	23:20	1001b	1001b indicates Root Complex Integrated Endpoint.

PCIE Capability List/Register – RO - 32 bits - [PCI_Reg:A0h]			
Field Name	**Bits**	**Default**	**Description**
Slot Implemented	24	0b	When Set, this bit indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled). This field is valid for the following PCI Express Device/Port Types: - Root Port of PCI Express Root Complex - Downstream Port of PCI Express Switch Hard-wired to 0.
Interrupt Message Number	29:25	0h	This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure.
Reserved	31:30	00b	

Device Capability Register – RO - 32 bits - [PCI_Reg:A4h]			
Field Name	**Bits**	**Default**	**Description**
Max_Payload_Size Supported	2:0	000b	This field indicates the maximum payload size that the Function can support for TLPs. Defined encodings are: 000b: 128 bytes max payload size 001b: 256 bytes max payload size 010b: 512 bytes max payload size 011b: 1024 bytes max payload size 100b: 2048 bytes max payload size 101b: 4096 bytes max payload size 110b: Reserved 111b: Reserved The Functions of a multi-function Function device are permitted to report different values for this field.
Phantom Functions Supported	4:3	00b	No Function Number bits are used for Phantom Functions.
Extended Tag Field Supported	5	0b	This bit indicates the maximum supported size of the Tag field as a Requester. 0: 5-bit Tag field supported.
Endpoint L0s Acceptable Latency	8:6	111b	This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. It is essentially an indirect measure of the Endpoints internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L0s entry can be used with no loss of performance. 111b: No limit.

Device Capability Register – RO - 32 bits - [PCI_Reg:A4h]			
Field Name	**Bits**	**Default**	**Description**
Endpoint L1 Acceptable Latency	11:9	111b	This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L1 Acceptable Latency number to compare against the L1 Exit Latencies reported (see below) by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L1 entry can be used with no loss of performance. 111b: No limit.
Reserved	14:12	000b	
Role-Based Error Reporting	15	1b	When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for *PCI Express Base Specification, Revision 1.0a*, and later incorporated into *PCI Express Base Specification, Revision 1.1*.
Reserved	17:16	00b	
Captured Slot Power Limit Value (Upstream Ports only)	25:18	0h	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit Message or hardwired to 00h.
Captured Slot Power Limit Scale (Upstream Ports only)	27:26	00b	Specifies the scale used for the Slot Power Limit Value. Range of Values: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x This value is set by the Set_Slot_Power_Limit Message or hardwired to 00b.
Function Level Reset Capability	28	0b	A value of 1b indicates the Function supports the optional Function Level Reset mechanism. This field applies to Endpoints only. For all other Function types this bit must be hardwired to 0b.
Reserved	31:29	000b	

Device Control/Status Register – RW - 32 bits - [PCI_Reg:A8h]			
Field Name	**Bits**	**Default**	**Description**
Correctable Error Reporting Enable	0	0b	This bit, in conjunction with other bits, controls sending ERR_COR Messages
Non-Fatal Error Reporting Enable	1	0b	This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages
Fatal Error Reporting Enable	2	0b	This bit, in conjunction with other bits, controls sending ERR_FATAL Messages
Unsupported Request Reporting Enable	3	0b	This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending Error Messages
Enable Relaxed Ordering	4	1b	If this bit is set, the Function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester.

Device Control/Status Register – RW - 32 bits - [PCI_Reg:A8h]			
Field Name	**Bits**	**Default**	**Description**
Max_Payload_Size	7:5	000b	This field sets maximum TLP payload size for the Function. As a Receiver, the Function must handle TLPs as large as the set value; As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register Defined encodings for this field are: 000b: 128 bytes max payload size 001b: 256 bytes max payload size 010b: 512 bytes max payload size 011b: 1024 bytes max payload size 100b: 2048 bytes max payload size 101b: 4096 bytes max payload size 110b: Reserved 111b: Reserved Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.
Extended Tag Field Enable	8	0b	(Read Only) When Set, this bit enables a Function to use an 8-bit Tag field as a Requester. If the bit is Clear, the Function is restricted to a 5-bit Tag field. Hard-wired to 0.
Phantom Functions Enable	9	0b	(Read Only) When Set, this bit enables a Function to use unclaimed Functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is Cleared, the Function is not allowed to use Phantom Functions Hard-wired to 0.
Auxiliary (AUX) Power PM Enable	10	0b	When Set, this bit enables a Function to draw AUX power independent of PME AUX power. Functions that require AUX power on legacy operating systems should continue to indicate PME AUX power requirements. AUX power is allocated as requested in the AUX_Current field of the Power Management Capabilities register (PMC), independent of the PME_En bit in the Power Management Control/Status register (PMCSR). For multi-function Function devices, a component is allowed to draw AUX power if at least one of the Functions has this bit set. Note: Function that consume AUX power must preserve the value of this sticky register when AUX power is available. In such Function, this register value is not modified by Conventional Reset.
Enable No Snoop	11	1b	If this bit is Set, the Function is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Note that setting this bit to 1b should not cause a Function to blindly set the No Snoop attribute on all transactions that it initiates. Even when this bit is set, a Function is only permitted to set the No Snoop attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system.

Device Control/Status Register – RW - 32 bits - [PCI_Reg:A8h]			
Field Name	**Bits**	**Default**	**Description**
Max_Read_Request_Size	14:12	010b	This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. 010b: 512 bytes maximum Read Request size
Initiate Function Level Reset	15	0b	A write of 1b initiates Function Level Reset to the Function. The value read by software from this bit is always 0b.
Correctable Error Detected	16	0b	(RW1C) This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Correctable Error Mask register.
Non-Fatal Error Detected	17	0b	(RW1C) This bit indicates status of non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-function device, each function indicates status of errors as perceived by the respective function. For function supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.
Fatal Error Detected	18	0b	(RW1C) This bit indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. For Function supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register.
Unsupported Request Detected	19	0b	(RW1C) This bit indicates that the Function received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function.
AUX Power Detected	20		(Read Only) Function that require AUX power report this bit as Set if AUX power is detected by the Function
Transactions Pending	21	0b	(Read Only) When Set, this bit indicates that the Function has issued Non-Posted Requests which that have not been completed. A Function reports this bit cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
Reserved	31:22	0h	

Device Capabilities 2 Register –RW - 32 bits - [PCI_Reg:C4h]			
Field Name	**Bits**	**Default**	**Description**
Completion Timeout Ranges Supported	3:0	0h	HwInit. This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is reserved and must be hardwired to 0000b.
Completion Timeout Disable Supported	4	1b	(Read Only) A value of 1b indicates support for the Completion Timeout Disable mechanism.
Reserved	10:5	0h	
LTR Mechanism Supported	11	1b	(Read Only) A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. Root Ports, Switches and Endpoints are permitted to implement this capability. For a multi-Function device associated with an Upstream Port, each Function must report the same value for this bit. For Bridges, Downstream Ports, and components that do not implement this capability, this bit must be hardwired to 0b.
Reserved	31:12	0h	

Device Control/Status 2 Register – RW - 32 bits - [PCI_Reg:C8h]			
Field Name	**Bits**	**Default**	**Description**
Completion Timeout Value	3:0	0h	In device Functions that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is reserved and must be hardwired to 0000b. A Function that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50 s to 50 ms. Functions that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Ranges Supported field.
Completion Timeout Disable	4	0b	When Set, this bit disables the Completion Timeout mechanism. This bit is required for all Functions that support the Completion Timeout Disable Capability. Functions that do not support this optional capability are permitted to hardwire this bit to 0b
Reserved	9:5	0h	

Device Control/Status 2 Register – RW - 32 bits - [PCI_Reg:C8h]			
Field Name	**Bits**	**Default**	**Description**
LTR Mechanism Enable	10	0b	When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For a Multi-Function device associated with an Upstream Port of a device that implements LTR, the bit in Function 0 is RW, and only Function 0 controls the components Link behavior. In all other Functions of that device, this bit is Reserved. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status.
Reserved	31:11	0h	

SP Register 0 – RO - 32 bits [PCI_Reg:E0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	1FFCh	Reserved

SP Register 1 – RO - 32 bits [PCI_Reg:E4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

SP Register 2 – RO - 32 bits [PCI_Reg:E8h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

SP Register 3 – RO - 32 bits [PCI_Reg:ECh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

SP Register 4 – RO - 32 bits [PCI_Reg:F0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

SP Register 5 – RO - 32 bits [PCI_Reg:F4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

SP Register 6 – RO - 32 bits [PCI_Reg:F8h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

SP Register 7 – RO - 32 bits [PCI_Reg:FCh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

LTR Extended Capability Header– RO - 32 bits - [PCI_Reg:100h]			
Field Name	**Bits**	**Default**	**Description**
PCI Express Extended Capability ID	15:0	18h	(Read Only) Extended Capability ID for Latency Tolerance is 0018h. For a multi-Function device associated with the Upstream Port of a component that implements LTR, this Capability structure must be implemented only in Function 0, and must control the components Link behavior on behalf of all the Functions of the device.
Capability Version	19:16	1h	(Read Only)
Next Capability Offset	31:20	0h	(Read Only) No other items exist in the linked list of Capabilities.
Note: Only applies to Function 0. Reserved for other Functions.			

Max Snoop Latency Register – RW - 16 bits - [PCI_Reg:104h]			
Field Name	**Bits**	**Default**	**Description**
Max Snoop Latency Value	9:0	0h	Along with the Max Snoop Latency Scale field, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less.
Max Snoop Latency Scale	12:10	000b	This register provides a scale for the value contained within the Maximum Snoop Latency Value field. Encoding is the same as the Latency Scale fields in the LTR Message.
Reserved	15:13	0h	
Note: Only applies to Function 0. Reserved for other Functions.			

Max No-Snoop Latency Register – RW - 16 bits - [PCI_Reg:106h]			
Field Name	**Bits**	**Default**	**Description**
Max No-Snoop Latency Value	9:0	0h	Along with the Max No-Snoop Latency Scale field, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platforms maximum supported latency or less.
Max No-Snoop Latency Scale	12:10	0h	This register provides a scale for the value contained within the Max No-Snoop Latency Value field. Encoding is the same as the Latency Scale fields in the LTR Message.
Reserved	15:13	0h	
Note: Only applies to Function 0. Reserved for other Functions.			

2.2.8.2 Indirect PCI Space

PCI Configuration registers "Indirect PCI Index" and "Indirect PCI Data" (48h/4Ch) define an address/data port through which a set of registers can be accessed.

The upper 2 bits of "Indirect PCI Index" selects indirect space.

00: 125Mhz register space
01: 60Mhz register space
10: Reserved
11: Reserved

The lower 16 bits of “Indirect PCI Index”is the DWord offset of the register to be accessed.

Thus the address range is as below:
0000_0000h ~ 0000_FFFFh : 125Mhz Indirect Space
0001_0000h ~ 3FFF_FFFFh : Reserved
4000_0000h ~ 4000_FFFFh : 60Mhz Indirect Space
4001_0000h ~ FFFF_FFFFh: Reserved

2.2.8.2.1 125Mhz Indirect Space

Registers 40h - 13Ch are reserved for SuperSpeed PHY registers.
40h ~ 58h: SuperSpeed PHY common registers. This group of register is shared by XHC controllers.
80h ~ 13Ch: SuperSpeed PHY per-port registers. Registers for each port occupy 16 register locations and are grouped together for future extendibility. Port 0 ranges from 080h ~ 0BCh, port 1 0C0h ~ 0FCh, …

Register Name	Offset Address
CFGU_AMD_REG00	00h
CFGU_AMD_REG04	04h
Port Disable Write Once	08h
Port Disable RW	0Ch
Usb_DClk_EventCnt0Lo	10h
Usb_DClk_EventCnt1Lo	14h
Usb_DClk_EventCntSel	18h
Usb_DClk_EventCnt0Hi	1Ah
Usb_DClk_EventCnt1Hi	1Bh
Usb_DClk_EventCntCtl	1Ch
	20h
	24h
	28h
	2Ch
	080h/0C0h
	084h/0C4h
	088h/0C8h
	08Ch/0CCh
	090h/0D0h
	094h/0D4h
	098h/0D8h

CFGU_AMD_REG00h – RW - 32 bits - [Ind_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
CFGU AMD REG 64h	15:0	00h	
Reserved	31:16	00h	Reserved

CFGU_AMD_REG04h – RW - 32 bits - [Ind_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	11h	AMD revision ID. 11h: A11
CFG_WRITE_ONCE_LOCK	8	0b	Write once lock bit for Vendor ID, Device ID, Subsystem Vendor ID, Subsystem ID, and IDP path. When the BIOS done, it sets the lock bit. So the registers locked by this bit wouldn't be programmable through PCI/JTAG path.
FLR_EN	9	0b	Set to 1 to enable FLR support. When this bit is 0, FLR capability read back as 0, and writing to Initiate Function Level Reset will not initiate a function level reset.
FLR_MODE	10	0b	Set to 1 to enable Firmware assistant when doing FLR. When this bit is 0, when doing FLR, XHC will send out SMI and set ACPI MMIO space 0xB4[17:16], the XHC FLR SMI Status bit.
Reserved	15:11	00h	
XHC Port_0_OverCurrentControl	19:16	1111b	This register controls the OverCurrent pin mapping for port-0. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7). 0000: USB_OC0# 0001: USB_OC1# 0010: USB_OC2# 0011: USB_OC3# 0100: USB_OC4# 0101: USB_OC5# 0110: USB_OC6# 0111: USB_OC7# Any value greater than 0x7h will disable the OverCurrent function for port-0.
XHC Port_1_OverCurrentControl	23:20	1111b	This register controls the OverCurrent pin mapping for port -1. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-1. 0000: USB_OC0# 0001: USB_OC1# 0010: USB_OC2# 0011: USB_OC3# 0100: USB_OC4# 0101: USB_OC5# 0110: USB_OC6# 0111: USB_OC7# Any value greater than 0x7h will disable the OverCurrent function for port-0.
Reserved	31:24	00h	

Port Disable Write Once – RW - 32 bits - [Ind_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
XHC Port Disable Write Once	1:0	00h	When these bits are set, the corresponding ports are disabled. For example, if bit [0] is set then port-0 (its corresponding port) is disabled; if bit [1] is set, then its corresponding port (port-1) is disabled. Only value 1 can be written into the register, the bit can be cleared to 0 by system reset (PciRst#). That is, when the bit is set to 1, the value is locked and cannot be cleared by any software write. Only writing value 1 takes effect on the register value, and software writing 0 has no effect. The register can only be cleared by hardware reset.
Reserved	31:2	00h	

Port Disable RW– RW - 32 bits - [Ind_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
XHC Port Disable RW	1:0	00h	When these bits are set, the corresponding ports are disabled. For example, if bit [0] is set then port-0 (its corresponding port) is disabled; if bit [1] is set, then its corresponding port (port-1) is disabled. This register field is writable. The final XHC Port Disable signal is the “OR” of “XHC Port Disable Write Once” at Ind_reg 08h and “XHC Port Disable RW” at Ind_reg 0Ch.
Reserved	31:2	0h	

Usb_DClk_EventCnt0Lo – R – 32 bits – [Ind_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
Usb_DClk_EventCnt0Lo	31:0	0h	Usb DClk Event Counter 0[31:0]

Usb_DClk_EventCnt1Lo – R – 32 bits – [Ind_Reg:14h]			
Field Name	**Bits**	**Default**	**Description**
Usb_DClk_EventCnt1Lo	31:0	0h	Usb DClk Event Counter 1[31:0]

Usb_DClk_EventCntSel – RW – 32 bits – [Ind_Reg:18h]			
Field Name	**Bits**	**Default**	**Description**
Usb_DClk_EventSel0	7:0	00h	Select event to be counted by Usb_DClk_EventCnt0.
Usb_DClk_EventSel1	15:8	00h	Select event to be counted by Usb_DClk_EventCnt1.
Usb_DClk_EventCnt0Hi	23:16	00h	Read-only. Usb DClk Event Counter 0[39:32]
Usb_DClk_EventCnt1Hi	31:24	00h	Read-only. Usb DClk Event Counter 1[39:32]

Usb_DClk_EventCntCtl – RW – 32 bits – [Ind_Reg:1Ch]			
Field Name	**Bits**	**Default**	**Description**
Usb_DClk_EventCntEn	0	0b	Enable Usb DClk event counters.
Usb_DClk_EventCntResetB	1	1b	Active low reset for Usb DClk event counters.
Usb_DClk_EventCntShadow	2	0b	Transfer Usb DClk event counter to shadow register.
Reserved	31:3	0h	Reserved

2.2.8.3 60MHz Indirect Space

Note: Registers in the IND60 space shall only be read and written with dword accesses.

Register Name	Offset Address
UTMI Control	00h
USB PHY Status	04h
USB Common PHY CAL & Control Register	08h
USB Common PHY Control	0Ch
HS_Loopback Test	10h
CL_Loopback Test	14h
Misc Control	18h
Usb_SClk_EventCnt0Lo	20h
Usb_SClk_EventCnt1Lo	24h
Usb_SClk_EventCntSel	28h
Usb_SClk_EventCnt0Hi	2Ah
Usb_SClk_EventCnt1Hi	2Bh
Usb_SClk_EventCntCtl	2Ch
XHC_SPI_RESERVED	30h
XHC_CHICKEN_BITS_RESERVED_34	34h
XHC_CHICKEN_BITS_RESERVED_38	38h
XHC_CHICKEN_BITS_RESERVED_3C	3Ch
ROM Test Control/Status	40h
ROM Test Data	44h
LPMCTRL	48h
USB Common PHY Control 2	50h
USB Common PHY Control 3	54h
XHC PORT HIDDEN CTRL 1	58h
XHC PORT HIDDEN CTRL 2	5Ch

UTMI Control – RW - 32 bits - [IND60_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
VControl	6:0	24h	Control PHY setting **Group-0** (VControlModeSel=0) VControl[6:0] = { CLKOff_disable, DCPADJ[2:0], HSADJ[2:0]} - HSADJ[2:0]: HS TX current adjustment – default 000b. 000: +0% for length < 5” 001: +5% for length < 8” 010: +10% for length < 12” 011: +15% for length > 12” - DCPADJ: adjust DLL charge pump (in analog PHY) – default 101b. 00020 uA 00123 uA 01025 uA 01128 uA 10030 uA 10136 uA 11042 uA 11150 uA - CLKOFF_disable : to disable UTMICLK gate off function **Group-1** (VControlModeSel =1) VControl[6:0] = {CDRDebugOutEnable , CDRDebugMode[1:0], TESTMODE[3:0]} TESTMODE[3:0]Description 0000 Disable Test Mode 0001~ 0111Enable Analog PHY Test mode, TMODE1 ~ TMODE7 1000 Enable Analog loop back 1001 Enable digital loop back 1010 (*)Enable MUXing of Rtesti_0 to TX data path (* Note) 1011 (*)Enable MUXing of Rtesti_1 to TX data path (* Note) 1100 Enable disconnect debug mode, route analog disconnect to FL_VM 1101 Enable Full speed driver (SPEED) when in HS mode 1110 ~ 1111Reserved * Note: When set to this mode, this port is used to support neighbor port CDR visibility, the port cannot operate in normal function. CDRDebugMode[1:0]Description 00 CDR debug disable, normal operation 01 MUX CDREnclkStatus to utmi_rxd, rsync to utmi_rxvalid. 10 MUX Rdata to utmi_rxd, rsync to utmi_rxvalid. 11 MUX ldata to utmi_rxd, lvalid to utmi_rxvalid. CDRDebugOutEnable - Enable to drive RCK & RData to the 2 test output pins, (rcko, rdo).

UTMI Control – RW - 32 bits - [IND60_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
			Group-2 Bits[1:0] CDRDebugRdoSel[1:0] Bits[3:2] CDRDebugRckoSel[1:0] Bits[5:4] Reserved Bit[6] CDRDebugEnClkSel **Group-3 (control bits)** Bit[0] HS Squelch detect de-glitch enable Bit[1] Digital loopback fix enable Bit[2] !CLKOFF_enable Bit[3] Transmit cycle fix enable Bit[4] CLK480TEST_EN Bit[5] RESETDLL Bit[6] Reserved **Group-4** Bits[6:0] Reserved **Group-5** Bits[6:0] Reserved **Group-6** Bits[6:0] Reserved **Group-7** Bit[0] XTION Limit Enable 0: Disabled (default) 1: Enabled Bit[1] XTION Limit Status Clear Bit[2] XTION Limit Mode 0: Limit == 2 1: Limit == 3 (default) Bits[6:3] Reserved
VControlModeSel	9:7	000b	The PHY control modes are divided into 8 groups. VcontrolModeSel is used to select the group.
Reserved	11:10		Reserved
VLoadB	12	1b	Update PHY control mode (active load) 0: load the new VControl value to PHY/common block 1: only VControlModeSel value to PHY will be updated for selecting different PHY status group (see PHY status registers, EOR_Reg x88 ~ x90). But VControl[6:0] value inside PHY won't get affected.
Port Number	16:13	0h	Select the corresponding port PHY or common block to load the VControl bits. 0000: port0 0001: port1 0010 ~ 1110: Reserved, no effect 1111: Common block
VBusy	17	0b	Read Only To block software write to bits[16:8] when port router is updating the field.
Reserved	31:18		Reserved
Note: Group1 - Group7 Vcontrol can be read back through USB PHY Status register. In order to read Group1 ~ Group7 Vcontrol: Set: UTMI_Control[0] = 0 UTMI_Control[9:7] = Group# UTMI_Control[16:13] = PHY Port Number Read corresponding PORTx_PHYStatus field of USB PHY Status			

USB PHY Status – RW - 32 bits - [IND60_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
PORT0_PHYStatus	7:0	21h	Read only. PHY Status of Port0
PORT1_PHYStatus	15:8	21h	Read only. PHY Status of Port1
Reserved	31:16		Reserved

PORTn_PHYStatus selection is controlled via the UTMI Control register (IND60_Reg: 00h).

When UTMI_Control[0]==1, the following tables specify PORTn_PHYStatus:

UTMI_Control[8:6] == 000b

Bit	Description
2:0	HSADJ2-0
5:3	DUTYADJ2-0
6	CLKOFF bit to turn off UTMI clock
7	Ebuffer error or rx error

UTMI_Control[8:6] == 001b

Bit	Description
0	Irsync
1	Istate, state of the ebuffer
2	sync from rxdec
3	latch_hseopr
6:4	rxstate
7	group3_vcontrol[0]

UTMI_Control[8:6] == 010b

Bit	Description
3:0	group1_vcontrol[3:0]
4	CONNECT_STATUS
5	VDM_SRC_EN
6	IDP_SINK_EN
7	VDAT_DET

UTMI_Control[8:6] == 011b

Bit	Description
7:0	CDREnClkStatus

UTMI_Control[8:6] == 100b

Bit	Description
0	ADISCONN
1	HS_SQUEL
3	xtion_limit_status
7:3	5'd0

When UTMI_Control[0]==0, UTMI_Control[9:7] (VControlModeSel) selects the corresponding VControl register to PORTn_PHYStatus.

VControlModeSel	Description
000b	{0, group0_vcontrol[6:0]}
001b	{0, group1_vcontrol[6:0]}
010b	{0, group2_vcontrol[6:0]}
011b	{0, group3_vcontrol[6:0]}
100b	{0, group4_vcontrol[6:0]}
101b	{0, group5_vcontrol[6:0]}
110b	{0, group6_vcontrol[6:0]}
111b	{0, group7_vcontrol[6:0]}

USB Common PHY CAL & Control Register – RW - 32 bits - [IND60_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
ComCalBus	6:0		Read Only. Calibration bus value from PHY before adjustment. Default value = Don't care.
Reserved	7	0b	Reserved
NewCalBus	15:8	00h	New calibration bus signed value.
UseCommonCalibration	16	0b	If set, the PHY's calibration value in bits[6:0] is returned to the PHY ports. If cleared, the value after adjustment is returned to the PHY ports.
AddToCommonCalibration	17	1b	If set, the signed NewCalBus is added to the ComCalBus and returned to the PHY ports. Any overflow is clamped to all 1s. Any underflow is clamped to all 0s. If cleared, the signed NewCalBus replaces the ComCalBus and returns to the PHY ports.
Reserved	23:18	0000h	
CommonPhyCalBus	30:24	7Fh	Read Only. Phy Common Calibration Bus
Reserved	31	0b	
Note: This register shall only be read and written with dword accesses.			

Note:

1. The equation for the calibration resistor value is

   Rcal = 1/ [1/59.4 + CalValue/(1.05*3.8k ohm)]

   where CalValue is the final 7 bits of calibration setting sent to PHY.
2. The total termination resistance value for HS USB D+/D- should include another 5 ohm resistance from the FS driver.

USB Common PHY Control – RW - 32 bits - [IND60_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
CPADJ (*)	3:0	4h	Charge Pump setting for common block PLL.
XREFADJ (*)	7:4	1h	External reference bias adjustment for common block.
IREFADJ (*)	11:8	1h	Internal reference bias adjustment for common block.
PVI (*)	15:12	2h	PLL V-I Converter Control for common block PLL.
DUTYADJ (*)	19:16	4h	CLK480 duty cycle control from 40-60% to 60-40%.
PLL Bypass	20	0b	Enable USB Common PLL bypass
Reserved	23:21	0h	Reserved
DLL Control	31:24	A0h	USB PHY DLL control {DLL_VtoI[1:0], DLL_cpump[2:0], DLL_EN_PFDphases, reserved[1:0]} DLL_VtoI: DLL gain control DLL_cpump: DLL charge pump current control DLL_EN_PFDphases: Enable DLL phase-sampling based lock detection
* Note: Common block uses 3 bits for each control function, so the 4th bit of the control doesn't have any effect on the common block. Note: This register shall only be read and written with dword accesses.			

HS_Loopback Test – RW - 32 bits - [IND60_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Received Packet Count	3:0	0h	RX data packet count. This counter defines the number (in power of 16) of RX data packet that should be checked for the loop back test.
Reserved	7:4		Reserved
Enable Loop Back Test	8	0b	Enable external USB port loopback test. The loopback test is to set one port to TX mode (Test Packet mode) and one port to RX mode (Test SE0_NAK). Refer to PORTSC [19:16] for information on the tests.
Loopback Test Status	9	0b	Read Only. 0: CRC error on loopback receiving data 1: Good CRC on loopback receiving data
Loopback Test Done	10	0b	Read Only. Indicates loopback test is done.
Reserved	11	0b	
Good Received Packet Count	19:12	--	Read Only. The number of good packets that the host controller received during the loopback test mode. These bits will be cleared by clearing bit[8] (Enable Loop Back test).
Enable PHY PowerUp State Checking	20	0b	Enable auto-checking on PHY Power Up State. There is built-in logic to check the PHY default Power Up state to detect manufacturing defects in the PHY macro.
Status of ports for PowerUp State Check	22:21	0b	Read Only. Status bit to indicate the Power Up state auto-checking result from the individual port. Each bit maps to a corresponding port, from port-0 to port-5, i.e. bit-21 for port-0, bit-22 for port-1, and so on. The value can only be checked when the PHY PowerUp State Checking Done bit is set. 0: PHY Power Up State checking is fail. 1: PHY Power Up State checking is good.
Reserved	31:23	00000b	

CL_LoopBackControl- 32 bits - [IND60_Reg: 14h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
LoopBackTestStart	0	0	RW	R	To start the Loop Back test. Software should set this bit to start the loop back test and should clear this bit to clear out all the test status before starting the next loop.
Reserved	3:1				
PortUnderTest	7:4	0	RW	R	Port Under Test. Software selects the port under test through these bits. Software should only program the port number to the range of # of ports that OHCI supports. 0000: port-0 0001: port-1 0010: port-2 ... and so on.
LoopBackTestData	15:8	0	RW	R	1-byte test data pattern for transmit and receive logic check the received data to match with this data pattern.
LoopBackTestStatus	30:16	0	R	W	Loop Back Test Status for the port under test. Read-only. 0: Fail 1: Pass Bit-16 represents the status from port-0, bit-17 for port-1 and so on. Software can only check these status bits when the “LoopBackTestDone” bit is set by the host controller. These bits can only be cleared when software clears the “LoopBackTestStart” bit.

CL_LoopBackControl- 32 bits - [IND60_Reg: 14h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
LoopBackTestDone	31	0	R	W	Read-only. Host Controller sets the bit when loop back is done. The bit is cleared when software clears the "LoopBackTestStart" bit.

Misc Control – RW - 16 bits - [IND60_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
U2IF Power Saving Enable	0	1b	Enable power saving clock gating. When enabled, dynamic clock gating is enabled when U2IF trans_state is in idle state. (The clock going to all memory modules can be gated off. Blink clock also can get gated off unless the connection interrupt is detected.)
Test packet inter-packet gap enable	2	1b	Enable inter-packet gap function for general test packet mode.
Reserved	3	0h	Reserved
Obsoleted	5:4	0h	Used to enable the battery charger for xhc ports
Reserved	7:6	0h	Reserved
Inter-packet Gap Adjust Counter	11:8	4h	Counter used to adjust the inter-packet gap for test packet.
Reserved	15:12	0h	Reserved

Usb_SClk_EventCnt0Lo – R – 32 bits – [Ind60_Reg:20h]			
Field Name	**Bits**	**Default**	**Description**
Usb_SClk_EventCnt0Lo	31:0	0h	Usb SClk Event Counter 0[31:0]

Usb_SClk_EventCnt1Lo – R – 32 bits – [Ind60_Reg:24h]			
Field Name	**Bits**	**Default**	**Description**
Usb_SClk_EventCnt1Lo	31:0	0h	Usb SClk Event Counter 1[31:0]

Usb_SClk_EventCntSel – RW – 32 bits – [Ind60_Reg:28h]			
Field Name	**Bits**	**Default**	**Description**
Usb_SClk_EventSel0	7:0	00h	Select event to be counted by Usb_SClk_EventCnt0.
Usb_SClk_EventSel1	15:8	00h	Select event to be counted by Usb_SClk_EventCnt1.
Usb_SClk_EventCnt0Hi	23:16	00h	(Read Only) Usb SClk Event Counter 0[39:32]
Usb_SClk_EventCnt1Hi	31:24	00h	(Read Only) Usb SClk Event Counter 1[39:32]

Usb_SClk_EventCntCtl – RW – 32 bits – [Ind60_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Usb_SClk_EventCntEn	0	0b	Enable Usb SClk event counters.
Usb_SClk_EventCntResetB	1	1b	Active low reset for Usb SClk event counters.
Usb_SClk_EventCntShadow	2	0b	Transfer Usb SClk event counter to shadow register.
Reserved	31:3	0h	Reserved

XHC_Reserved – RW – 32 bits – [Ind60_Reg:30h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	RW

XHC_CHICKEN_BITS_RESERVED_34 – RW – 32 bits – [Ind60_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
XHC_CHICKEN_BITS_RESERVED_34	31:0	0h	Reserved registers for chicken bits

XHC_CHICKEN_BITS_RESERVED_38 – RW – 32 bits – [Ind60_Reg:38h]			
Field Name	**Bits**	**Default**	**Description**
XHC_CHICKEN_BITS_RESERVED_38	31:0	0h	Reserved registers for chicken bits

XHC_CHICKEN_BITS_RESERVED_3C – RW – 32 bits – [Ind60_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
XHC_CHICKEN_BITS_RESERVED_3C	31:0	0h	Reserved registers for chicken bits

ROMTESTCS – RW - 32 bits - [IND60_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
ROM Test Initiate	0	0b	Write Only When this bit is written to 1, the ROM test will be initiated. When this bit is written, Done bit and Pass bit can be cleared. This bit is always read as 0.
ROM Test Mode	1	0b	0: Self-test Mode 1: Read Mode
ROM Test Address	14:2	0b	This field specifies the address in DWords of the end address for self-test mode or the read address in the read mode. Valid values are from 0000h to 1fffh.
Reserved	28:15	0h	Reserved
ROM Test Busy	29	0b	Read Only When this bit is 1, it indicates the ROM test is in progress.
ROM Test Done	30	0b	Read Only When this bit is 1, it indicates the self-test result or the read data is valid.
ROM Test Pass	31	0b	Read Only 0: Failed 1: Passed
Note: The ROM Test Mode and ROM Test Addr should be ready before or at the same time when ROM Test Initiate set to 1. They can be written in one shot when DWord access. When program register ROMTESTCS byte by byte, please be sure to program byte 0 at last or program ROM Test Mode and ROM Test Addr firstly with ROM Test Initiate as 0 and then do another program to set ROM Test Initiate to 1			

ROMTESTDATA – RW - 32 bits - [IND60_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
ROM Test Data	31:0	0h	Rom Test Data RW When it's in self-test mode, this field will be compared with the test calculation result. When it's in read mode, this field is the ROM read out data associated with the test address.
Note: This register shall only be read and written using dword accesses.			

LPMCTRL – RW - 32 bits - [IND60_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
CFGU_L1_RESIDENCY_DURATION	4:0	0h	L1 Residency Duration RW Software sets this field to indicate the minimum duration that the XHC should stay in L1Suspend. The L1 Residency Timer will load this duration when LPM transaction ACK is received and HLE is 0. When the timer expires and there is either Hardware Initiated L1 Resume Request or Remote Wake detected, the Root Hub state will jump to L1Resuming. 00000 50us 00001 100us 00010 150us … … 11111 1.6ms

LPMCTRL – RW - 32 bits - [IND60_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
CFGU_RWAKE_RSM_DURATION[3:0]	8:5	0h	Remote Wake Resume Duration RW Software sets this field to indicate how long the XHC should stay in L1Resuming after remote wake is detected. The L1 Resume Timer will load this duration after remote wake is detected and HLE is 0. When the timer expires, the Root Hub state will jump to SENDEOR. 0000 60us 0001 135us 0010 210us … … 1100 960us Others Reserved
CFGU_DEV_RECOVERY_DIS	9	0b	Device Recovery Timer Disable RW When this bit is set, the XHC does not wait for the Device Recovery Time.
CFGU_P0_VIR_LPMRESP	12:10	0h	Port 0 Virtual LPM Response RW 3'b000: ACK 3'b010: STALL 3'b011: NYET 3'b110: TIMEOUT Others: Reserved
CFGU_P0_VIR_LPMRESP_EN	13	0h	Port0 Virtual LPM Response Enable RW 1: Force a virtual response of port 0 LPM transaction. The type of response is determined by CFGU_P0_VIR_LPMRESP 0: Disable virtual LPM Response
CFGU_P1_VIR_LPMRESP	16:14	0h	Port 1 Virtual LPM Response RW 3'b000: ACK 3'b010: STALL 3'b011: NYET 3'b110: TIMEOUT Others: Reserved
CFGU_P1_VIR_LPMRESP_EN	17	0h	Port1 Virtual LPM Response Enable RW 1: Force a virtual response of port 1 LPM transaction. The type of response is determined by CFGU_P1_VIR_LPMRESP 0: Disable virtual LPM Response
Reserved	31:18	0000h	Reserved RW

USB Common PHY Control 2 – RW - 32 bits - [IND60_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
BGADJ (*)	3:0	6h	Bandgap voltage adjust
CBACKUP (*)	7:4	0h	Common block backup
ENLOCKDETECT	8		Enable PLL lock detection
LOCKDETECT	9		Lock detection observability
UNLOCKRESET	10		Reset sticky un-lock detector
UNLOCKSTICKY	11		Sticky unlock detection observability
Reserved	15:12		
BAT_CHARGER_EN[9:0]	25:16	10'b0	Enabling the battery charger
Bat charger expansion	31:26	6'b0	Saved for battery charger in case more control bits need to be added in the future

USB Common PHY Control 3 – RW - 32 bits - [IND60_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
BGSTART	0	1'b0	Bandgap startup tuning setting
CALENABLE	1	1'b0	Calibration Enable
PLLREG	3:2	2'b0	PLL Regulator tuning setting
PLLDIV	5:4	2'b0	PLL divider setting
PLLFILTER	7:6	2'b0	PLL Filter tuning setting

XHC PORT HIDDEN CTRL 1 – RW – 32 bits – [Ind60_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
XHC_PORT_HIDDEN_EN	0	0h	Enable bit for port number override control 0: disabled 1: enabled
Reserved	7:1	0h	Reserved registers for chicken bits
XHC_MAX_PORTS	15:8	0h	The oreverride value for HCSPARAMS1.MaxPorts This field specifies the maximum Port Number value, i.e. the highest numbered of Port Register Set that are addressable in the Operational Register Space (refer to Table 26). Valid values are in the range of 1h to FFh.
reserved	31:16	0h	Reserved registers for chicken bits

XHC PORT HIDDEN CTRL 12– RW – 32 bits – [Ind60_Reg:5Ch]			
Field Name	**Bits**	**Default**	**Description**
XHC_USB3_PORT_OFFSET	7:0	0h	The oreverride value for Compatible Port Offset field of xHCI Supported Protocol Capability USB3.0 This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.
XHC_USB3_PORT_COUNT	15:8	0h	The oreverride value for Compatible Port Count field of xHCI Supported Protocol Capability USB3.0 This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts

XHC PORT HIDDEN CTRL 12– RW – 32 bits – [Ind60_Reg:5Ch]			
Field Name	**Bits**	**Default**	**Description**
XHC_USB2_PORT_OFFSET	23:16	0h	The oreverride value for Compatible Port Offset field of xHCI Supported Protocol Capability USB2.0 This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.
XHC_USB2_PORT_COUNT	31:24	0h	The oreverride value for Compatible Port Count field of xHCI Supported Protocol Capability USB2.0 This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts

2.2.8.4 XHCI Memory Mapped Registers

Base = PCI Configuration Registers: {17h-14h,13h-10h}
Op_Base= Base + CAPLENGTH
Ext Cap Base= Base + HCCPARAMS.xECP <<2
Runtime Base= Base + RTSOFF
Doorbell Base= Base + DBOFF
MSI-X Tab Base= Base + PCI Cinfig.MSI-X Capability.Table Offset
MSI-X PBA Base= Base Address + PCI Config.MSI-X Capability.PBA Offset

2.2.8.4.1 XHC Capability Registers

Register Name	Offset Address
CAPLENGTH	00h
HCIVERSION	02h
HCSPARAMS 1	04h
HCSPARAMS 2	08h
HCSPARAMS 3	0Ch
HCCPARAMS	10h
DBOFF	14h
RTSOFF	18h

CAPLENGTH – RO – 8 bits - [Base + 00h]			
Field Name	**Bits**	**Default**	**Description**
CAPLENGTH	7:0	20h	Capability Registers Length This register is used as an offset to add to register base to find the beginning of the Operational Register space.

HCIVERSION – RO – 16 bits - [Base + 02h]			
Field Name	**Bits**	**Default**	**Description**
HCIVERSION	15:0	0100h	Host Controller Interface Version Number This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. e.g. 0100h corresponds to xHCI version 1.0. Note: Hardware default value after reset will be 0096h, it will reflect 0100h after BIOS post.

HCSPARAMS1 – RO – 32 bits - [Base + 04h]			
Field Name	**Bits**	**Default**	**Description**
MaxSlots	7:0	20h	Number of Device Slots This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255. The value of '0' is reserved.
MaxIntrs	18:8	008h	Number of Interrupters This field specifies the number of Interrupters implemented on this host controller. Each Interrupter may be allocated to a MSI or MSI-X vector and controls its generation and moderation. The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space. Valid values are in the range of 1h to 400h. A '0' in this field is undefined.
Reserved	23:19	00h	
MaxPorts	31:24	04h	Number of Ports This field specifies the maximum Port Number value, i.e. the highest numbered Port Register Sets thatare addressable in the Operational Register Space. Valid values are in the range of 1h to FFh. The value in this field shall reflect the maximum Port Number assigned by an xHCI Supported Protocol Capability. Software shall refer to these capabilities to identify whether a specific Port Number is valid, and the protocol supported by the associated Port Register Set.

HCSPARAMS2 – RO – 32 bits - [Base + 08h]			
Field Name	**Bits**	**Default**	**Description**
IST	3:0	1h	Isochronous Scheduling Threshold The value in this field indicates to system software the minimum distance (in time) that it is required to stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/ microframes. If bit [3] of IST is cleared to '0', software can add a TRB no later than IST[2:0] Microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to '1', software can add a TRB no later than IST[2:0] Frames before that TRB is scheduled to be executed.

HCSPARAMS2 – RO – 32 bits - [Base + 08h]			
Field Name	**Bits**	**Default**	**Description**
ERST Max	7:4	1h	Event Ring Segment Table Max Valid values are 0 – 15. This field determines the maximum value supported the Event Ring Segment Table Base Size registers where: The maximum number of Event Ring Segment Table entries = 2^{ERST_MAX} e.g. if the ERST_MAX = 7, then the xHC *Event Ring Segment Table(s)* supports up to 128 entries, 15 then 32K entries, etc
Reserved	20:8	0000h	
Max Scratchpad Bufs Hi	25:21	00h	Max Scratchpad Buffers This field indicates the high order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC.
SPR	26	0b	Scratchpad Restore If Max Scratchpad Buffers > '0', then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If Max Scratchpad Buffers=0, this flag shall be 0. A value of '1' indicates that the xHC requires the integrity of the Scratchpad Buffer space to be maintained across power events. A value of '0' indicates that the Scratchpad Buffer space may be freed and reallocated between power events.
Max Scratchpad Bufs Lo	31:27	0h	Max ScratchPad Buffers Valid values for Max Scratchpad Buffers (Hi and Lo) are 0-1023. This field indicates the low order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC.

HCSPARAMS3 – RO – 32 bits - [Base + 0Ch]			
Field Name	**Bits**	**Default**	**Description**
U1 Device Exit Latency	7:0	00h	U1 Device Exit Latency Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs. … 0Ah Less than 10 µs. 0B-FFh Reserved
Reserved	15:8	00h	
U2 Device Exit Latency	31:16	0000h	U2 Device Exit Latency Worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: Value Description 0000h Zero 0001h Less than 1 µs. 0002h Less than 2 µs. … 07FFh Less than 2047 µs. 0800-FFFFh Reserved

HCCPARAMS – RO – 32 bits - [Base + 10h]			
Field Name	**Bits**	**Default**	**Description**
AC64	0	1b	64-bit Addressing Capability This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64 bit register and data structure pointer fields. Values for this flag have the following interpretation: **Value Description** 0 32-bit address memory pointers implemented 1 64-bit address memory pointers implemented If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers.
BNC	1	1b	BW Negotiation Capability This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: **Value Description** 0 BW Negotiation not implemented 1 BW Negotiation implemented
CSZ	2	0b	Context Size If this bit is set to '1', then the xHC uses 64 byte Context data structures. If this bit is cleared to '0', then the xHC uses 32 byte Context data structures. Note: This flag does not apply to Stream Contexts.
PPC	3	0b	Port Power Control This flag indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches. The value of this flag affects the functionality of the PP flag in each port status and control register.
PIND	4	0b	Port Indicators This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/ writeable field for controlling the state of the port indicator
LHRC	5	0b	Light HC Reset Capability This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A '1' in this bit indicates that Light Host Controller Reset is supported. A '0' in this bit indicates that Light Host Controller Reset is not supported. The value of this flag affects the functionality of the Light Host Controller Reset (LHCRST) flag in the USBCMD register.
LTC	6	1b	Latency Tolerance Messaging Capability This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A '1' in this bit indicates that LTM is supported. A '0' in this bit indicates that LTM is not supported.
NSS	7	1b	No Secondary SID Support This flag indicates whether the host controller implementation supports Secondary Stream IDs. A '1' in this bit indicates that Secondary Stream ID decoding is not supported. A '0' in this bit indicates that Secondary Stream ID decoding is supported.
PAE	8	0b	Parse All Event Data This flag indicates whether the host controller implementation parses all Event Data TRBs while advancing to the next TD after a Short Packet, or it skips all but the first Event Data TRB. A '1' in this it indicates that all Event Data TRBs are parsed. A '0' in this bit indicates that only the first Event Data TRB is parsed.
Reserved	11:9	000b	

HCCPARAMS – RO – 32 bits - [Base + 10h]			
Field Name	**Bits**	**Default**	**Description**
MaxPSASize	15:12	4h	Maximum Primary Stream Array Size This field identifies the maximum size Primary Stream Array that the xHC supports. The *Primary Stream Array* size = $2^{MaxPSASize+1}$. Valid *MaxPSASize* values are 0 to 15, where '0' indicates that Streams are not supported..
xHCI Extended Capabilities Pointer xECP	31:16	0140h	xHCI Extended Capabilities Pointer This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability. For example, using the offset of Base is 1000h and the xECP value of 0068h, we can calculate the following effective address of the first extended capability: 1000h + (0068h << 2) -> 1000h + 01A0h -> 11A0h

DBOFF – RO – 32 bits - [Base + 14h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0000_0800h	
DBOFF	31:2		Doorbell Array Offset This field defines the offset in Dwords of the Doorbell Array base address from the Base (i.e., the base address of the xHCI Capability register address space)

RTSOFF – RO – 32 bits - [Base + 18h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	4:0	0000_0600h	
RTSOFF	31:5		Runtime Register Space Offset This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. i.e. Runtime Register Base Address = Base + Runtime Register Set Offset

2.2.8.4.2 XHC Operational Registers

Register Name	Offset Address
USBCMD	00h
USBSTS	04h
PAGESIZE	08h
Reserved	0C-13h
DNCTRL	14h
CRCR	18h
Reserved	20-2Fh
DCBAAP	30h
CONFIG	38h
Reserved	3C-3FFh
Port Register Set 1 - 4	420-45Ch
Reserved	460-13FFh

USBCMD – RW – 32 bits - [OP_Base + 00h]			
Field Name	**Bits**	**Default**	**Description**
R/S	0	0b	Run/Stop '1' = Run. '0' = Stop. When set to a '1', the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a '1'. When this bit is cleared to '0', the xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. The xHC shall halt within 16 microframes after software clears the *Run/Stop* bit if the above conditions have been met. The *HCHalted* (HCH) bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (i.e. *HCH* in the USBSTS register is '1'). Doing so will yield undefined results. Writing a '0' to this flag when the xHC is in the Running state (i.e. HCH = '0') and any Event Rings are in the Event Ring Full state may result in lost events. When this register is exposed by a Virtual Function (VF), this bit only controls the run state of the xHC instance presented by the selected VF.
HCRST	1	0b	Host Controller Reset This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to a Chip Hardware Reset. When software writes a '1' to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset shall not be driven on USB2 downstream ports, however a Hot or Warm Reset shall be initiated on USB3 Root Hub downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Software shall reinitialize the host controller in order to return the host controller to an operational state. This bit is cleared to '0' by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a '0' to this bit and shall not write any xHC Operational or Runtime registers until while *HCRST* is '1'. Note, the completion of the xHC reset process is not gated by the Root Hub port reset process. Software shall not set this bit to '1' when the HCHalted (HCH) bit in the USBSTS register is a '0'. Attempting to reset an actively running host controller may result in undefined behavior. When this register is exposed by a Virtual Function (VF), this bit only resets the xHC instance presented by the selected VF.

USBCMD – RW – 32 bits - [OP_Base + 00h]			
Field Name	**Bits**	**Default**	**Description**
INTE	2	0b	Interrupter Enable This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is a '1', then Interrupter host system interrupt generation is allowed, e.g. the xHC shall issue an interrupt at the next interrupt threshold if the host system interrupt mechanism (e.g. MSI, MSI-X, etc.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism. When this register is exposed by a Virtual Function (VF), this bit only enables the set of Interrupters assigned to the selected VF.
HSEE	3	0b	Host System Error Enable When this bit is a '1', and the *HSE* bit in the USBSTS register is a '1', the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the *HSE* bit. When this register is exposed by a Virtual Function (VF), the effect of the assertion of this bit on the Physical Function (PF0) is determined by the VMM.
Reserved	6:4	000b	
LHCRST	7	0b	Light Host Controller Reset - RO If the *Light HC Reset Capability* (LHRC) bit in the HCCPARAMS register is '1', then this flag allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as '0' indicates the *Light Host Controller Reset* has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a '1' indicates the *Light Host Controller Reset* has not yet completed. If not implemented, a read of this flag shall always return a '0'. All registers in the Aux Power well shall maintain the values that had been asserted prior to the *Light Host Controller Reset*. When this register is exposed by a Virtual Function (VF), this bit only generates a Light Reset to the xHC instance presented by the selected VF, e.g. Disable the VFs' device slots and set the associated VF Run bit to Stopped.
CSS	8	0b	Controller Save State When written by software with '1' and *HCHalted* (HCH) = '1', then the xHC shall save any internal state that may be restored by a subsequent Restore State operation. When written by software with '1' and *HCHalted* (HCH) = '0', or written with '0', no Save State operation shall be performed. This flag always returns '0' when read. Refer to the *Save State Status* (SSS) flag in the USBSTS register for information on Save State completion. Note that undefined behavior may occur if a Save State operation is initiated while *Restore State Status* (RSS) = '1'. When this register is exposed by a Virtual Function (VF), this bit only controls saving the state of the xHC instance presented by the selected VF.

USBCMD – RW – 32 bits - [OP_Base + 00h]			
Field Name	**Bits**	**Default**	**Description**
CRS	9	0b	Controller Restore State When set to '1', and *HCHalted* (HCH) = '1', then the xHC shall perform a Restore State operation and restore its internal state. When set to '1' and *Run/Stop* (R/S) = '1' or *HCHalted* (HCH) = '0', or when cleared to '0', no Restore State operation shall be performed. This flag always returns '0' when read. Refer to the *Restore State Status* (RSS) flag in the USBSTS register for information on Restore State completion. Note that undefined behavior may occur if a Restore State operation is initiated while *Save State Status* (SSS) = '1'. When this register is exposed by a Virtual Function (VF), this bit only controls restoring the state of the xHC instance presented by the selected VF.
EWE	10	0b	Enable Wrap Event When set to '1', the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to '0' no MFINDEX Wrap Events are generated. When this register is exposed by a Virtual Function (VF), the generation of MFINDEX Wrap Events to VFs shall be emulated by the VMM.
EU3S	11	0b	Enable U3 MFINDEX Stop When set to '1', the xHC may stop the MFINDEX counting action if all Root Hub ports are in the **U3**, **Disconnected**, **Disabled**, or **Powered-off** state. When cleared to '0' the xHC may stop the MFINDEX counting action if all Root Hub ports are in the **Disconnected**, **Disabled**, **Training,** or **Powered-off** state.
Reserved	31:12	0000h	
Note: The *R/S* flag has no affect on the operation of the Debug Capability.			

USBSTS – RO/RW/RW1C – 32 bits - [OP_Base + 04h]			
Field Name	**Bits**	**Default**	**Description**
HCH	0	1b	HCHalted - RO This bit is a '0' whenever the *Run/Stop* (R/S) bit is a '1'. The xHC sets this bit to '1' after it has stopped executing as a result of the *Run/Stop* (R/S) bit being cleared to '0', either by software or by the xHC hardware (e.g. internal error). If this bit is '1', then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC, and any received Transaction Packet shall be dropped. When this register is exposed by a Virtual Function (VF), this bit only reflects the Halted state of the xHC instance presented by the selected VF.
Reserved	1	0b	
HSE	2	0b	Host System Error - RW1C The xHC sets this bit to '1' when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. (In a PCI system, conditions that set this bit to '1' include PCI Parity error, PCI Master Abort, and PCI Target Abort.) When this error occurs, the xHC clears the *Run/Stop* (R/S) bit in the USBCMD register to prevent further execution of the scheduled TDs. If the *HSEE* bit in the USBCMD register is a '1', the xHC shall also assert out-of-band error signaling to the host. When this register is exposed by a Virtual Function (VF), the assertion of this bit affects all VFs and reflects the *Host System Error* state of the Physical Function (PF0).

USBSTS – RO/RW/RW1C – 32 bits - [OP_Base + 04h]			
Field Name	**Bits**	**Default**	**Description**
EINT	3	0b	Event Interrupt - RW1C The xHC sets this bit to '1' when the *Interrupt Pending* (IP) bit of any Interrupter transitions from '0' to '1'. Software that uses *EINT* shall clear it prior to clearing any *IP* flags. A race condition may occur if software clears the *IP* flags then clears the *EINT* flag, and between the operations another *IP* '0' to '1' transition occurs. In this case the new IP transition shall be lost. When this register is exposed by a Virtual Function (VF), this bit is the logical 'OR' of the *IP* bits for the Interrupters assigned to the selected VF. And it shall be cleared to '0' when all associated interrupter *IP* bits are cleared, i.e. all the VF's Interrupter Event Ring(s) are empty.
PCD	4	0b	Port Change Detect - RW1C The xHC sets this bit to a '1' when any port has a change bit transition from a '0' to a '1'. This bit is allowed to be maintained in the Aux power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits. This bit provides system software an efficient means of determining if there has been Root Hub port activity. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Root Hub Ports associated with the Device Slots assigned to the selected VF.
Reserved	7:5	000b	
SSS	8	0b	Save State Status - RO When the *Controller Save State* (CSS) flag in the USBCMD register is written with '1' this bit shall be set to '1' and remain 1 while the xHC saves its internal state. When the Save State operation is complete, this bit shall be cleared to '0'. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the saving the state for the selected VF.
RSS	9	0b	Restore State Status - RO When the *Controller Restore State* (CRS) flag in the USBCMD register is written with '1' this bit shall be set to '1' and remain 1 while the xHC restores its internal state. When the Restore State operation is complete, this bit shall be cleared to '0'. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the restoring the state for the selected VF.
SRE	10	0b	Save/Restore Error - RW1C If an error occurs during a Save or Restore operation this bit shall be set to '1'. This bit shall be cleared to '0' when a Save or Restore operation is initiated or when written with '1'. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Save/Restore completion status for the selected VF.
CNR	11	1b	Controller Not Ready - RO '0' = Ready and '1' = Not Ready. Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = '0'. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared ('0') until the next Chip Hardware Reset.
HCE	12	0b	Host Controller Error - RO 0' = No internal xHC error conditions exist and '1' = Internal xHC error condition. This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC.
Reserved	31:13		

PAGESIZE – RO – 32 bits - [OP_Base + 08h]			
Field Name	**Bits**	**Default**	**Description**
Page Size	15:0	0001h	Page Size This field defines the page size supported by the xHC implementation. This xHC supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the xHC supports 4k byte page sizes. For a Virtual Function, this register reflects the page size selected in the *System Page Size* field of the SR-IOV Extended Capability structure. For the Physical Function 0, this register reflects the implementation dependent default xHC page size. Various xHC resources reference PAGESIZE to describe their minimum alignment requirements. The maximum possible page size is 128M.
Rsvd	31:16	0000h	

DNCTRL – RW – 32 bits - [OP_Base + 14h]			
Field Name	**Bits**	**Default**	**Description**
N0 – N15	15:0	0000h	Notification Enable When a Notification Enable bit is set, a Device Notification Event shall be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), etc.
Reserved	31:16	0000h	

CRCR – RW – 64 bits - [OP_Base + 18]			
Field Name	**Bits**	**Default**	**Description**
RCS	0	0b	Ring Cycle State This bit identifies the value of the xHC *Consumer Cycle State* (CCS) flag for the TRB referenced by the *Command Ring Pointer*. Writes to this flag are ignored if *Command Ring Running* (CRR) is '1'. If the CRCR is written while the Command Ring is stopped (CRR = '0'), then the value of this flag shall be used to fetch the first Command TRB the next time the *Host Controller Doorbell* register is written with the *DB Reason* field set to *Host Controller Command*. If the CRCR is *not* written while the Command Ring is stopped (CRR = '0'), then the Command Ring shall begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. Reading this flag always returns '0'.
CS	1	0b	Command Stop – RW1S Writing a '1' to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a *Command Completion Event* with the *Completion Code* set to *Command Ring Stopped* and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. The next write to the *Host Controller Doorbell* with *DB Reason* field set to *Host Controller Command* shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if *Command Ring Running* (CRR) = '0'. Reading this bit shall always return '0'.

CRCR – RW – 64 bits - [OP_Base + 18]			
Field Name	**Bits**	**Default**	**Description**
CA	2	0b	Command Abort – RW1S Writing a '1' to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a *Command Completion Event* with the *Completion Code* set to *Command Ring Stopped*. The next write to the *Host Controller Doorbell* with *DB Reason* field set to *Host Controller Command* shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if *Command Ring Running* (CRR) = '0'. Reading this bit always returns '0'.
CRR	3	0b	Command Ring Running - RO This flag is set to '1' if the Run/Stop (R/S) bit is '1' and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to '0' when the Command Ring is "stopped" after writing a '1' to the Command Stop (CS) or Command Abort (CA) flags, or if the R/S bit is cleared to '0'.
Reserved	5:4	00b	
Command Ring Pointer	64:6	0h	Command Ring Pointer This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when *Command Ring Running* (CRR) = '1'. If the CRCR is written while the Command Ring is stopped (CCR = '0'), the value of this field shall be used to fetch the first Command TRB the next time the *Host Controller Doorbell* register is written with the *DB Reason* field set to *Host Controller Command*. If the CRCR is *not* written while the Command Ring is stopped (CCR = '0') then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns '0'.

DCBAAP – RW – 64 bits - [OP_Base + 30h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	5:0	00h	
Device Context Base Address Array Pointer	63:6	0h	This field defines high order bits of the 64-bit base address of the Device Context Pointer Array. A table of address pointers that reference Device Context structures for the devices attached to the host

CONFIG – RW – 32 bits - [OP_Base + 38h]			
Field Name	**Bits**	**Default**	**Description**
Max Device Slots Enabled MaxSlotsEn	7:0	00h	Max Device Slots Enabled This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0 to MaxSlots. Enabled Devices Slots are allocated contiguously. e.g. A value of 16 specifies that Device Slots 1 to 16 are active. A value of '0' disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references. This field shall not be modified by software if the xHC is running (*Run/Stop* (R/S) = '1').
Reserved	31:8	0h	

PORTSC – RO/RW/RW1C – 32 bits - [OP_Base + (420h + (10h * (n–1)))] n = 1, 2, 3, 4			
Field Name	**Bits**	**Default**	**Description**
CCS	0	0b	Current Connect Status - ROS '1' = Device is connected to the port. '0' = A device is not connected. This value reflects the current state of the port, and may not correspond directly to the event that caused the *Connect Status Change* (CSC) bit to be set to '1'. This flag is '0' if *PP* is '0'.
PED	1	0b	Port Enabled/Disabled - RW1CS '1' = Enabled. '0' = Disabled Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag. This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = '0') downstream propagation of data is blocked on this port, except for reset. For USB2.0 protocol ports: When the port is in the **Disabled** state, software shall reset the port (*PR* = '1') to transition *PED* to '1' and the port to the **Enabled** state. For USB3.0 protocol ports: When the port is in the **Polling** state (after detecting an attach), the port shall automatically transition to the **Enabled** state and set *PED* to '1' upon the completion of successful link training. When the port is in the **Disabled** state, software shall write a '5' (RxDetect) to the *PLS* field to transition the port to the **Disconnected** state. PED shall automatically be cleared to '0' when *PR* is set to '1', and set to '1' when *PR* transitions from '1' to '0' after a successful reset. Refer to Port Reset (*PR*) bit for more information on how the *PED* bit is managed. Note that when software writes this bit to a '1', it shall also write a '0' to the *PR* bit. This flag is '0' if *PP* is '0'.
Reserved	2	0b	
OCA	3	0b	Over-Current Active - RO '1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.
PR	4	0b	Port Reset - RW1S '1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit (generating a '0' to '1' transition) the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. *PR* remains set until reset signaling is completed by the root hub. Note that software shall write a '1' to this flag to transition a USB2 port from the **Polling** state to the **Enabled** state. This flag is '0' if *PP* is '0'.

PORTSC – RO/RW/RW1C – 32 bits - [OP_Base + (420h + (10h * (n–1)))] n = 1, 2, 3, 4			
Field Name	**Bits**	**Default**	**Description**
PLS	8:5	5h	Port Link State - RWS This field is used to power manage the port and reflects its current link state. When the port is in the **Enabled** state, system software may set the link U state by writing this field. System software may also write this field to force a **Disabled** to **Disconnected** state transition of the port. **Write Value** **Description** 0 The link shall transition to a U0 state from any of the U states 2 USB2 protocol ports only. The link should transition to the U2 State 3 The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. While the *Port Link State* = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5 USB3 protocol ports only. If the port is in the **Disabled** state (*PLS* = Disabled, *PP* = 1), then the link shall transition to a RxDetect state and the port shall transition to the **Disconnected** state, else ignored. 1,4,6-14 Ignored. 15 USB2 protocol ports only. If the port is in the **U3** state (*PLS* = U3), then the link shall remain in the U3 state and the port shall transition to the **Resume** substate, else ignored Note: The *Port Link State Write Strobe* (LWS) shall also be set to '1' to write this field. For USB2 protocol ports: Writing a value of '2' to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of '0' shall deassert L1 signaling on the USB. Writing a value of '1' shall have no affect. The U1 state shall never be reported by a USB2 protocol port. **Read Value** **Meaning** 0 Link is in the **U0** State 1 Link is in the **U1** State 2 Link is in the **U2** State 3 Link is in the **U3** State (Device Suspended) 4 Link is in the **Disabled** State 5 Link is in the **RxDetect** Stated 6 Link is in the **Inactive** State 7 Link is in the **Polling** State 8 Link is in the **Recovery** State 9 Link is in the **Hot Reset** State 10 Link is in the **Compliance Mode** State 11 Link is in the **Test Mode** State 12:14 Reserved 15 Link is in the **Resume** State This field is undefined if *PP* = '0'. Note: Transitions between different states are not reflected until the transition is complete.

PORTSC – RO/RW/RW1C – 32 bits - [OP_Base + (420h + (10h * (n–1)))] n = 1, 2, 3, 4			
Field Name	**Bits**	**Default**	**Description**
PP	9	1b	Port Power - RWS This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When *PP* equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when *PP* = '0' if *PPC* = '0'. After modifying PP, software shall read PP and confirm it is reached its target state before modifying it again, undefined behavior may occur if this procedure is not followed. 0 = This port is in the Powered-off state. 1 = This port is not in the Powered-off state. If the *Port Power Control* (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' = on). If the *Port Power Control* (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the *PP* bit in each affected port from a '1' to '0' (removing power from the port).
Port Speed	13:10	0h	Port Speed - ROS**.** This field identifies the speed of the connected USB Device. This field is only relevant if a device is connected (*CCS* = '1') in all other cases this field shall indicate *Undefined Speed*. **Value Meaning** 0 Undefined Speed 1 Full-speed device attached 2 Low-speed device attached 3 High-speed device attached 4 SuperSpeed device attached 5-15 Reserved Note: This field is invalid on a USB2 protocol port until after the port is reset.
PIC	15:14	00b	Port Indicator Control - RWS Writing to these bits has no effect if the *Port Indicators* (*PIND*) bit in the *HCCPARAMS* register is a '0'. If *PIND* bit is a '1', then the bit encodings are: **Value Meaning** 0 Port indicators are off 1 Amber 2 Green 3 Undefined Refer to the USB2 Specification for a description on how these bits are to be used. This field is '0' if *PP* is '0'.
LWS	16	0b	Port Link State Write Strobe - RW When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'.

PORTSC – RO/RW/RW1C – 32 bits - [OP_Base + (420h + (10h * (n–1)))] n = 1, 2, 3, 4			
Field Name	**Bits**	**Default**	**Description**
CSC	17	0b	Connect Status Change - RW1CS '1' = Change in *CCS*. '0' = No change. This flag indicates a change has occurred in the port's *Current Connect Status* (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the *CCS* transition was due to software setting *PP* to '0', or the CAS transition was due to software setting WPR to '1'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing *Connect Status Change*. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it.
PEC	18	0b	Port Enabled/Disabled Change - RW1CS '1' = change in *PED*. '0' = No change. Note that this flag shall not be set if the *PED* transition was due to software setting *PP* to '0'. Software shall clear this bit by writing a '1' to it. For a USB2.0 protocol port, this bit shall be set to '1' only when the port is disabled due to the appropriate conditions existing at the EOF2 point. For a USB3 protocol port, this bit shall never be set to '1'.
WRC	19	0b	Warm Port Reset Change - RW1CS/ Reserved This bit is set when Warm Reset processing on this port completes. '0' = No change. '1' = Warm Reset complete. Note that this flag shall not be set to '1' if the Warm Reset processing was forced to terminate due to software clearing *PP* or *PED* to '0'. Software shall clear this bit by writing a '1' to it. This bit only applies to USB3 protocol ports. For USB2.0 protocol ports it shall be Reserved.
OCC	20	0b	Over-current Change - RW1CS This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-current Active (OCA). Software shall clear this bit by writing a '1' to it.
PRC	21	0b	Port Reset Change - RW1CS This flag is set to '1' due to a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to '1' if the reset processing was forced to terminate due to software clearing PP or PED to '0'. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it.
PLC	22	0b	Port Link State Change - RW1CS This flag is set to '1' due to the following *PLS* transitions: **TransitionCondition** U3 -> ResumeWakeup signaling from a device Resume -> Recovery -> U0Device Resume complete (USB3.0 protocol ports only) Resume -> U0Device Resume complete (USB2.0 protocol ports only) U3 -> Recovery -> U0 Software Resume complete (USB3.0 protocol ports only) U3 -> U0Software Resume complete (USB2.0 protocol ports only) U2 -> U0L1 Resume complete (USB2.0 protocol ports only) U0 -> U0L1 Entry Reject (USB2.0 protocol ports only) Any state -> Inactive Error (USB3.0 protocol ports only). Note that this flag shall not be set if the *PLS* transition was due to software setting *PP* to '0'. '0' = No change. '1' = Link Status Changed. Software shall clear this bit by writing a '1' to it.
CEC	23	0b	Port Config Error Change - RW1CS/Reserved This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it. Note: This flag is valid only for USB3 protocol ports. For USB2 protocol ports this bit shall be Reserved.

PORTSC – RO/RW/RW1C – 32 bits - [OP_Base + (420h + (10h * (n–1)))] n = 1, 2, 3, 4			
Field Name	**Bits**	**Default**	**Description**
CAS	24	0b	Cold Attach Status – RO '1' = Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a '1' to WPR or the xHC shall clear this bit if CCS transitions to '1'. This flag is '0' if PP is '0' or for USB2 protocol ports.
WCE	25	0b	Wake on Connect Enable - RWS Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up events.
WDE	26	0b	Wake on Disconnect Enable - RWS Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up events
WOE	27	0b	Wake on Over-current Enable - RWS Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up events
Reserved	29:28	00b	
DR	30		Device Removable - RO This flag indicates if this port has a removable device attached. '1' = Device is non-removable. '0' = Device is removable
WPR	31	0b	Warm Port Reset - RW1S/Reserved When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the *PR* flag is set to '1'. Once initiated, the *PR*, *PRC*, and *WRC* flags shall reflect the progress of the Warm Reset sequence. This flag shall always return '0' when read. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be Reserved

Port n USB3 Protocol PORTPMSC – RWS – 32 bits - [OP_Base + (424h + (10h * (n-1)))] n = 1, 2			
Field Name	**Bits**	**Default**	**Description**
U1 Timeout	7:0	00h	U1 Timeout - RWS Timeout value for U1 inactivity timer. If equal to FFh, the port is disabled from initiating U1 entry. This field shall be set to '0' by the assertion of *PR* to '1'. The following are permissible values: **Value Description** 00h Zero (default) 01h 1 µs. 02h 2 µs … 7Fh 127 µs 80h–FEhReserved FFh Infinite
U2 Timeout	15:8	00h	U2 Timeout - RWS Timeout value for U2 inactivity timer. If equal to FFh, the port is disabled from initiating U2 entry. This field shall be set to '0' by the assertion of PR to '1'. The following are permissible values: **Value Description** 00h Zero (default) 01h 256 µs 02h 512 µs … FEh 65.024 ms FFh Infinite A *U2 Inactivity Timeout LMP* shall be sent by the xHC to the device connected on this port when this field is written.

Port n USB3 Protocol PORTPMSC – RWS – 32 bits - [OP_Base + (424h + (10h * (n-1)))] n = 1, 2			
Field Name	**Bits**	**Default**	**Description**
FLA	16	0b	Force Link PM Accept - RW When this bit is set to '1', the port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit asserted ('1'). When this bit is cleared to '0', the port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit de-asserted ('0'). This flag shall be set to '0' by the assertion of *PR* to '1' or when *CCS* = transitions from '0' to '1'. Writes to this flag have no affect if *PP* = '0'. The Set Link Function LMP is sent by the xHC to the device connected on this port when this bit transitions from '0' to '1' or '1' to '0'. Improper use of the SS Force_LinkPM_Accept functionality can impact the performance of the link significantly. This bit shall only be used for compliance and testing purposes. Software shall ensure that there are no pending packets at the link level before setting this bit. This flag is '0' if PP is '0'.
Reserved	31:17	0000h	

Port n – USB2 Protocol PORTPMSC – RO/RW – 32 bits - [OP_Base + (424h + (10h * (n-1)))] n = 3,4			
Field Name	**Bits**	**Default**	**Description**
L1S	2:0	0b	L1 Status - RO This field is used by software to determine whether an L1- based suspend request (LPM transaction) was successful, specifically: **Value Meaning** 0 Invalid - This field shall be ignored by software. 1 Success - Port successfully transitioned to L1 (ACK) 2 Not Yet - Device is unable to enter L1 at this time (NYET) 3 Not Supported - Device does not support L1 transitions (STALL) 4 Timeout/Error - Device failed to respond to the LPM Transaction or an error occurred 5-7 Reserved The value of this field is only valid when the port resides in the L0 or L1 state (*PLS* = '0' or '2').
RWE	3	0b	Remote Wake Enable - RW System software sets this flag to enable or disable the device for remote wake from L1. The value of this flag shall temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.

Port n – USB2 Protocol PORTPMSC – RO/RW – 32 bits - [OP_Base + (424h + (10h * (n-1)))] n = 3,4			
Field Name	**Bits**	**Default**	**Description**
BESL	7:4	0h	Best Effort Service Latency - RW System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. The BESL value is encoded as follows: **BESL Value BESLDuration (us) Closest HIRD Duration (us)** 0 125 75 1 150 100 2 200 150 3 300 250 4 400 350 5 500 450 6 1000 950 7 2000 1950 8 3000 2950 9 4000 3950 10 5000 4950 11 6000 5950 12 7000 6950 13 8000 7950 14 9000 8950 15 10000 9950
L1 Device Slot	15:8	00h	L1 Device Slot - RW System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of '0' indicates no device is present. The xHC uses this field to lookup information necessary to generate the LPM Token packet.
HLE	16		Hardware LPM Enable - RW If this bit is set to '1', then hardware controlled LPM shall be enabled for this port. If the USB2 *Hardware LPM Capability* is not supported (*HLC* = '0') this field shall be Reserved.
Reserved	27:17	0h	
Port Test Control	31:28	0h	Port Test Control - RW When this field is '0', the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the *Powered-Off* state (PLS = *Disabled*). If the port is not in this state, the xHC shall respond with the *Port Test Control* field set to *Port Test Control Error*. The encoding of the Test Mode bits for a USB2.0 protocol port are: **Value Test Mode** 0 Test mode not enabled 1 Test J_STATE 2 Test K_STATE 3 Test SE0_NAK 4 Test Packet 5 Test FORCE_ENABLE 6-14 Reserved. 15 Port Test Control Error

Port n USB3 Protocol PORTLI – RO – 32 bits - [OP_Base + (428h + (10h * (n-1)))] n = 1, 2			
Field Name	**Bits**	**Default**	**Description**
Link Error Count	15:0	0000h	Link Error Count - RO This field returns the number of link errors detected by the port. This value shall be reset to '0' by the assertion of a Chip Hardware Reset, *HCRST*, when *PR* transitions from '1' to '0', or when *CCS* = transitions from '0' to '1'.
Reserved	31:16	0000h	

Port n USB2 Protocol PORTLI – RO – 32 bits - [OP_Base + (428h + (10h * (n-1)))] n = 3, 4			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0000h	

2.2.8.4.3 XHC Extended Capabilities

Register Name	Offset Address
USB Legacy SupportCapability	00h
	04h
Reserved	08h
Reserved	0Ch
xHCI Supported Protocol Capability (USB3)	10h
	14h
	18h
Reserved	1Ch
xHCI Supported Protocol Capability (USB2)	20h
	24h
	28h
Reserved	2Ch
Debug Capability	40h
	44h
	48h
	50h
	58h
	60h
Status	64h
	68h
	70h
	78h
	7Ch

2.2.8.4.4 USB Legacy Support Capability

USBLEGSUP – RO/RWS – 32 bits - [Ext_Cap_Base + 00h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	01h	Capability ID - RO This field identifies the extended capability.
Next Capability Pointer	15:8	04h	Next Capability Pointer - RO This field indicates the location of the next capability with respect to the effective address of this capability.
HC BIOS Owned Semaphore	16	0b	HC BIOS Owned Semaphore - RW The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to a '0' in response to a request for ownership of the xHC by system software.
Reserved	23:17		
HC OS Owned Semaphore	24	0b	HC OS Owned Semaphore - RW System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as '1' and the *HC BIOS Owned Semaphore* bit reads as '0'.
Reserved	31:25		

USBLEGCTLSTS – RO/RWS/RW1CS – 32 bits - [Ext_Cap_Base + 04h]			
Field Name	**Bits**	**Default**	**Description**
USB SMI Enable	0	0b	USB SMI Enable - RW When this bit is a '1', and the *SMI on Event Interrupt* bit (below) in this register is a '1', the host controller will issue an SMI immediately.
Reserved	3:1	000b	
SMI on Host System Error Enable	4	0b	SMI on Host System Error Enable - RW When this bit is a '1', and the *SMI on Host System Error* bit (below) in this register is a '1', the host controller will issue an SMI immediately.
Reserved	12:5	00h	
SMI on OS Ownership Enable	13	0b	SMI on OS Ownership Enable - RW When this bit is a '1' AND the OS Ownership Change bit is '1', the host controller will issue an SMI.
SMI on PCI Command Enable	14	0b	SMI on PCI Command Enable - RW When this bit is '1' and SMI on PCI Command is '1', then the host controller will issue an SMI.
SMI on BAR Enable	15	0b	SMI on BAR Enable - RW When this bit is '1' and SMI on BAR is '1', then the host controller will issue an SMI.
SMI on Event Interrupt	16	0b	SMI on Event Interrupt - RO Shadow bit of *Event Interrupt* (EINT) bit in the USBSTS register. This bit follows the state the *Event Interrupt* (EINT) bit in the USBSTS register, e.g. it automatically clears when EINT clears or set when EINT is set.
Reserved	19:17	000b	
SMI on Host System Error	20	0b	SMI on Host System Error - RO Shadow bit of *Host System Error* (HSE) bit in the USBSTS register. To clear this bit to a '0', system software shall write a '1' to the *Host System Error* (HSE) bit in the USBSTS register.
Reserved	28:21		
SMI on OS Ownership Change	29	0b	SMI on OS Ownership Change - RW1C This bit is set to '1' whenever the *HC OS Owned Semaphore* bit in the USBLEGSUP register transitions from '1' to a '0' or '0' to a '1'.
SMI on PCI Command	30	0b	SMI on PCI Command - RW1C This bit is set to '1' whenever the PCI Command Register is written.
SMI on BAR	31	0b	SMI on BAR - RW1C This bit is set to '1' whenever the Base Address Register (BAR) is written.

2.2.8.4.5 xHCI Supported Protocol Capability (USB3)

xHCI Supported Protocol Capability USB3 – RO – 32 bits - [Ext_Cap_Base + 10h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	02h	Capability ID - RO This field identifies the extended capability.
Next Capability Pointer	15:8	04h	Next Capability Pointer - RO This field indicates the location of the next capability with respect to the effective address of this capability.
Minor Revision	23:16	00h	Minor Revision - RO Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
Major Revision	31:24	03h	Major Revision - RO Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant

xHCI Supported Protocol Capability USB3 – RO – 32 bits - [Ext_Cap_Base + 14h]			
Field Name	**Bits**	**Default**	**Description**
Name String	31:0	5553_4220h	Name String - RO This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive.

xHCI Supported Protocol Capability USB3 – RO – 32 bits - [Ext_Cap_Base + 18h]			
Field Name	**Bits**	**Default**	**Description**
Compatible Port Offset	7:0	01h	Compatible Port Offset - RO This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are ‘1’ to MaxPorts.
Compatible Port Count	15:8	02h	Compatible Port Count - RO This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
Reserved	27:16	000h	
PSIC	31:28	0h	Protocol Speed ID Count This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains. If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply.

2.2.8.4.6 xHCI Supported Protocol Capability (USB2)

xHCI Supported Protocol Capability USB2 – RO – 32 bits - [Ext_Cap_Base + 20h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	02h	Capability ID - RO This field identifies the extended capability.
Next Capability Pointer	15:8	00h	Next Capability Pointer - RO This field indicates the location of the next capability with respect to the effective address of this capability. If DBC_CONTROL.DEBUG_CAP_EN == 1, then Next Capability Pointer = 08h.
Minor Revision	23:16	00h	Minor Revision - RO Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
Major Revision	31:24	02h	Major Revision - RO Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant

xHCI Supported Protocol Capability USB2 – RO – 32 bits - [Ext_Cap_Base + 24h]			
Field Name	**Bits**	**Default**	**Description**
Name String	31:0	5553_4220h	Name String - RO This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive.

xHCI Supported Protocol Capability USB2 – RO – 32 bits - [Ext_Cap_Base + 28h]			
Field Name	**Bits**	**Default**	**Description**
Compatible Port Offset	7:0	03h	Compatible Port Offset - RO This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are ‘1’ to MaxPorts.
Compatible Port Count	15:8	02h	Compatible Port Count - RO This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
Reserved	16	0b	
HSO	17	0b	High-speed Only - RO If this bit is set to ‘0’, the USB2 ports described by this capability are Low-, Full-, and High-speed capable. If this bit is set to ‘1’, the USB2 ports described by this capability are High-speed only, e.g. the ports don’t support Low- or Full-speed operation. High-speed only implementations may introduce a “Tier mismatch”.
IHI	18	0b	Integrated Hub Implemented – RO If this bit is cleared to ‘0’, the Root Hub to External xHC port mapping adheres to the default mapping. If this bit is set to a ‘1’, the Root Hub to External xHC port mapping does not adhere to the default mapping, and an ACPI or other mechanism is required to define the mapping.

xHCI Supported Protocol Capability USB2 – RO – 32 bits - [Ext_Cap_Base + 28h]			
Field Name	**Bits**	**Default**	**Description**
HLC	19	0b	Hardware LPM Capability (HLC) – RO. If this bit is set to '1', the ports described by this xHCI Supported Protocol Capability support hardware controlled USB2 Link Power Management. If XHCI_1_0_ENABLE.HW_LPM_EN is set to '1', HLC = '1'.
BLC	20	1b	BESL LPM Capability – RO If this bit is set to '1', the ports described by this xHCI Supported Protocol Capability shall apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. If this bit is cleared to '0', the ports described by this xHCI Supported Protocol Capability shall apply HIRD timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. If XHCI_1_0_ENABLE.LPM_BLC_SEL == '1', BLC = '0'.
Reserved	31:21		

2.2.8.4.7 Debug Capability

Debug Capability ID – RO - 32 bits - [Ext_Cap_Base + 40h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	0xA	Capability ID This field identifies that the function supports a Debug Device
Next Capability Pointer	15:8	0x0	Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability.
DCERST Max	20:16	0x0	Debug Capability Event Ring Segment Table Max Valid values are 0 – 15. This field determines the maximum value supported the *Debug Capability Event Ring Segment Table Base Size* registers, where: The maximum number of Event Ring Segment Table entries = $2^{\text{DCERST Max}}$. e.g., if DCERST Max = 7, then the *Debug Capability Event Ring Segment Table(s)* supports up to 128 entries, 15 then 32K entries, etc.
Reserved	31:21		

Debug Capability Doorbell – RW - 32 bits - [Ext_Cap_Base + 44h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	0h	
DB Target	15:8	0h	Doorbell Target This field defines the target of the doorbell reference. The table below defines the Debug Capability notification that is generated by ringing the doorbell. **Value Definition** 0 Data EP 1 OUT Enqueue Pointer Update 1 Data EP 1 IN Enqueue Pointer Update 2 – 255Reserved This field returns '0' when read and the value should be treated as undefined by software.
Reserved	31:16	0h	

Debug Capability Event Ring Segment Table Size – RW - 32bits - [Ext_Cap_Base + 48h]			
Field Name	**Bits**	**Default**	**Description**
Event Ring Segment Table Size	15:0	0h	Event Ring Segment Table Size This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the *Debug Capability Event Ring Segment Table Base Address* register. The maximum value supported by an xHC implementation for this register is defined by the *DCERST Max* field in the DCID register Software shall initialize this register before setting the *Debug Capability Enable* field in the DCCTRL register to '1'.
Reserved	31:16	0h	

Debug Capability Event Ring Segment Table Base Address – RW - 64 bits - [Ext_Cap_Base + 50h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	
Event Ring Segment Table Base Address Register	63:4	0h	Event Ring Segment Table Base Address Register This field defines the high order bits of the start address of the Debug Capability Event Ring Segment Table. Software shall initialize this register before setting the *Debug Capability Enable* field in the DCCTRL register to '1'.

Debug Capability Event Ring Dequeue Pointer – RW - 64 bits - [Ext_Cap_Base + 58h]			
Field Name	**Bits**	**Default**	**Description**
DESI	2:0	0h	Dequeue ERST Segment Index This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.
Reserved	3	0h	
Dequeue Pointer	63:4	0h	Dequeue Pointer This field defines the high order bits of the 64-bit address of the current Debug Capability Event Ring Dequeue Pointer. Software shall initialize this register before setting the *Debug Capability Enable* field in the DCCTRL register to '1'.

Debug Capability Control (DCCTRL) – RO/RW/RW1S/RW1C - 32 bits - [Ext_Cap_Base + 60h]			
Field Name	**Bits**	**Default**	**Description**
DCR	0	0h	DbC Run - RO When 0, Debug Device is not in the Configured state. When '1', Debug Device is in the Configured state and bulk Data pipe transactions are accepted by Debug Capability and routed to the IN and OUT Transfer Rings. A '0' to '1' transition of the *Port Reset* (DCPORTSC:PR) bit will clear this bit to '0'.
LSE	1	0h	Link Status Event Enable - RW Setting this bit to a '1' enables the Debug Capability to generate Port Status Change Events due to the *Port Link Status Change* bit transitioning from a '0' to a '1'.

Debug Capability Control (DCCTRL) – RO/RW/RW1S/RW1C - 32 bits - [Ext_Cap_Base + 60h]			
Field Name	**Bits**	**Default**	**Description**
HOT	2	0h	Halt Out TR - RW1S While this bit is '1' the Debug Capability shall generate STALL TPs for all IN TPs received for the OUT TR. The Debug Capability shall clear this bit when a ClearFeature(ENDPOINT_HALT) request is received for the endpoint. This field is valid *only* when the Debug Capability is in Run Mode (*DCR* = '1'). When not in Run Mode, this field shall return '0' when read, and writes will have no effect.
HIT	3	0h	Halt IN TR - RW1S While this bit is '1' the Debug Capability shall generate STALL TPs for all OUT DPs received for the IN TR. The Debug Capability shall clear this bit when a ClearFeature(ENDPOINT_HALT) request is received for the endpoint. This field is valid *only* when the Debug Capability is in Run Mode (*DCR* = '1'). When not in Run Mode, this field shall return '0' when read, and writes will have no effect.
DRC	4	0h	DbC Run Change - RW1C This bit shall be set to '1' when DCR bit is cleared to '0', i.e. by any DbC Port State transition that exits the **DbC-Configured** state. While this bit is '1' the *Debug Capability Doorbell Register* (DCDB) is disabled. Software shall clear this bit to re-enable the *DCDB*.
Reserved	15:5	0h	
Debug Max Burst Size	23:16	0h	Debug Max Burst Size - RO This field identifies the maximum burst size supported by the bulk endpoints of this DbC implementation.
Device Address	30:24	0h	Device Address – RO This field reports the USB device address assigned to the Debug Device during the enumeration process. This field is valid when the *DbC Run* bit is '1'.
DCE	31	0h	Debug Capability Enable – RW Setting this bit to a '1' enables xHCI USB Debug Capability operation. This bit is a '0' if the USB Debug Capability is disabled. Clearing this bit releases the Root Hub port assigned to the Debug Capability, and terminates any Debug Capability Transfer or Event Ring activity.

Debug Capability Status (DCST) – RO - 32 bits - [Ext_Cap_Base + 64h]			
Field Name	**Bits**	**Default**	**Description**
ER	0	0h	Event Ring Not Empty When '1', this field indicates that the Debug Capability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHC when the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer is equal to the *Debug Capability Event Ring Dequeue Pointer* register.
Reserved	23:1	0h	
Debug Port Number	31:24	0h	Debug Port Number This field provides the ID of the Root Hub port that the Debug Capability has been automatically attached to. The value is '0' when the Debug Capability is not attached to a Root Hub port.

Debug Capability Port Status and Control (DCPORTSC) – RO/RW/RW1C - 32 bits - [Ext_Cap_Base + 68h]			
Field Name	**Bits**	**Default**	**Description**
CCS	0	0h	Current Connect Status – RO '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the *Connect Status Change* (CSC) field in the *Port Status Change Event* that was generated by a '0' to '1' transition of this bit. This flag is '0' if *Debug Capability Enable* (DCE) is '0'.
PED	1	0h	Port Enabled/Disabled – RW '1' = Enabled. '0' = Disabled. This flag shall be set to '1' by a '0' to '1' transition of *CCS* or a '1' to '0' transition of the *PR*. When *PED* transitions from '1' to '0' due to the assertion of PR, the port's link shall transition to the Rx.Detect state. This flag may be used by software to enable or disable the operation of the Root Hub port assigned to the Debug Capability. The Debug Capability Root Hub port operation may be disabled by a fault condition (disconnect event or other fault condition, e.g. a LTSSM Polling substate timeout, tPortConfiguration timeout error, etc.), the assertion of DCPORTSC *PR*, or by software. 0 = Debug Capability Root Hub port is disabled. 1 = Debug Capability Root Hub port is enabled. When the port is disabled (*PED* = '0') the port's link shall enter the SS.Disabled state and remain there until *PED* is reasserted ('1') or *DCE* is negated ('0'). Note that the Root Hub port is remains mapped to Debug Capability while *PED* = '0'. While *PED* = '0' the Debug Capability will appear to be disconnected to the Debug Host. Note, this bit is not affected by PORTSC *PR* bit transitions. This field is '0' if *DCE* or CCS are '0'.
Reserved	3:2	0h	
PR	4	0h	Port Reset – RO '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC *PED* ('0'). This field is '0' if *DCE* or CCS are '0'.
PLS	8:5	0h	Port Link State – RO This field reflects its current link state. This field is only relevant when a Debug Host is attached (*Debug Port Number* > '0'). **Value Meaning** 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled State 5 Link is in the RxDetect State 6 Link is in the Inactive State 7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 15 – 10 Reserved Note: Transitions between different states are not reflected until the transition is complete.
Reserved	9	0h	

Debug Capability Port Status and Control (DCPORTSC) – RO/RW/RW1C - 32 bits - [Ext_Cap_Base + 68h]			
Field Name	**Bits**	**Default**	**Description**
Port Speed	13:10	0h	Port Speed – RO This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (*CCS* = '1') in all other cases this field shall indicate Undefined Speed. **Value Meaning** 0 Undefined Speed 1 – 15 Protocol Speed ID (PSI) Note: The Debug Capability does not support LS, FS, or HS operation.
Reserved	16:14	0h	
CSC	17	0h	Connect Status Change - RW1C '1' = Change in Current Connect Status. '0' = No change. Indicates a change has occurred in the port's *Current Connect Status*. The xHC sets this bit to '1' for all changes to the Debug Device connect status, even if system software has not cleared an existing DbC Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if *DCE* is '0'.
Reserved	20:18	0h	
PRC	21	0h	Port Reset Change - RW1C This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of *PR*). '0' = No change. '1' = Reset complete.Software shall clear this bit by writing a '1' to it. This field is '0' if *DCE* is '0'.
PLC	22	0h	Port Link Status Change - RW1C This flag is set to '1' due to the following *PLS* transitions: **TransitionCondition** U0 -> U3Suspend signaling detected from Debug Host U3 -> U0Resume complete Polling -> DisabledTraining Error Ux or Recovery -> InactiveError Software shall clear this bit by writing a '1' to it. This field is '0' if *DCE* is '0'.
CEC	23	0h	Port Config Error Change - RW1C This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it.
Reserved	31:24	00h	

Debug Capability Context Pointer (DCCP) – RW – 64 bits - [Ext_Cap_Base + 70h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	
Debug Capability Context Pointer Register	63:4	0000000h	Debug Capability Context Pointer This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the *Debug Capability Enable* bit in the *Debug Capability Control Register* to '1'.

Debug Capability Device Descriptor Info Register 1 (DCDDI1) – RW – 32 bits - [Ext_Cap_Base + 78h]			
Field Name	**Bits**	**Default**	**Description**
DbC Protocol	7:0	00h	DbC Protocol This field is presented by the Debug Device in the USB Interface Descriptor *bInterfaceProtocol* field. **Value Function** 0 Debug Target vendor defined 1 GNU Remote Debug Command Set supported. 2 – 255 Reserved
Reserved	15:8	00h	
Vendor ID	31:16	0000h	Vendor ID This field is presented by the Debug Device in the USB Device Descriptor *idVendor* field.

Debug Capability Device Descriptor Info Register 2 (DCDDI2) – RW – 32 bits - [Ext_Cap_Base + 7Ch]			
Field Name	**Bits**	**Default**	**Description**
Product ID	15:0	0000h	Product ID This field is presented by the Debug Device in the USB Device Descriptor *idProduct* field.
Device Revision	31:16	0000h	Device Revision This field is presented by the Debug Device in the USB Device Descriptor *bcdDevice* field.

2.2.8.4.8 XHC Runtime Registers

Runtime Base= Base + RTSOFF

Register Name	Offset Address
MFINDEX	00h
Reserved	0004h – 001Ch
Interrupter Register Set 0	0020h – 003Ch
Interrupter Register Set 1	0040h – 005Ch
Interrupter Register Set 2	0060h – 007Ch
Interrupter Register Set 3	0080h – 009Ch
Interrupter Register Set 4	00A0h – 00BCh
Interrupter Register Set 5	00C0h – 00DCh
Interrupter Register Set 6	00E0h – 00FCh
Interrupter Register Set 7	0100h – 011Ch

Microframe Index (MFINDEX) - RO - 32 bits - [Runtime Base + 00h]			
Field Name	**Bits**	**Default**	Description
Microframe Index	13:0	0h	Microframe Index The value in this register increments at the end of each microframe (e.g. 125us.). Bits [13:3] may be used to determine the current 1ms. Frame Index.
Reserved	31:14	0h	

2.2.8.4.9 Interrupter Register Set

The host controller implements eight Interrupter Register Sets. Each Interrupter Register Set consists of the following five registers:

Register Name	Offset Address
Interrupter Management (IMAN)	00h
Interrupter Moderation (IMOD)	04h
Event Ring Segment Table Size (ERSTSZ)	08h
Reserved	0Ch
Event Ring Segment Table Base Address (ERSTBA)	10h
Event Ring Dequeue Pointer (ERDP)	18h

Interrupter Register Set n - IMAN - RW - 32 bits - [Runtime Base + (20h + (20h * n))] n = 0 : 7			
Field Name	**Bits**	**Default**	**Description**
IP	0	0b	Interrupt Pending - RW1C This flag represents the current state of the Interrupter. If IP = '1', an interrupt is pending for this Interrupter. A '0' value indicates that no interrupt is pending for the Interrupter.
IE	1	0b	Interrupt Enable - RW This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set ('1'), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches '0'. If this bit is '0', then the Interrupter is prohibited from generating interrupts.
Reserved	31:2		

Interrupter Register Set n - IMOD - RW - 32 bits - [Runtime Base + (24h + (20h * n))] n = 0 : 7			
Field Name	**Bits**	**Default**	**Description**
IMODI	15:0	0FA0h	Interrupt Moderation Interval Default = '4000' (~1ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if *IP* = '0', *EHB* = '0', and the Event Ring is not empty.
IMODC	31:16	0000h	Interrupt Moderation Counter Down counter. Loaded with the IMODI value whenever *IP* is cleared to '0', counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the *IE* and *IP* flags = '1', and *EHB* = '0'. This counter may be directly written by software at any time to alter the interrupt rate

Interrupter Register Set n - ERSTSZ - RW - 32 bits - [Runtime Base + (28h + (20h * n))] n = 0 : 7			
Field Name	**Bits**	**Default**	**Description**
Event Ring Segment Table Size	15:0	0000h	Event Ring Segment Table Size This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the *Event Ring Segment Table Base Address* register. The maximum value supported by an xHC implementation for this register is defined by the *ERST Max* field in the HSCPARAMS2 register. For Secondary Interrupters: Writing a value of '0' to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of '0' to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled.
Reserved	31:16		

Interrupter Register Set n - ERSTBA - RW - 64 bits - [Runtime Base + (30h + (20h * n))] n = 0 : 7			
Field Name	**Bits**	**Default**	**Description**
Reserved	5:0		
Event Ring Segment Table Base Address Register	63:6	0h	Event Ring Segment Table Base Address This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine:EREP Advancement to the Start state. This field shall not be modified if *HCHalted* (HCH) = '0'.

Interrupter Register Set n - ERDP - RW - 64 bits - [Runtime Base + (38h + (20h * n))] n = 0 : 7			
Field Name	**Bits**	**Default**	**Description**
DESI	2:0	000b	Dequeue ERST Segment Index - RW This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.
EHB	3	0b	Event Handler Busy - RW1C This flag shall be set to '1' when the *IP* bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written.
Event Ring Dequeue Pointer	63:4	0h	Event Ring Dequeue Pointer - RW This field defines the high order bits of the 64- bit address of the current Event Ring Dequeue Pointer.

2.2.8.4.10 XHC Doorbell Registers

Doorbell Base= Base + DBOFF

Doorbell n - RW - 32 bits - [Doorbell Base + (00h + (04h * n))] n = 0 : 32			
Field Name	**Bits**	**Default**	**Description**
DB Target	7:0	00h	Doorbell Target - RW This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1-255) **Value Definition** 0 Reserved 1 Control EP 0 Enqueue Pointer Update 2 EP 1 OUT Enqueue Pointer Update 3 EP 1 IN Enqueue Pointer Update 4 EP 2 OUT Enqueue Pointer Update 5 EP 2 IN Enqueue Pointer Update … … 30 EP 15 OUT Enqueue Pointer Update 31 EP 15 IN Enqueue Pointer Update 32:247 Reserved 248:255 Vendor Defined Host Controller Doorbell (0) **Value Definition** 0 Command Doorbell 1:247 Reserved 248:255 Vendor Defined This field returns '0' when read and should be treated as "undefined" by software When the *Command Doorbell* is written, the *DB Stream ID* field shall be cleared to '0'.
Reserved	15:8	00h	
DB Stream ID	31:16	0000h	Doorbell Stream ID - RW If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (*MaxPStreams* > 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (*MaxPStreams* = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to *Device Context Doorbells* and shall be cleared to '0' for *Host Controller Command Doorbells*. This field returns '0' when read.

2.2.8.4.11 MSI-X Table

Register Name	Offset Address
MSI-X Table 0	00h – 0Ch
MSI-X Table 1	10h – 1Ch
MSI-X Table 2	20h – 2Ch
MSI-X Table 3	30h – 3Ch

Register Name	Offset Address
MSI-X Table 4	40h – 4Ch
MSI-X Table 5	50h – 5Ch
MSI-X Table 6	60h – 6Ch
MSI-X Table 7	70h – 7Ch

MSI-X Tab Base = Base + PCI Config.MSI-X Capability.Table Offset

The host controller implements eight MSI-X Tables. Each MSI-X Table has the following structure:

Register Name	Offset Address
Message Address	00h
Message Upper Address	04h
Message Data	08h
Vector Control	0Ch

Message Address for MSI-X Table #n - RW - 32 bits - [MSI-X Tab Base + (10h * n)] n = 0 : 7			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	RO For proper DWORD alignment, software must always write zeroes to these two bits; otherwise the result is undefined. The state of these bits after reset must be 0.
MessageAddress	31:2	0000_0000h	Message Address - RW System-specified message lower address. For MSI-X messages, the contents of this field from an MSI-X Table entry specifies the lower portion of the DWORD-aligned address for the memory write transaction.

Message Upper Address for MSI-X Table #n - RW - 32 bits - [MSI-X Tab Base + (14h * n)] n = 0 : 7			
Field Name	**Bits**	**Default**	**Description**
Message Upper Address	31:0	0000_0000h	Message Upper Address - RW System-specified message upper address bits.

Message Data for MSI-X Table #n - RW - 32 bits - [MSI-X Tab Base + (18h * n)] n = 0 : 7			
Field Name	**Bits**	**Default**	**Description**
Message Data	31:0	0000_0000h	Message Data - RW System-specified message data.

Vector Control for MSI-X Table #n - RW - 32 bits - [MSI-X Tab Base + (1Ch * n)] n = 0 : 7			
Field Name	**Bits**	**Default**	Description
Mask Bit	0	0b	Mask Bit - RW When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).
Reserved	31:1		

2.2.8.4.12 MSI-X PBA

MSI-X PBA Base= Base Address + PCI Config.MSI-X Capability.PBA Offset

Pending Bits for MSI-X PBA Entries - RW - 64 bits - [MSI-X PBA Base + 00h]			
Field Name	**Bits**	**Default**	**Description**
Pending Bits	63:0	0h	Pending Bits - RW For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Pending bits that have no associated MSI-X Table entry are reserved. After reset, the state of reserved Pending bits must be 0. Software should never write, and should only read Pending Bits. If software writes to Pending Bits, the result is undefined. Each Pending Bit's state after reset is 0 (no message pending).

2.3 HD Audio Controller Registers

2.3.1 HD Audio Controller PCI Configuration Space Registers (Device 20 Function 2)

Register Name	Offset Address
Device ID	00h
Vendor ID	02h
PCI Command	04h
PCI Status	06h
Revision ID	08h
Prog . Interface	09h
Sub Class Code	0Ah
Base Class Code	0Bh
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
BIST	0Fh
Lower Base Address Register	10h
Upper Base Address Register	14h
Subsystem Vendor ID	2Ch
Subsystem ID	2Eh
Capabilities Ptr	34h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min Grant	3Eh
Max Latency	3Fh
Misc Control 1	40h
Misc Control 2	42h
Misc Control 3	43h
Intr Pin Control	44h
Capability Control	45h
Debug Control	46h
Power Management Capability ID	50h
Next Capability Pointer	51h
Power Management Capabilities	52h
Power Management Control/Status	54h
MSI Capability ID	60h
Next Capability Pointer	61h
MSI Message Control	62h
MSI Lower Address	64h
MSI Upper Address	68h

Register Name	Offset Address
MSI Message Data	6Ch
AF Capability ID	70h
Next Capability Pointer	71h
AF Length	72h
AF Capabilities	73h
AF Control	74h
AF Status	75h

Vendor ID – R – 16 bits – [PCI_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Identifies the vendor as AMD

Device ID – R/W – 16 bits – [PCI_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	780Dh	Identifies this device as HD Audio Controller

PCI Command – R/W – 16 bits – [PCI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved.
Memory Space Enable	1	0b	Memory Space Enable. This bit enables the HD Audio controller to respond to PCI memory space access.
Bus Master Enable	2	0b	This bit set enables the HD Audio controller's bus mastering capability.
Reserved	9:3	00h	Reserved
Interrupt Disable	10	0b	Interrupt Disable. This bit disables the device from asserting INTx#. Note: This bit does not affect the generation of MSI.
Reserved	15:11	00h	Reserved

PCI Status – R/W – 16 bits – [PCI_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0h	Reserved
Interrupt Status	3	0b	Interrupt status. This bit is a "1" when INTx# is asserted. Note: This bit is not set by MSI.
Capabilities List	4	1b	PCI Capabilities List. This bit is hardwired to 1 to indicate that the HD Audio controller contains a capability pointer list. The first item at offset 34h
Reserved	12:5	00h	Reserved
Received Master Abort	13	0b	This bit set indicates that the HD Audio controller terminated a PCI bus operation with a Master Abort.
Reserved	15:14	0h	Reserved

Revision ID – R – 8 bits – [PCI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	01h	Chip Revision ID. This field is hardwired to 01h to indicate the revision level of the HD Audio Controller.

Programming Interface – R – 8 bits – [PCI_Reg: 09h]			
Field Name	**Bits**	**Default**	**Description**
Programming Interface	7:0	00h	Programming Interface.

Sub Class Code – R – 8 bits – [PCI_Reg: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
Sub Class Code	7:0	03h	Sub Class Code. Indicates a HD Audio device in the context of a multimedia device class.

Base Class Code – R – 8 bits – [PCI_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Base Class Code	7:0	04h	Base Class Code. Indicates a multimedia device.

Cache Line Size – R/W – 8bits – [PCI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This field is implemented as a read/write field for legacy compatibility purposes only and has no functional impact.

Latency Timer – R – 8 bits – [PCI_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Latency Timer	7:0	00h	Hardwired to 0.

Header Type – R – 8 bits – [PCI_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	00h	Hardwired to 0.

BIST – R – 8 bits – [PCI_Reg: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
BIST	15:0	0000h	Hardwired to 0.

Lower Base Address Register – R/W – 32 bits – [PCI_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Space Type	0	0b	Hardwired to 0 to indicate this BAR is located in memory space only.
Address Range	2:1	10b	Hardwired to “10” to indicate this BAR can be located anywhere in 64-bit address space.
Prefetchable	3	0b	Hardwired to 0 to indicate this BAR is not prefetchable.
Reserved	13:4	000h	Hardwired to 0.
Lower Base Address	31:14	00000h	Lower Base Address for the HD Audio controller’s memory mapped configuration registers. 16K bytes are requested by hardwiring bits [13:4] to 0.

Upper Base Address Register – R/W – 32 bits – [PCI_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Upper Base Address	31:0	00000000h	Upper Base Address for the HD Audio controller’s memory mapped confuration registers.

Subsystem Vendor ID – R/W – 16 bits – [PCI_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	This register is implemented as write-once register. Any subsequent writes have no effect.

Subsystem ID – R/W – 16 bits – [PCI_Reg: 2Dh]			
Field Name	**Bits**	**Default**	**Description**
Subsystem ID	15:0	0000h	This register is implemented as write-once register. Any subsequent writes have no effect.

Reset Value: 0

Capabilities Pointer – R – 8 bits – [PCI_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	50h	This register indicates the offset for the capability pointer.

Interrupt Line – R/W – 8 bits – [PCI_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	This register is used to communicate to software the interrupt line that the interrupt pin is connected to. It is not used by the HD Audio controller.

Interrupt Pin – R – 8 bits – [PCI_Reg: 3Dh]			
Interrupt Pin	3:0	1h	This register reflects the value programs into Interrupt Control Pin register at offset 44h, bits [3:0]
Reserved	7:4	0h	Reserved

Minimum Grant – R – 8 bits – [PCI_Reg: 3Eh]			
Field Name	**Bits**	**Default**	**Description**
Minimum Grant	7:0	00h	Hardwired to 0.

Maximum Latency – R – 8 bits – [PCI_Reg: 3Fh]			
Field Name	**Bits**	**Default**	**Description**
Maximum Latency	7:0	00h	Hardwired to 0.

Reset Value: 0

Misc Control 1 – R/W – 16 bits – [PCI_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Static Output FIFO Size Select	1:0	00b	Static Output FIFO Size is functional only when the Static Output FIFO Size Enable bit is set to “1”. 00: One-eigth of the maximum Output FIFO Size 01: One-quarter of the maximum Output FIFO size 10: One-half of the maximum Output FIFO Size 11: Use the maximum Output FIFO Size
Reserved	7:2	00h	Reserved
Static Output FIFO Size Enable	8	0b	Enable Static Output FIFO Size otherwise Output FIFO Size is set dynamically set based on Stream Format.
Reserved	15:9	00h	Reserved.

Misc Control 2 Register – R/W – 8 bits – [PCI_Reg: 42h]			
Field Name	**Bits**	**Default**	**Description**
Disable No Snoop	0	0b	1: No Snoop attribute is disabled on Buffer Descriptor and Data Buffer DMA. 0: Set the No Snoop attribute on Buffer Descriptor and Data Buffer DMA when the Traffic Priority bit is set in the Stream Descriptor.
Disable No Snoop Override	1	0b	1: Bit [0] of this register controls the No Snoop attribute 0: Override the bit [0] setting meaing always generate No Snoop attribute on Buffer Descriptor and Data Buffer DMA
Enable No Snoop Request	2	0b	1: Enable No Snoop request to ACPI 0: Disable No snoop request to ACPI When enabled and the DMA cycle is No Snoop, ACPI will not generate a wake to CPU in C2 state.
Reserved	3	0b	Reserved

Misc Control 2 Register – R/W – 8 bits – [PCI_Reg: 42h]			
Field Name	**Bits**	**Default**	**Description**
Disable Minimum Retry	4	0b	1: Disable minimum retry on ALink Bus 0: Enable When enabled, after the first request of a transaction, it will not generate another request for the same transaction unless notified by AB the data is available
Enable Clock Gating	5	0b	1: Enable clock gating 0: Disable
Enable Stop A-Link Clock	6	0b	1: Enable stop A-Link clock indication 0: Disable
Reserved	7	0b	Reserved

Misc Control 3 Register – R/W – 8 bits – [PCI_Reg: 43h]			
Reserved	7:0	00h	Reserved

Interrupt Pin Control Register – R/W – 8 bits – [PCI_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin Control	3:0	1h	Controls the value reports in Interrupt Pin Register at offset 3Dh.
Reserved	7:4	00h	Reserved

Capability Control Register – R/W – 8 bits – [PCI_Reg: 45h]			
Field Name	**Bits**	**Default**	**Description**
Enable MSI Capability	0	0b	1: Enable MSI Capability 0: Disable MSI Capability
Enable AF Capability	1	0b	1: Enable Advanced Features Capability 0: Disable Advanced Features Capability
Reserved	7:2	00h	Reserved

Debug Control Register – R/W – 16 bits – [PCI_Reg: 46h]			
Field Name	**Bits**	**Default**	**Description**
Input DMA Debug Select	1:0	00b	Selects one of four Input DMA debug signals
Output DMA Debug Select	3:2	00b	Selects one of four Output DMA debug signals
Link Input Debug Select	5:4	00b	Selects one of four Link Input debug signals
Link Output Debug Select	7:6	00b	Selects one of Link Output debug signals
Misc Debug Select	8	0b	Selects one of two sets of misc debug signals
Reserved	14:9	00h	Reserved
HD Audio Link Short Reset Enable	15	0b	1: Shorten HD Audio Link reset timing for simulation/test purposes 0: Normal reset timing operation

Power Management Capability ID – R – 8 bits – [PCI_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	01h	Hardwired to 0x01. Indicates PCI Power Management Capability.

Next Capability Pointer – R – 8 bits – [PCI_Reg: 51h]			
Field Name	**Bits**	**Default**	**Description**
Next Capability Pointer	7:0	00h	00h: If both MSI and AF capability are disabled 60h: If MSI Capability is enabled 70h: If MSI Capability is disabled and AF Capability is enabled 60h: If both MSI capability and AF capability are enabled

Power Management Capabilities – R – 16 bits – [PCI_Reg: 52h]			
Field Name	**Bits**	**Default**	**Description**
Version	2:0	010b	Hardwired to 010b. Indicates this function complies with Revision 1.1 of the PCI Power Management Interface Specification
PME Clock	3	0b	Hardwired to 0. Indicates that no PCI clock is required for the function to generate PME#.
Reserved	4	0b	Reserved
Device Specific Initialization	5	0b	Hardwired to 0. Indicates that no device specific initialization is required.
Aux Current	8:6	001b	Hardwired to 001b. Indicates 55mA maximum suspend well current is required in the D3cold state.
D1 Support	9	0b	Hardwired to 0. Indicates D1 state is not supported.
D2 Support	10	0b	Hardwired to 0. Indicates D2 state is not supported.
PME Support	15:11	11001b	Hardwired to 11001b. Indicates PME# can be generated from D0 and D3 states.

Power Management Control/Status – R/W – 32 bits – [PCI_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
Power State	1:0	00b	This field is used both to determine the current power state and to set a new power state of the HD Audio controller.
Reserved	7:2	00h	Reserved
PME Enable	8	0b	Enables the function to assert PME#. This bit is in resume well and only cleared on power-on reset.
Reserved	14:9	00h	Reserved
PME Status	15	0b	This bit set when when HD Audio controller asserts the PME# signal, it is independent of the PME Enable bit. Writing a “1” clears this bit. This bit is in resume well and only cleared on power-on reset.
Reserved	31:16	0000h	Reserved

MSI Capability ID – R – 8 bits – [PCI_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	05h	Hardwired to 0x05. Indicates MSI Capability.

Next Capability Pointer – R – 8 bits – [PCI_Reg: 61h]			
Field Name	**Bits**	**Default**	**Description**
Next Capability Pointer	7:0	00h	00h: If AF Capability is disabled 70h: If AF Capability is enabled

MSI Message Control – R/W - 16 bits – [PCI_Reg: 62h]			
Field Name	**Bits**	**Default**	**Description**
MSI Enable	0	0b	Enables MSI if set to 1.
Multiple Message Capable	3:1	0h	Hardwired to 0. Indicates support for one message only.
Multiple Message Enable	6:4	0h	Hardwired to 0. Indicates support for one message only.
64 Bit Address Capability	7	1b	Hardwired to 1. Indicates the ability to generate 64-bit message address.
Reserved	15:8	00h	Reserved

MSI Message Lower Address – R/W - 32 bits – [PCI_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
MSI Message Lower Address	31:2	00000000h	Lower Address used for MSI Message.
Reserved	01:0	00b	Reserved

MSI Message Upper Address – R/W - 32 bits – [PCI_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
MSI Message Upper Address	31:0	00000000h	Upper Address used for MSI Message.

MSI Message Data – R/W - 16 bits – [PCI_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
MSI Message Data	15:00	0000h	Data used for MSI Message.

Advanced Features Capability ID – R/W - 8 bits – [PCI_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
AF Capability ID	7:0	13h	Hardwared to 0x13. Indicates Advanced Features Capability

Next Capability Pointer – R/W - 8 bits – [PCI_Reg: 71h]			
Field Name	**Bits**	**Default**	**Description**
Next Capability Pointer	7:0	00h	Hardwired to 0. Indicates this is the last capability structure in the list.

Advanced Features Length – R/W - 8 bits – [PCI_Reg: 72h]			
Field Name	**Bits**	**Default**	**Description**
AF Length	7:0	06h	Hardwired to 0x06h. Indicates AF Structure Length (bytes).

Advanced Features Capabilities – R/W - 8 bits – [PCI_Reg: 73h]			
Field Name	**Bits**	**Default**	**Description**
FLR Capabilities	0	1b	Hardwired to 1b. Indicates support for Function Level Reset (FLR).
TP Capabilities	1	1b	Hardwired to 1b. Indicates support for Transactions Pending.
Reserved	7:2	00h	Reserved

Advanced Features Control – R/W - 8 bits – [PCI_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
Initiate FLR	0	0b	A write of 1b initiates FLR. FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there. The value read by software from this bit shall always be 0b.
Reserved	7:1	00h	Reserved

Advanced Features Status – R/W - 8 bits – [PCI_Reg: 75h]			
Field Name	**Bits**	**Default**	**Description**
Transaction Pending	0	0b	Transaction Pending (TP): A value of 1b indicates that the function has issued one or more non-posted transactions which have not been completed including non-posted transactions that a target has terminted with retry. A value of 0b indicates that all non-posted transactions have been completed. This field is read only.
Reserved	7:1	00h	Reserved

2.3.2 HD Audio Controller Memory Mapped Registers

The base memory location for these memory mapped registers is specified in the PCI Configuration Upper and Lower Base Adress Registers. The individual registers are then accessible at Base + offset as indicated in the following table. These registers are accessed in byte, word, or dword quantities.

Register Name	Offset Address
Global Capabilities	00h
Minor Version	02h
Major Version	03h
Output Payload Capability	04h
Input Payload Capability	06h
Global Control	08h
Wake Enable	0Ch
Wake Status	0Eh
Global Status	10h
Output Stream Payload Capability	18h
Input Stream Payload Capability	1Ah
Interrupt Control	20h
Interrupt Status	24h
Wall Clock Counter	30h
Stream Synchronization	38h
CORB Lower Base Address	40h
CORB Upper Base Address	44h
CORB Write Pointer	48h
CORB Read Pointer	4Ah
CORB Control	4Ch
CORB Status	4Dh
CORB SIze	4Eh
RIRB Lower Base Address	50h
RIRB Upper Base Address	54h
RIRB Write Pointer	58h
Response Interrupt Control	5Ah
RIRB Control	5Ch
RIRB Status	5Dh
RIRB Size	5Eh
Immediate Command Output Interface	60h
Immediate Command Input Interface	64h
Immediate Command Status	68h
DMA Position Buffer Lower Base Address	70h
DMA Position Buffer Upper Base Address	74h
Input Stream Descriptor 0	
Control	80h
Status	83h
Link Position in Current Buffer	84h
Cyclic Buffer Length	88h
Last Valid Index	8Ch
FIFO Size	90h
Stream Format	92h
Buffer Descriptor Lower Base Address	98h
Buffer Descriptor Upper Base Address	9Ch
Input Stream Descriptor 1	
Control	A0h
Status	A3h
Link Position in Current Buffer	A4h
Cyclic Buffer Length	A8h
Last Valid Index	ACh
FIFO Size	B0h
Stream Format	B2h
Buffer Descriptor Lower Base Address	B8h
Buffer Descriptor Upper Base Address	BCh
Input Stream Descriptor 2	

Register Name	Offset Address
Control	C0h
Status	C3h
Link Position in Current Buffer	C4h
Cyclic Buffer Length	C8h
Last Valid Index	CCh
FIFO Size	D0h
Stream Format	D2h
Buffer Descriptor Lower Base Address	D8h
Buffer Descriptor Upper Base Address	DCh
Input Stream Descriptor 3	
Control	E0h
Status	E3h
Link Position in Current Buffer	E4h
Cyclic Buffer Length	E8h
Last Valid Index	ECh
FIFO Size	F0h
Stream Format	F2h
Buffer Descriptor Lower Base Address	F8h
Buffer Descriptor Upper Base Address	FCh
Output Stream Descriptor 0	
Control	100h
Status	103h
Link Position in Current Buffer	104h
Cyclic Buffer Length	108h
Last Valid Index	10Ch
FIFO Size	110h
Stream Format	112h
Buffer Descriptor Lower Base Address	118h
Buffer Descriptor Upper Base Address	11Ch
Output Stream Descriptor 1	
Control	120h
Status	123h
Link Position in Current Buffer	124h
Cyclic Buffer Length	128h
Last Valid Index	12Ch
FIFO Size	130h
Stream Format	132h
Buffer Descriptor Lower Base Address	138h
Buffer Descriptor Upper Base Address	13Ch
Output Stream Descriptor 2	
Control	140h
Status	143h
Link Position in Current Buffer	144h
Cyclic Buffer Length	148h
Last Valid Index	14Ch
FIFO Size	150h
Stream Format	152h
Buffer Descriptor Lower Base Address	158h
Buffer Descriptor Upper Base Address	15Ch
Output Stream Descriptor 3	
Control	160h
Status	163h
Link Position in Current Buffer	164h
Cyclic Buffer Length	168h
Last Valid Index	16Ch
FIFO Size	170h
Stream Format	172h
Buffer Descriptor Lower Base Address	178h
Buffer Descriptor Upper Base Address	17Ch
Alias Registers	
Wall Clock Counter Alias	2030h
Input Stream Descriptor 0 - Link Position in Current Buffer Alias	2084h
Input Stream Descriptor 1 - Link Position in Current Buffer Alias	20A4h

Register Name	Offset Address
Input Stream Descriptor 2 - Link Position in Current Buffer Alias	20C4h
Input Stream Descriptor 3 - Link Position in Current Buffer Alias	20E4h
Output Stream Descriptor 0 - Link Position in Current Buffer Alias	2104h
Output Stream Descriptor 1 - Link Position in Current Buffer Alias	2124h
Output Stream Descriptor 2 - Link Position in Current Buffer Alias	2144h
Output Stream Descriptor 3 - Link Position in Current Buffer Alias	2164h

Global Capabilities – R – 16 bits - [Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
64 Bit Address Supported	0	1b	Hardwired to 1. Indicates that 64-bit addressing capability is supported by the HD Audio controller for BDL, Data Buffer, Command Buffer, and Response Buffer addresses.
Number of Serial Data Output Signals	2:1	0h	Hardwired to 0. Indicates that one SDO line is supported.
Number of Bidirectional Streams Supported	7:3	0h	Hardwired to 0. Indicates that bidirectional stream is not supported.
Number of Input Streams Supported	11:8	4h	4 Input Streams are supported.
Number of Output Streams Supported	15:12	4h	4 Output Streams are supported.

Minor Version – R – 8 bits - [Mem_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Minor Version	31:2	00000000h	Hardwired to 0.

Major Version – R – 8 bits - [Mem_Reg: 03h]			
Field Name	**Bits**	**Default**	**Description**
Major Version	0	1b	Hardwired to 1.

Output Payload Capability – R – 16 bits - [Mem_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Output Payload Capability	15:0	003Ch	Hardwired to 3Ch. Indicates the total output payload on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48kHz frame. The default link clock speed of 24MHz (double data rate) provides 1000 bits per frame minus 40 bits for command and control, leaving 960 bits (60 words) for data payload.

Input Payload Capability – R – 16 bits - [Mem_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Input Payload Capability	15:0	001Dh	Hardwired to 1Dh. Indicates the total input payload on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48kHz frame. The default link clock speed of 24MHz provides 500 bits per frame minus 36 bits for response, leaving 464 bits (29 words) for data payload.

Global Control – R/W – 32 bits - [Mem_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Controller Reset	0	0b	Writing a 0 to this bit causes the controller to transition to the Reset state. After the hardware has completed sequencing into the Reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit the Reset state and deassert the link RESET# signals. Software is responsible for setting/clearing this bit such that the minimum link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers.
Flush Control	1	0b	Writing a 1 to this bit initiates a flush. The flush is completed when Flush Status is set.
Reserved	7:2	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.
Accepted Unsolicited Response Enable	8	0b	If “1”, Unsolicited Response from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If “0”, Unsolicited Responses are accepted and dropped.
Reserved	31:9	000000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

Wake Enable – R/W – 16 bits - [Mem_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Wake Enable	3:0	0h	This field controls which SDIN signals may generate a wake event in response to a codec State Change event. Bit [0] corresponds to Codec 0 – SDIN[0] Bit [1] corresponds to Codec 1 – SDIN[1] Bit [2] corresponds to Codec 2 – SDIN[2] Bit [3] corresponds to Codec 3 – SDIN[3] These bits are only cleared by a power-on reset.
Reserved	15:4	000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

State Change Status – R/W – 16 bits - [Mem_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
State Change Status Flags	3:0	0h	This field indicates which SDIN signal(s) received a State Change event. Bit [0] corresponds to Codec 0 – SDIN[0] Bit [1] corresponds to Codec 1 – SDIN[1] Bit [2] corresponds to Codec 2 – SDIN[2] Bit [3] corresponds to Codec 3 – SDIN[3] These bits are cleared by writing 1's to them. These bits are only cleared by a power-on reset.
Reserved (R/W)	15:4	000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

Global Status – R/W – 16 bits - [Mem_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved. Software must use 0 for write to this bit.
Flush Status	1	0b	This bit is set to a "1" by hardware to indicate that the flush cycle initiated by setting the Flush Control has completed. Software must write a "1" to clear this bit before the next time Flush Control is set.
Reserved	15:2	0000h	Reserved. Software must use 0's for write to these bits.

Output Stream Payload Capability – R – 16 bits - [Mem_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Output Stream Payload Capability	15:0	003Ch	This field indicates the maximum number of words per frame for any single output stream. This measurement is in 16-bit word quantities per 48 kHz frame. The value must not be greater than the Output Payload Capability register value. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h: No Limit (Stream size is limited only by Output Payload Capability register) 01h: 1 word payload : : FFh: 255 word payload

Input Stream Payload Capability – R – 16 bits - [Mem_Reg: 1Ah]			
Field Name	**Bits**	**Default**	**Description**
Input Stream Payload Capability	15:0	0000h	This field indicates the maximum number of words per frame for any single input stream. This measurement is in 16-bit word quantities per 48 kHz frame. The value must not be greater than the Input Payload Capability register value. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h: No Limit (Stream size is limited only by Input Payload Capability register) 01h: 1 word payload : : FFh: 255 word payload

Interrupt Control – R/W – 32 bits - [Mem_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
Stream Interrupt Enable	7:0	00h	When set to “1”, the individual streams are enabled to generate an interrupt when the corresponding stream status bits are set. A stream interrupt is caused as a result of a buffer with IOC in the BDL entry being completed or as result of FIFO error. Control over the generation of each of these sources is in the associated Stream Descriptor. Bit [0]: Input Stream 0 Bit [1]: Input Stream 1 Bit [2]: Input Stream 2 Bit [3]: Input Stream 3 Bit [4]: Output Stream 0 Bit [5]: Output Stream 1 Bit [6]: Output Stream 2 Bit [7]: Output Stream 3
Reserved	29:8	000000h	Reserved
Controller Interrupt Enable	30	0b	Enables the general interrupt for controller functions. When set to “1’, the controller generates an interrupt when the corresponding status bit gets set due to a Response Interrupt, a Response Buffer Overrun, and Wake events.
Global Interrupt Enable	31	0b	Enables device interrupt generation. When set to “1”, the HD Audio device is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space such as the Interrupt Enable bit in the PCI Configuration Space.

Interrupt Status – R/W – 32 bits - [Mem_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
Stream Interrupt Status	7:0	00h	An “1” indicates that an interrupt condition occurred on the corresponding stream. These bits are cleared by writing 1’s to them. Note: These bits are set regardless of the state of the corresponding Interrupt Enable bits.
Reserved	29:8	000000h	Reserved
Controller Interrupt Status	30	0b	A “1” indicates that an interrupt condition occurred. This bit is cleared by writing a “1” to it. Note that this bit is set regardless of the state of the corresponding Interrupt Enable bit.
Global Interrupt Status	31	0b	This bit is an “OR” of all the interrupt status bits in this register.

Wall Clock Counter – R – 32 bits - [Mem_Reg: 30h]			
Field Name	**Bits**	**Default**	**Description**
Wall Clock Counter	31:0	00000000h	32 bit counter that Is incremented at the link bitclock rate and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to 0 with period of approximately 179 seconds with the nomial 24 MHz bitclock rate.

Stream Synchronization – R/W – 32 bits – [Mem_Reg: 38h]			
Field Name	**Bits**	**Default**	**Description**
Stream Synchronization	7:0	00h	These bits when set, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor. To synchronously start a set of DMA engines, the bits in this register are set to a “1”. The RUN bits for the associated Stream Descriptors can be set to a “1” to start the DMA engines. When all streams are ready, the associated Stream Synchronization bits can all be set to 0 at the same time, and transmission or reception from the link will begin together at the start of the next full link frame. To synchronously stop streams, these bits are set, and the RUN bits in the Stream Descriptors are cleared by software.
Reserved	31:8	000000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

CORB Lower Base Address – R/W – 32 bits – [Mem_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
CORB Lower Base Address Unimplemented Bits	6:0	00h	Hardwired to 0. This forces 128-byte buffer alignment for cache line fetch optimizations.
CORB Lower Base Address	31:7	0000000h	Upper 25 bits of the 32 bits Lower Base address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 1 KB boundary. This register must not be written when the DMA engine is running or the DMA transfer may be corrupted.

CORB Upper Base Address – RW – 32 bits – [Mem_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
CORB Upper Base Address	31:0	00000000h	Upper 32 bits address of the CORB. This register must not be written when the DMA engine is running or the DMA transfer may be corrupted.

CORB Write Pointer – R/W – 16 bits – [Mem_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
CORB Write Pointer	7:0	00h	Software writes the last valid CORB entry offset into this field in dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. This supports up to 256 CORB entries. This field may not be written while the DMA engine is running.
Reserved	15:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

CORB Read Pointer – R/W – 16 bits – [Mem_Reg: 4Ah]			
Field Name	**Bits**	**Default**	**Description**
CORB Read Pointer	7:0	00h	Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. This field may be read while the DMA engine is running.
Reserved	14:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

CORB Read Pointer – R/W – 16 bits – [Mem_Reg: 4Ah]			
Field Name	**Bits**	**Default**	**Description**
CORB Read Pointer Reset	15	0b	Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual prefetched commands in the CORB hardware buffer within the controller. The hardware will physically update this bit to 1 when the CORB pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0, by writing a 0, and then read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.

CORB Control – R/W – 8 bits – [Mem_Reg: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
CORB Memory Error Interrupt Enable	0	0b	If this bit is set, the controller will generate an interrupt if the Memory Error Interrupt bit is set.
Enable CORB DMA Engine	1	0b	0: DMA Stop 1: DMA Run After software writes a “0” to this bit, the hardware may not stop immediately. The hardware will physically update the bit to “0” when the DMA engine is truly stopped. Software must read a “0” from this bit to verify that the DMA engine is truly stopped.
Reserved	7:2	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

CORB Status – R/W – 8 bits – [Mem_Reg: 4Dh]			
Field Name	**Bits**	**Default**	**Description**
CORB Memory error Indication	0	0	If this status bit is set, the controller has detected an error in the pathway between the controller and memory. Writing a “1” to this bit will clear the bit, but a CRST must be performed before operation continues/
Reserved	7:2	0	Reserved. Software must use 0’s for write to these bits.

CORB Size – R/W – 8 bits – [Mem_Reg: 4Eh]			
Field Name	**Bits**	**Default**	**Description**
CORB Size	1:0	10b	These bits have no functional impact to the hardware. This HD Audio controller only supports 256 entries.
Reserved	3:2	00b	Reserved. Software must do a read-modify-write to preserve the value of these bits.
CORB Size Capability	7:4	0100b	Hardwired to 0100b indicating this controller only supports a CORB size of 256 entries.

RIRB Lower Base Address – RW – 32 bits – [Mem_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
RIRB Lower Base Address Unimplemented Bits	6:0	00h	Hardwired to 0. This forces 128-byte buffer alignment for cache line fetch optimizations.
RIRB Lower Base Address	31:7	0000000h	Upper 25 bits of the 32 bits Lower Base Address of the Response Input Ring Buffer, allowing the RIRB Base Address to be assigned on any 2 KB boundary. This register must not be written when the DMA engine is running or the DMA transfer may be corrupted.

RIRB Upper Address – RW – 32 bits – [Mem_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
RIRB Upper Base Address	31:0	00000000h	Upper 32 bits address of the RIRB. This register must not be written when the DMA engine is running or the DMA transfer may be corrupted.

RIRB Write Pointer – RW – 16 bits – [Mem_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
RIRB Write Pointer	7:0	00h	This field indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in two dwords since each RIRB entry is two dwords. This field may be read while the DMA engine is running.
Reserved	14:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.
RIRB Write Pointer Reset	15	0b	Software writes a “1” to this bit to reset the RIRB Write Pointer to 0’s. The DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.

RIRB Response Interrupt Count – R/W – 16 bits – [Mem_Reg: 5Ah]			
Field Name	**Bits**	**Default**	**Description**
N Response Interrupt Count	7:0	00h	0x01: 1 Response sent to RIRB : 0xFF: 255 Responses sent to RIRB 0x00: 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note: Each response occupies two dwords in the RIRB. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.
Reserved	15:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

RIRB Control – R/W – 8 bits – [Mem_Reg: 5Ch]			
Field Name	**Bits**	**Default**	**Description**
Response Interrupt Control	0	0b	0: Disable Interrupt 1: Generate an interrupt after N number of Responses are sent to the RIRB buffer or when an empty Response slot is encountered on all SDIN_x inputs after a frame which return a response (whichever occurs first). The N counter is reset when the interrupt is generated.
RIRB DMA Enable	1	0b	0: DMA Stop 1: DMA Run
Response Overrun Interrupt Control	2	0b	If this bit is set, the hardware will generate an interrupt when the Response Overrun Interrupt Status is set.
Reserved	15:3	0000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

RIRB Status – R/W – 8 bits – [Mem_Reg: 5Dh]			
Field Name	**Bits**	**Default**	**Description**
Response Interrupt	0	0b	Hardware sets this bit to “1” when an interrupt has been generated after N number of Responses are sent to the RIRB buffer or when empty Response slot is encountered on all SDIN_x inputs (whichever occurs first). Software clears this bit by writing a “1” to this bit.
Reserved	2	0b	Reserved. Software must use 0’s for write to these bits.
Response Overrun Interrupt Status	2	0b	Hardware sets this bit to a “1’ when an overrun occurs in the RIRB. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Software clears this bit by writing a “1” to it.
Reserved	7:3	00h	Reserved. Software must use 0’s for write to these bits.

RIRB Size – R/W – 8 bits – [Mem_Reg: 5Eh]			
Field Name	**Bits**	**Default**	**Description**
RIRB Size	1:0	10b	These bits have no functional impact to the hardware. This HD Audio controller only supports 256 entries.
Reserved	3:2	00b	Reserved. Software must do a read-modify-write to preserve the value of these bits.
RIRB Size Capability	7:4	0100b	Hardwired to 0100b indicating this controller only supports a RIRB size of 256 entries.

Immediate Command Output Interface – R/W – 32 bits – [Mem_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
Immediate Command Write	31:0	00000000h	The value written into this register is used as the verb to be sent out over the link when the ICB (Immediate Command Busy) bit is set to “1”. Software must ensure that the ICB bit is cleared before writing a value into this register or undefined behavior wil result. Reads from this register will always return 0’s.

Immediate Command Input Interface – R/W – 32 bits – [Mem_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
Immediate Response Read	31:0	00000000h	This register contains the value from the last response to come in over the link. If multiple codecs responsed in the same frame, which one of the responses that will be saved is indeterminate.

Immediate Command Input Interface – R/W – 16 bits – [Mem_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
Immediate Command Status	0	0b	This bit is a 0 when the controller can accept an immediate command. Software must wait for this bit to be 0 before writing a value in the ICW register. This bit will be clear (indicating "ready") when the following conditions are met: (1) the link is running, (2) the CORB is not active (CORBRP = CORBWP or CORBEN is not set), and (3) there is not an immediate command already in the queue waiting to be sent. Writing this bit to 1 will cause the contents of the ICW register to be sent as a verb in the next frame. Once a response is received the IRV bit will be set and this bit will be cleared indicating ready to transmit another verb.
Immediate Result Valid	1	0b	This bit is set to a 1 by hardware when a new response is latched into the IRR (Immediate Response Read) register. Software must clear this bit before issuing a new command by writing a one to it so that the software may determine when a new response has arrived.
Reserved	2	0b	Reserved. Software must use 0's for write to these bits.
Immediate Response Result Unsolicited	3	0b	Indicates whether the response latched in the Immediate Response Input Register is a solicited or unsolicited response.
Immediate Response Result Address	7:4	0h	The address of the codec which sent the response currently latched into the Immediate Response Input.
Reserved	15:8	00h	Reserved. Software must use 0's for write to these bits.

DMA Position Lower Base Address – R/W – 32 bits – [Mem_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
DMA Position Buffer Enable	0	0b	When this bit is set to a "1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically. Software can use this value to know what data in memory is valid data.
DMA Position Lower Base Address Unimplemented Bits	6:1	00h	Hardwired to 0. This forces 128-byte buffer alignment for cache line fetch optimizations.
DMA Position Lower Base Address	31:7	0000000h	Contains the upper 25 bits of the ower 32 bits of the DMA Position Buffer Base Address. This same address is used by the Flush Control, and must be programmed with a valid value before the Flush Control is initiated.

DMA Position Upper Base Address – R/W – 32 bits – [Mem_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
DMA Position Upper Base Address	31:0	00000000h	Upper 32 bits of the DMA Position Buffer Base Address. This same address is used by the Flush Control, and must be programmed with a valid value before the Flush Control is initiated.

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor Control – R/W – 24 bits Input Stream 0 - [Mem_Reg: 80h] Input Stream 1 - [Mem_Reg: A0h] Input Stream 2 - [Mem_Reg: C0h] Input Stream 3 - [Mem_Reg: E0h] Output Stream 0 - [Mem_Reg: 100h] Output Stream 1 - [Mem_Reg: 120h] Output Stream 2 - [Mem_Reg: 140h] Output Stream 3 - [Mem_Reg: 160h]			
Field Name	**Bits**	**Default**	**Description**
Stream Reset	0	0b	Writing a “1” causes the corresponding stream to be reset. The Stream Descriptor registers (except this bit), FIFO’s and cadence generator for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset stte, it will report a “1” in this bit. Software must read a “1’ from this bit to verify that the stream is in reset. Writing a “0” causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a “0” in this bit. Software must read a “0” from this bit before accessing any of the stream registers. The Run bit must be cleared before asserting SRST (Stream Reset).
Stream Run	1	0b	When set to “1”, the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. When cleared to “0”, the DMA engine associated with this input stream will be disabled. If the corresponding SSYNC bit is “0”, input stream data will be taken from the link and moved to the FIFO and an over-run may occur.
Interrupt On Completion Enable	2	0b	Controls whether an interrupt is generated when the Buffer Completion Interrupt Status is set
FIFO Error Interrupt Enable	3	0b	Controls whether an interrupt is generated when the FIFO Error is set.
Descriptor Error Interrupt Enable	4	0b	Controls whether an interrupt is generated when the Descriptor Error Status is set.
Reserved	15:5	000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.
Stripe Control	17:16	00b	The hardware only supports one SDO, this field has no functional impact.
Traffic Priority	18	0b	If set to “1”, it will cause the controller to generate non-snooped traffic.
Bidirectional Direction Control	19	0b	The hardware does not support bidirection, this field has no impact.

Stream Descriptor Control – R/W – 24 bits Input Stream 0 - [Mem_Reg: 80h] Input Stream 1 - [Mem_Reg: A0h] Input Stream 2 - [Mem_Reg: C0h] Input Stream 3 - [Mem_Reg: E0h] Output Stream 0 - [Mem_Reg: 100h] Output Stream 1 - [Mem_Reg: 120h] Output Stream 2 - [Mem_Reg: 140h] Output Stream 3 - [Mem_Reg: 160h]			
Field Name	**Bits**	**Default**	**Description**
Stream Number	23:20	0h	The value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal. When an input stream is detected on any of the SDIN_x signals that match this value, the data are loaded into the FIFO associated with this descriptor. 0000: Reserved 0001: Stream 1 : 1111: Stream 15

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor Status – R/W – 8 bits Input Stream 0 - [Mem_Reg: 83h] Input Stream 1 - [Mem_Reg: A3h] Input Stream 2 - [Mem_Reg: C3h] Input Stream 3 - [Mem_Reg: E3h] Output Stream 0 - [Mem_Reg: 103h] Output Stream 1 - [Mem_Reg: 123h] Output Stream 2 - [Mem_Reg: 143h] Output Stream 3 - [Mem_Reg: 163h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved. Software must use 0's for write to these bits.
Buffer Completion Interrupt Status	2	0b	For an Output Stream engine, this bit is set to "1" by the hardware after the last byte of data has been fetched from memory and put into DMA FIFO and the current descriptor has the IOC bit set. For an Input Stream engine, this bit is set to "1" by the hardware after the last byte of data has been removed from the DMA FIFO and the current descriptor has the IOC bit set. This bit is cleared by writing a "1" to this bit.
FIFO Error	3	0b	Set when a FIFO error occurs regardless of the FIFO Error Interrupt Enable bit. This bit is cleared by writing a "1" to this bit.
Descriptor Error	4	0b	During the fetch of a descriptor, an error has occurred.
FIFO Ready	5	0b	For an Output Stream, the controller hardware will set this bit to a "1" while the output DMA FIFO contains enough data to maintainthe stream on the link.
Reserved	7:6	00b	Reserved. Software must use 0's for write to these bits.

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor Link Position in Buffer – R – 32 bits Input Stream 0 - [Mem_Reg: 84h] Input Stream 1 - [Mem_Reg: A4h] Input Stream 2 - [Mem_Reg: C4h] Input Stream 3 - [Mem_Reg: E4h] Output Stream 0 - [Mem_Reg: 104h] Output Stream 1 - [Mem_Reg: 124h] Output Stream 2 - [Mem_Reg: 144h] Output Stream 3 - [Mem_Reg: 164h]			
Field Name	**Bits**	**Default**	**Description**
Link Position in Buffer	31:0	00000000h	This field indicates the number of bytes that have been received off the link.

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor Cyclic Buffer Length – R/W – 32 bits Input Stream 0 - [Mem_Reg: 88h] Input Stream 1 - [Mem_Reg: A8h] Input Stream 2 - [Mem_Reg: C8h] Input Stream 3 - [Mem_Reg: E8h] Output Stream 0 - [Mem_Reg: 108h] Output Stream 1 - [Mem_Reg: 128h] Output Stream 2 - [Mem_Reg: 148h] Output Stream 3 - [Mem_Reg: 168h]			
Field Name	**Bits**	**Default**	**Description**
Cyclic Buffer Length	31:0	00000000h	Indicates the number of bytes in the complete cyclic buffer. Link Position in Buffer will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. Once the Run bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or undefined events will occur.

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor Last Valid Index – R/W – 16 bits Input Stream 0 - [Mem_Reg: 8Ch] Input Stream 1 - [Mem_Reg: ACh] Input Stream 2 - [Mem_Reg: CCh] Input Stream 3 - [Mem_Reg: ECh] Output Stream 0 - [Mem_Reg: 10Ch] Output Stream 1 - [Mem_Reg: 12Ch] Output Stream 2 - [Mem_Reg: 14Ch] Output Stream 3 - [Mem_Reg: 16Ch]			
Field Name	**Bits**	**Default**	**Description**
Last Valid Index	7:0	00h	The value written to this register indicates the index for the last valid Buffer Descriptor in BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI (Last Valid Index) must be “1”; that is, there must be at least two valid entries in the BDL before DMA operations can begin. This value should not be modified except when the Run bit is “0”.
Reserved	15:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor FIFO Size – R – 16 bits Input Stream 0 - [Mem_Reg: 90h] Input Stream 1 - [Mem_Reg: B0h] Input Stream 2 - [Mem_Reg: D0h] Input Stream 3 - [Mem_Reg: F0h] Output Stream 0 - [Mem_Reg: 110h] Output Stream 1 - [Mem_Reg: 130h] Output Stream 2 - [Mem_Reg: 150h] Output Stream 3 - [Mem_Reg: 170h]			
Field Name	**Bits**	**Default**	**Description**
FIFO Size	15:0	00h	For Output Stream, the FIFO Size varies between 32 dwords to 256 dwords depending on the Stream Format. For Input Stream, the FIFO Size is fixed at 64 dwords.

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor Format – R/W – 16 bits Input Stream 0 - [Mem_Reg: 92h] Input Stream 1 - [Mem_Reg: B2h] Input Stream 2 - [Mem_Reg: D2h] Input Stream 3 - [Mem_Reg: F2h] Output Stream 0 - [Mem_Reg: 112h] Output Stream 1 - [Mem_Reg: 132h] Output Stream 2 - [Mem_Reg: 152h] Output Stream 3 - [Mem_Reg: 172h]			
Field Name	**Bits**	**Default**	**Description**
Number of Channels	3:0	0h	Number of channels in each frame of the stream. 0000: 1 0001: 2 : 1111: 16
Bits per Sample	6:4	0h	000: 8 bits 001: 16 bits 010: 20 bits 011: 24 bits 100: 32 bits 101: 111: Reserved
Reserved	7	0b	Reserved. Software must do a read-modify-write to preserve the value of these bits.
Sample Base Rate Divisor	10:8	000b	000: Divide by 1 (48 kHz, 44.1 kHz) 001: Divide by 2 (24 kHz, 22.05 kHz) 010: Divide by 3 (16 kHz, 32 kHz) 011: Divide by 4 (11.025 kHz) 100: Divide by 5 (9.6 kHz) 101: Divide by 6 (8 kHz) 110: Divide by 7 111: Divide by 8 (6 kHz)
Sample Base Rate Multiple	13:11	000b	000: x1 (48 kHz, 44.1 kHz) 001: x2 (96 kHz, 88.2 kHz, 32 kHz) 010: x3 (144 kHz) 011: x4 (192 kHz, 176.4 kHz) 101 – 111: Reserved
Sample Base Rate	14	0b	0: 48 kHz 1: 44.1 kHz
Reserved	15	0b	Reserved

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor BDL Pointer Lower Base Address – R/W – 32 bits Input Stream 0 - [Mem_Reg: Base + 98h] Input Stream 1 - [Mem_Reg: Base + B8h] Input Stream 2 - [Mem_Reg: Base + D8h] Input Stream 3 - [Mem_Reg: Base + F8h] Output Stream 0 - [Mem_Reg: Base + 118h] Output Stream 1 - [Mem_Reg: Base + 138h] Output Stream 2 - [Mem_Reg: Base + 158h] Output Stream 3 - [Mem_Reg: Base + 178h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	6:0	00h	Hardwired to 0's to force 128 byte alignment of the BDL.
Buffer Descriptor List Lower Base Address	31:7	0000000h	Upper 25 bits of the lower 32 bit address of the Buffer Descriptor List. This value should not be modified except when the Run bit is "0".

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor BDL Pointer Upper Base Address – R/W – 32 bits Input Stream 0 - [Mem_Reg: 9Ch] Input Stream 1 - [Mem_Reg: BCh] Input Stream 2 - [Mem_Reg: DCh] Input Stream 3 - [Mem_Reg: FCh] Output Stream 0 - [Mem_Reg: 11Ch] Output Stream 1 - [Mem_Reg: 13Ch] Output Stream 2 - [Mem_Reg: 15Ch] Output Stream 3 - [Mem_Reg: 17Ch]			
Field Name	**Bits**	**Default**	**Description**
Buffer Descriptor List Upper Base Address	31:0	00000000h	Upper 32 bit address of the Buffer Descriptor List. This value should not be modified except when the Run bit is "0".

Wall Clock Counter Alias – R – 32 bits – [Mem_Reg: 2030h]			
Field Name	**Bits**	**Default**	**Description**
Wall Clock Counter Alias	31:0	00000000h	An alias of the Wall Clock Counter register at offset 0x30. It behaves exactly the same as if the Wall Clock Counter register were being read directly.

Note: To avoid repetition, the table below applies to 8 registers as indicated.

Stream Descriptor Link Position in Buffer Alias – R – 32 bits Input Stream 0 - [Mem_Reg: 2084h] Input Stream 1 - [Mem_Reg: 20A4h] Input Stream 2 - [Mem_Reg: 20C4h] Input Stream 3 - [Mem_Reg: 20E4h] Output Stream 0 - [Mem_Reg: 2104h] Output Stream 1 - [Mem_Reg: 2124h] Output Stream 2 - [Mem_Reg: 2144h] Output Stream 3 - [Mem_Reg: 2164h]			
Field Name	**Bits**	**Default**	**Description**
Link Position in Buffer Alias	31:0	00000000h	An alias of the Link Position in Buffer register of each Stream Descriptor.

2.4 SD Controller Registers

SD controller sits on bus 0, device 0x14, function 7.

2.4.1 SD PCI Configuration Registers

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID/Class Code	08h
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
BIST	0Fh
Base Address Reg 0	10h
Subsystem ID & Subsystem Vendor ID	2Ch
Capabilities Pointer	34h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Slot Imformation	40h
Capability ID	80h
Next Item Ptr	81h
Power Management Capabilities (PMC)	82h
Power Management Control/Status (PMCSR)	84h
PMCSR PCI to PCI Bridge Support (PMCSR_BSE)	86h
PMC_Data	87h
SD_PCI_MSI_CAP_HEADER	90h
SD_PCI_MSI_CTRL	92h
SD_PCI_MSI_ADDR	94h
SD_PCI_MSI_U_ADDR	98h
SD_PCI_MSI_DATA	9Ch
Card Detection Control	A0h
SD_CAPABILITY_0	A4h
SD_CAPABILITY_1	A8h
SD_CONTROL	ACh
SD_DEBUG_REG	B0h
SD_ADMA_IF_CONTROL	C0h

Vendor ID- R - 16 bits - [PCI_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Vendor ID

Vendor ID Register: This register holds a unique 16-bit value assigned to a vendor, and combined with the device ID, it identifies any PCI device.

Device ID - R - 16 bits - [PCI_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Devide ID	15:0	7806h	Device ID

Device ID Register: This register holds a unique 16-bit value assigned to a device, and together with the vendor ID, it identifies any PCI device.

Command - RW - 16 bits - [PCI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
IO Space	0	0b	I/O Access Enable. This function is not implemented. This bit is always 0.
Memory Space	1	0b	Memory Access Enable. 1=Enable, 0=Disable
Bus Master	2	0b	Master Enable. Bus master function enable. 1=Enable, 0=Disable.
Special Cycles	3	0b	Special Cycle recognition Enable. This feature is not implemented and this bit is always 0.
Memory Write and Invalidate Enable	4	0b	Memory Write and Invalidate Enable. Not implemented. This bit is always 0.
VGA Palette Snoop	5	0b	VGA Palette Snoop Enable. Bolton does not need to snoop VGA palette cycles. This bit is always 0.
Parity Error Response	6	0b	PERR# (Response) Detection Enable bit - If set to 1, Bolton asserts PERR# when it is the agent receiving data AND it detects a parity error. PERR# is not asserted if this bit is 0.
Stepping Control	7	0b	Wait Cycle enable - Bolton does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
SERR# Enable	8	0b	SERR# enable - If set to 1, Bolton asserts SERR# when it detects as address parity error.
Fast Back-tp-Back Enable	9	0b	Fast Back-to-back enable. Bolton only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
Reserved	15:10	00h	

Command Register: The PCI specification defines this register to control a PCI device's ability to generate and respond to PCI cycles. Writes to this register except bit 6, have no effect. Bit[3:0]=0fh and read only

Status - RW - 16 bits - [PCI_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	
Capabilities List	4	1b	This bit is shown as 1b if either MSI or PMC capability is enabled; otherwise, it will return 0b
Reserved	7:5	0h	
Master Data Parity Error	8	0h	Data Parity reported – Set to 1 if Bolton detects PERR# asserted while acting as PCI master (whether PERR# was driven by Bolton or not.)

Status - RW - 16 bits - [PCI_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Device Select Timing	10:9	1h	DEVSEL# timing – Read only bits indicating DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
Signaled Target Abort	11	0b	Signaled Target Abort – This bit is set to 1 when Bolton signals Target Abort.
Received Target Abort	12	0b	Received Target Abort – This bit is set to 1 when a Bolton generated PCI cycle (Bolton is the PCI master) is aborted by a PCI target. Cleared by writing a 1 to it.
Received Master Abort	13	0b	Received Master Abort Status. Set to 1 when Bolton acts as a PCI master and aborts a PCI bus memory cycle. Cleared by writing a 1 to this bit.
Signaled System Error	14	0b	SERR# status. This bit is set to 1, when Bolton detects a PCI address parity error.
Detected Parity Error	15	0b	Detected Parity Error. This bit is set to 1 when Bolton detects a parity error.

Status Register: The PCI specification defines this register to record status information for PCI related events. This is a read/write register. However, writes can only reset bits. A bit is reset when the register is written and the data in the corresponding bit location is a 1.

Revision ID/Class Code - R - 8 bits - [PCI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	00h	These bits are hardwired to 00h to indicate the revision level of the chip design
Interface Code	15:8	01h	00h: Standard Host not supported DMA 01h: Standard Host supported DMA 02h: Vendor unique SD Host Controller We want to have a backdoor method to make this to be programmable for debugging purpose
Sub Class	23:16	05h	For SD host controller
Class Code	31:24	08h	Basic Class

Cache Line Size - R - 8 bits - [PCI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	Cache Line Size.

Cache Line Size Register: This register specifies the system cache line size. This register is not implemented.

Latency Timer - R - 8 bits - [PCI_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Latency Timer	7:0	00h	Latency Timer.

Latency Timer Register: This register specifies the value of the Latency Timer in units of PCICLKs.

Header Type - R - 8 bits - [PCI_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	80h	Header Type.

Header Type Register: This register identifies the type of the predefined header in the configuration space. Since Bolton is a multifunction device, the most significant bit is set.

BIST- R - 8 bits - [PCI_Reg: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
BIST	7:0	00h	BIST.

Built-in Self Test Register: This register is used for control and status for Built-in Self Test. LPC has no BIST modes.

Base Address Reg 0- RW* - 32 bits - [PCI_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 0	31:8	0000_00h	Base address register 0.
Reserved	7:4	0000b	Reserved
Prefetchable	3	0b	Fix to 0. Indicate can not prefetch.
Type	2:1	00b	00h when PCI_Reg ACh bit 3 is 0, indicate 32-bit address 10h when PCI_Reg ACh bit 3 is 1, indicate 64-bit address
Space Indicator	0	0b	Fix to 0. Indicate mapped to the memory space

Upper Base Address Reg 0- RW* - 32 bits - [PCI_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 0	31:0	0000_0000h	Upper 32 bit of Base address register 0. Valid when PCI_Reg ACh bit 3 is 1. Should return all 0's when PCI_Reg ACh bit 3 is 0 and read only.

Subsystem ID & Subsystem Vendor ID - Wo/Ro - 32 bits - [PCI_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	1022h	Subsystem Vendor ID.
Subsystem ID	31:16	7806h	Subsystem ID.

This 4-byte register is a write-once & read-only afterward register. The BIOS writes this register once (all 4 bytes at once) and software reads its value (when needed).

Capabilities Pointer - R - 32 bits - [PCI_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	80h	Default is 00h if no capability is enabled. The value of it depends on the Capabilities Enable bit in PCI_CONFIG_REG[0xAC]. When both MSI and PMC capability are disabled, 00h When both MSI and PMC capability are enabled, 80h When only MSI cap is enabled, 80h When only PMC cap is enabled, 90h
Reserved	31:8	000000h	

Interrupt Line - RW - 32 bits - [PCI_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	Interrupt Line.

Interrupt Pin - R - 32 bits - [PCI_Reg: 3Dh]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin	7:0	01h	Interrupt pin. Can be backdoor programmed if BACKDOOR_INT_PIN (PCI_Reg: Ach[5]) is set.
Reserved	31:8	000000h	

Slot Information - RW - 8 bits - [PCI_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0h	
First Base Address Register Number	2:0	000b	Up to 6 base addresses can be specified in single configuration. These bits indicate the first base address register number assigned to SD Host Controller register set. In the case of single function and multiple register sets, contiguous base addresses are used. Bits [6:4] (Number Of Slots) specifies the number of base addresses. 000b: Base Address 10h (BAR0) 001b: Base Address 14h (BAR1) 010b: Base Address 18h (BAR2) 011b: Base Address 1Ch (BAR3) 100b: Base Address 20h (BAR4) 101b: Base Address 24h (BAR5)
Reserved	3	0b	
Number of Slots	6:4	000b	Number of slots supported. These bits indicate the number of slots the Host Controller supports. In the case of a single function, a maximum of 6 slots can be assigned. 000b: 1 slot 001b: 2 slots 010b: 3 slots 011b: 4 slots 100b: 5 slots 101b: 6 slots
Reserved	7	0b	

SD_PCI_MSI_CAP_HEADER - R -16 bits - [SD_PCI_CFG: 80h]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	05h	A value of 05h indicates MSI
CAP_NXT_PTR	15:8	00h	Pointer to the next item in the capabilities list. The value of it depends on the Capabilities Enable bit in PCI_CONFIG_REG[0xAC]. If both MSI and PMC capabilities are enabled, 90h; else 00h

SD_PCI_MSI_CTRL- RW - 16bits - [SD_PCI_CFG: 82h]			
Field Name	**Bits**	**Default**	**Description**
MSI_Enable	0	0b	MSI Enable.
Mul_Msg_Cap	3:1	000b	Multiple Message Capable.
Mul_Msg_En	6:4	000b	Multiple Message Enable.
Extend_Addr_En	7	0b	64-bit Address Capable.
MSI_CTRL_Reserved	15:8	00h	Reserved

SD_PCI_MSI_ADDR - RW - 16bits - [SD_PCI_CFG: 84h]			
Field Name	**Bits**	**Default**	**Description**
MSI_ADDR_Reserved	1:0	00b	Reserved
Msg_Addr	31:2	00000000h	Message Address.

SD_PCI_MSI_U_ADDR - RW - 16bits - [SD_PCI_CFG: 88h]			
Field Name	**Bits**	**Default**	**Description**
Msg_Upper_Addr	31:0	0	Message Upper Address. Bits [15:0] of this register will be MSI_DATA if 32 bit MSI is selected.

SD_PCI_MSI_DATA - RW - 16bits - [SD_PCI_CFG: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
Msg_Data	15:0	0	Message Data.

Power Management Capability Register- R - 32 bits - [PCI_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
CAP ID	7:0	01h	Power management.
CAP Next Pointer	15:0	00h	No other capability.
Version	18:16	011b	A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.
PME Clock	19	0b	PME Clock - When this bit is a "1", it indicates that the function relies on the presence of the PCI clock for PME# operation. When this bit is a "0", it indicates that no PCI clock is required for the function to generate PME#. Functions that do not support PME# generation in any state must return "0" for this field.
Reserved	20	0b	
DSI	21	0b	DSI - The Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it.
Aux Current	24:22	000b	This 3 bit field reports the 3.3V auxiliary current requirements for the PCI function.
D1 Support	25	0b	If this bit is a "1", this function supports the D1 Power Management State.
D2 Support	26	0b	If this bit is a "1", this function supports the D2 Power Management State.
PME Support	31:27	00000b	This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1 bit(13) X X1XXb - PME# can be asserted from D2 bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold

PMCSR - R - 32 bits - [PCI_Reg: 94h]			
Field Name	**Bits**	**Default**	**Description**
Power	1:0	00b	This 2-bit field is used to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.
Reserved	2	0b	
No Soft Reset	3	0b	When set ("1"), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset.
Reserved	7:4	0000b	
PME En	8	0b	A "1" enables the function to assert PME#. When "0", PME# assertion is disabled.
Data Select	12:9	0000b	This 4-bit field is used to select which data is to be reported through the Data register and Data_Scale field.
Data Scale	14:13	00b	This 2-bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field will vary depending on which data value has been selected by the Data_Select field.
PME Status	15	0b	This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit.

PMCSR_BSE - R - 32 bits - [PCI_Reg: 96h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	5:0	000000b	
B2 B3#	6	0b	B2/B3 support for D3hot.
BPCC En	7	0b	Bus Power/Clock Control Enable.

PMCData - R - 32 bits - [PCI_Reg: 97h]			
Field Name	**Bits**	**Default**	**Description**
Data	7:0	00h	This register is used to report the state dependent data requested by the Data_Select field. The value of this register is scaled by the value reported by the Data_Scale field.

Card_Detection - RW - 16 bits - [SD_PCI_CFG : A0h]			
Field Name	**Bits**	**Default**	**Description**
CD_SELECT	0	0b	Read Only. Status of input CD_SELECT pin. 0: Select CD Pin 1: Select DAT3 Pin
CD_CTRL_SIG	1	1b	When CD DETECT register setting is 1, programming this register will control the output of the CD_CTRL_SIG pin. When selecting DAT3 Pin as card detect pin, system should clear this register before using DAT3 as data input.

SD_CAPABILITY_0 - RW - 32 bits – [SD_PCI_CFG: A4h]			
Field Name	**Bits**	**Default**	**Description**
TMO_FREQ	5:0	00h	Time out clock freq. Valid when CAPSEL=1
TMO_UNIT	6	0b	Time Out clock select. Valid when CAPSEL=1 0 = Time out clock from internal 1 = Time out clock from external
BASE_FREQ	12:7	00h	Base clock frequency. Valid when CAPSEL=1
MAX_LEN	14:13	00b	Maximum block length. Valid when CAPSEL=1
MMC4_SUP	15	0b	MMC 8-bit support. Valid when CAPSEL=1 0 = MMC 8bit is not supported 1 = MMC 8bit is supported
ADMA_SUP	16	0b	Advanced DMA support. Valid when CAPSEL=1 0 = ADMA is not supported 1 = ADMA is supported
HSPSUP	17	0b	High speed support. Valid when CAPSEL=1. 0 = High speed is not supported 1 = High speed is supported
DMASUP	18	0b	DMA support. Valid when CAPSEL=1 0 = DMA is not supported 1 = DMA is supported
SUSSUP	19	0b	Sunpend/Resume support. Valid when CAPSEL=1 0 = Suspend/Resume is not supported 1 = Suspend/Resume is supported
VSUP	22:20	0b	Voltage support. Valid when CAPSEL=1 0 = 3.3V 1 = 3.0V 2 = 1.8V
A64BSUP	23	0b	64-bit system address support.
ADMA2_SUP	24	0b	Advanced DMA 2 support.
CE_ATA_SUP	25	0b	CE_ATA support. Valid when CAPSEL=1 0 = CE_ATA is not supported 1 = CE_ATA_SUP is supported

SD_CAPABILITY_0 - RW - 32 bits – [SD_PCI_CFG: A4h]			
Field Name	**Bits**	**Default**	**Description**
BUF256X2_SUP	26	0b	Buffer 256Bx2 support. Valid when CAPSEL=1 0 = BUF 256x2 is not supported 1 = BUF 256x2 is supported
BIGENDIAN	27	0b	Endian select. 0 = Big endian is supported 1 = Little endian is supported
UNUSED	30:28	000b	This field is not used.
CAPSEL	31	0b	Capability Input select. 0 = Constant value of package file is inputted 1 = Load from external pins

SD Capability Register.
This register contains capability control of the SD IP core.

SD_CAPABILITY_1 - RW - 32 bits – [SD_PCI_CFG: A8h]			
Field Name	**Bits**	**Default**	**Description**
MAX_C	23:0	000000h	Maximum current. Valid when CAPSEL=1
UNUSED	31:24	00h	This field is not used.

SD maximum capability register.

SD_CONTROL - R - 32 bits - [PCI_Reg: ACh]			
Field Name	**Bits**	**Default**	**Description**
al_prefetch_en	0	1b	A-Link prefetch enable.
CAP_MSI_EN	1	1b	MSI capability enable bit.
CAP_PWC_EN	2	0b	PWC capability enable bit.
BADDR_64_EN	3	1b	64 bit PCI base address enable.
MSI_64_EN	4	1b	64 bit MSI enable.
	5	0b	

SD control register

SD_DEBUG_REG - RW - 32 bits - [PCI_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
			.
SD_HOLD_TIME_FIX	11:10	00b	SD hold time fix enable. 00: Disable 01: Reserved 10: Reserved 11: Enable
			.

SD_ADMA_IF_CONTROL - R - 8 bits - [PCI_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
ADMA_TRAN_MODE	2:0	011b	ADMA interface transfer mode. 000: INCR4 001: INCR8 010: INCR16 011: INCR 1xx: Single
Reserved	6:3	0000b	Reserved.
ADMA_LOCK_MODE	7	0b	ADMA interface lock mode. 0: LOCK is not inserted 1: LOCK is inserted

2.4.2 SD Host Standard Registers

Register Name	Group:Offset
SDHC_SYS_ADDR	00h
SDHC_BLK_CS	04h
SDHC_CMD_ARG	08h
SDHC_CMD_TRN	0Ch
SDHC_RESP1_0	10h
SDHC_RESP3_2	14h
SDHC_RESP5_4	18h
SDHC_RESP7_6	1Ch
SDHC_BUFFER	20h
SDHC_PRSNT_STATE	24h
SDHC_CTRL1	28h
SDHC_CTRL2	2Ch
SDHC_INT_STATUS	30h
SDHC_INT_MASK	34h
SDHC_SIG_MASK	38h
SDHC_ACMD12_ERR	3Ch
SDHC_CAPABILITY	40h
SDHC_CURR_CAPABILITY	48h
SDHC_FORCE_EVT	50h
SDHC_ADMA_ERR	54h
SDHC_ADMA_SAD	58h
SDHC_VER_SLOT	FCh

SDHC_SYS_ADDR - RW - 32 bits - SD_HOST_STD:0x00			
Field Name	**Bits**	**Default**	**Description**
SYS_ADDR0	15:0	0000h	System Address lower bits. Updating this register clears DMA_WAIT.
SYS_ADDR1	31:16	0000h	System Address upper bits. Updating this register clears DMA_WAIT. It indicates system memory address for DMA. When DMA transfer detects the DMA Buffer Boundary specified by the Host DMA Buffer Boundary in the Block Size register, SD controller asserts DMA_WAIT. Also SD controller generates DMA interrupt at this time when corresponding bits in the Normal Interrupt Status Enable register and Normal Interrupt Signal Enable register are set. While ADMA is enabled, this register will not be used.

SDHC_BLK_CS - RW - 32 bits - SD_HOST_STD:0x04			
Field Name	**Bits**	**Default**	**Description**
BLK_SIZE	11:0	000h	Transfer Data Length (max. block size is 2K bytes). When the CE-ATA Enable bit of the CE-ATA Control register is set, a value of 0x000 indicates block size of 4K bytes.
DMA_BUF_BNDRY	14:12	000b	Host DMA Buffer Boundary. Indicates the contiguous buffer size in the system memory. When the boundary is reached, DMA interrupt will be generated. 0 = 4K bytes 1 = 8K bytes 2 = 16K bytes 3 = 32K bytes 4 = 64K bytes 5 = 128K bytes 6 = 256K bytes 7 = 512K bytes
UNUSED0 (R)	15	0b	This field is not used.
BLK_CNT	31:16	0000h	Block Count. It indicates block count of multiple data transfer. It is enabled when the Block Count Enable bit (D01) in the Transfer Mode register is set to 1. It is decremented after each block data transmission. During infinite data transmission, setting of this bit is meaningless.

Block Size and Block Count.

SDHC_CMD_ARG - RW - 32 bits - SD_HOST_STD:0x08			
Field Name	**Bits**	**Default**	**Description**
ARGUMENT0	15:0	0000h	Lower bits.
ARGUMENT1	31:16	0000h	Upper bits. Command Argument. Command arguments specified as bits [39:8] of the command format.

SDHC_CMD_TRN - RW - 32 bits - SD_HOST_STD:0x0C			
Field Name	**Bits**	**Default**	**Description**
DMA_EN	0	0b	DMA Enable 0 = Disable 1 = Enable
BLK_CNT_EN	1	0b	Block Count Enable 0 = Disable 1 = Enable
ACMD12_EN	2	0b	Auto CMD12 Enable. Not valid when Block Count Enable bit is set to 0 0 = Disable 1 = Enable
UNUSED0 (R)	3	0b	This field is not used
DATA_DIR	4	0b	Data Transfer Direction. 0 = Write 1 = Read
MULTI_BLK	5	0b	Multiple/Single Block Select. 0 = Single Block 1 = Multiple Block
UNUSED1 (R)	15:6	00h	This field is not used
RESP_TYPE	17:16	00b	Response Type Select. 0 = No Response 1 = Response length is 136 bits 2 = Response length is 48 bits without busy 3 = Response length is 48 bits with busy
UNUSED2 (R)	18	0b	This field is not used
CRC_CHK_EN	19	0b	Command CRC Check Enable 0 = Disable 1 = Enable
CMD_IDX_CHK_EN	20	0b	Command Index Check Enable. 0 = Disable 1 = Enable
DATA_PRSNT	21	0b	Data Present Select. Indicates data is present and will be transferred on the DAT line. When command is issued with this bit enabled, internal buffer will be cleared. 0 = No data 1 = Data
CMD_TYPE	23:22	00b	Command Type. 0 = Normal 1 = Suspend CMD52 for writing BR in CCCR 2 = Resume CMD52 for writing Func Sel in CCCR 3 = Abort CMD12 (SD Memory) or Abort CMD52 (SDIO)
CMD_IDX	29:24	000000b	Command Index
UNUSED3 (R)	31:30	00b	This field is not used.

Transfer Mode and Command.

SDHC_RESP1_0 - RW - 32 bits - SD_HOST_STD:0x10			
Field Name	**Bits**	**Default**	**Description**
RESPONSE0 (R)	15:0	0000h	R23-8 of response is saved in this register.
RESPONSE1 (R)	31:16	0000h	R39-24 of response is saved in this register.

Response. The value is preseved until the next response.

SDHC_RESP3_2 - RW - 32 bits - SD_HOST_STD:0x14			
Field Name	**Bits**	**Default**	**Description**
RESPONSE2 (R)	15:0	0000h	R55-40 of response is saved in this register.
RESPONSE3 (R)	31:16	0000h	R71-56 of response is saved in this register.

Response. The value is preseved until the next response.

SDHC_RESP5_4 - RW - 32 bits - SD_HOST_STD:0x18			
Field Name	**Bits**	**Default**	**Description**
RESPONSE4 (R)	15:0	0000h	R87-72 of response is saved in this register.
RESPONSE5 (R)	31:16	0000h	R103-88 of response is saved in this register.

Response. The value is preseved until the next response.

SDHC_RESP7_6 - RW - 32 bits - SD_HOST_STD:0x1C			
Field Name	**Bits**	**Default**	**Description**
RESPONSE6 (R)	15:0	0000h	R119-104 of response or R23-8 of Auto CMD12 response is saved in this register.
RESPONSE7 (R)	31:16	0000h	R127-120 of response or R39-24 of Auto CMD12 response is saved in this register.

Response. The value is preseved until the next response.

SDHC_BUFFER - RW - 32 bits - SD_HOST_STD:0x20			
Field Name	**Bits**	**Default**	**Description**
BUFF_DATA0	15:0	0000h	Lower bits.
BUFF_DATA1	31:16	0000h	Upper bits. Data Buffer. Data will be accessed through this register. Data which exceeds the size designated by the Block Size register will not be written in the data buffer.

SDHC_PRSNT_STATE - RW - 32 bits - SD_HOST_STD:0x24			
Field Name	**Bits**	**Default**	**Description**
CMD_INHIB_CMD (R)	0	0b	Command Inhibit (CMD). Indicates that commands which use only the CMD line can be issued. 0 = Can issue commands which use CMD line 1 = Cannot issue any commands
CMD_INHIB_DAT (R)	1	0b	Command Inhibit (DAT). Indicates that commands which use also the DAT line can be issued. 0 = Can issue commands which use DAT line 1 = Cannot issue any commands which use DAT line
DAT_LINE_ACTIVE (R)	2	0b	DAT Line Active. Indicates DAT line on SD Bus is active. 0 = DAT line inactive 1 = DAT line active
UNUSED0 (R)	7:3	00000b	This field is not used

SDHC_PRSNT_STATE - RW - 32 bits - SD_HOST_STD:0x24			
Field Name	**Bits**	**Default**	**Description**
WR_TX_ACTIVE (R)	8	0b	Write Transfer Active. Indicates occurrence of write data transfer. 0 = No data transferring 1 = Write data transferring
RD_TX_ACTIVE (R)	9	0b	Read Transfer Active. Indicates occurrence of read data transfer. 0 = No data transferring 1 = Read data transferring
BUF_WR_EN (R)	10	0b	Buffer Write Enable. Indicates buffer is ready for writing. 0 = Write disable 1 = Write enable
BUF_RD_EN (R)	11	0b	Buffer Read Enable. Indicates buffer is ready for reading 0 = Read disable 1 = Read enable
UNUSED1 (R)	15:12	0h	This field is not used.
CARD_INS (R)	16	0b	Card Inserted. 0 = No card inserted or debouncing state or resetting 1 = Card inserted
CARD_STABLE (R)	17	0b	Card State Stable. Indicates Card Detect signal level is stable. 0 = Not stable (debouncing or resetting) 1 = Card stable
CD_LEVEL (R)	18	0b	Card Detect Pin Level. 0 = No card present 1 = Card present
WP_LEVEL (R)	19	0b	Write Protect Switch Level. 0 = Write protected 1 = Write enable
DAT_LEVEL (R)	23:20	00b	DAT Line Signal Level. Reflects signal level of DAT line.
CMD_LEVEL (R)	24	0b	CMD Line Signal Level. Reflects signal level of CMD line.
UNUSED2 (R)	31:25	00h	This field is not used

SDHC_CTRL1 - RW - 32 bits - SD_HOST_STD:0x28			
Field Name	**Bits**	**Default**	**Description**
LED_CTRL	0	0b	LED control. Drives the LED_ON output. 0 = Off 1 = on
DAT_TX_WIDTH	1	0b	Data Transfer Width. 0 = 1-bit 1 = 4-bit
HIGH_SPEED_EN	2	0b	High Speed Enable. When disabled, SD controller outputs commands and data on the falling edge of the SD clock. (Up to 25MHz SD clock can be supported.) When enabled, SD controller outputs commands and data on the rising edge of the SD clock. (Up to 50MHz SD clock can be supported.) 0 = Normal speed 1 = High speed

SDHC_CTRL1 - RW - 32 bits - SD_HOST_STD:0x28			
Field Name	**Bits**	**Default**	**Description**
DMA_SELECT	4:3	00b	DMA Select. Valid only when DMA is enabled. 0 = No DMA or SDMA selected 1 = 32-bit ADMA 2 = 32-bit ADMA2 3 = 64-bit ADMA2
MMC_WIDTH	5	0b	Extended Data Transfer Width (MMC). 0 = Use width set by DAT_TX_WIDTH 1 = 8-bit
CD_TEST_LEVEL	6	0b	Card Detect Test Level. 0 = Card removed 1 = Card inserted
CD_TEST_EN	7	0b	Card Detect Signal Selection. 0 = I/O pin 1 = SD_TEST_LEVEL
SD_BUS_EN	8	0b	SD Bus Power. When card is removed, this bit is cleared automatically. 0 = Off 1 = On
SD_BUS_VOLTAGE	11:9	000b	SD Bus Voltage 5 = 1.8V 6 = 3.0V 7 = 3.3V
UNUSED0 (R)	15:12	0h	This field is not used.
BG_STOP_REQ	16	0b	Stop at Block Gap Request. Writing 1 to this bit triggers halting of current data transfer after next block gap. To use this request, the Read Wait function is necessary in read transaction. Even if the Auto CMD12 Enable bit is set to 1, Auto CMD12 is not issued in case this bit is set to 1. This bit is cleared by not only writing 0 to this bit, but also issuing abort commands. 0 = Transfer 1 = Stop
CONT_REQ	17	0b	Continue Request. Writing 1 to this bit triggers restart of halted data transaction with current register setting. Once this bit is 1, the internal buffer will be cleared and data transfer sequence will be restarted. 1 = Restart
READ_WAIT_EN	18	0b	Read Wait Control. Indicates Read Wait will be inserted when needed. 0 = Disable 1 = Enable
BG_INT_EN	19	0b	Interrupt at Block Gap. Enable interrupt detection during 4-bit block transmission. 0 = Disable 1 = Enable
UNUSED1 (R)	23:20	00b	This field is not used.
SD_INT_WAKE_EN	24	0b	SD Card Interrupt Wakeup. 0 = Disable 1 = Enable
SD_INS_WAKE_EN	25	0b	SD Card Insertion Wakeup. 0 = Disable 1 = Enable
SD_REM_WAKE_EN	26	0b	SD Card Removal Wakeup. 0 = Disable 1 = Enable
UNUSED2 (R)	31:27	0h	This field is not used.

Host, Power, Block Gap and Wakeup Control

SDHC_CTRL2 - RW - 32 bits - SD_HOST_STD:0x2C			
Field Name	**Bits**	**Default**	**Description**
SYSCLK_EN	0	0b	Internal Clock Enable. 0 = Disable 1 = Enable
SYSCLK_STABLE (R)	1	0b	Internal Clock Stable. 0 = Unstable 1 = Stable
SDCLK_EN	2	0b	SD Clock Enable. SDCLK Frequency Select can be changed when this bit is 0. When card is removed, this bit is cleared to 0 automatically. 0 = Disable 1 = Enable
UNUSED0 (R)	7:3	00000b	This field is not used.
SDCLK_DIV	15:8	00h	SDCLK Frequency Select. If multiple bits are set, the most significant bit will be selected. 0 = Divide by 1 1 = Divide by 2 2 = Divide by 4 4 = Divide by 8 8 = Divide by 16 16 = Divide by 32 32 = Divide by 64 64 = Divide by 128 128 = Divide by 256
DATA_TO_CNT	19:16	0h	Data Timeout Counter Value. By using this counter value, DAT line timeouts are detected. 0xF : reserved 0xE : 2^27 ... 0x1 : 2^14 0x0 : 2^13
UNUSED1 (R)	23:20	0h	This field is not used.
SOFT_RST_ALL	24	0b	Software Reset for All. The following registers will not be cleared: - CMD Line Signal Level - DAT[3:0] Line Signal Level - Write Protect Switch Pin Level - Card Detect Pin Level - Card State Stable - Card Inserted - all bits in the Capabilities Register - all bits in the Maximum Current Capabilities Register
SOFT_RST_CMD	25	0b	Software Reset for CMD Line. The following registers will be cleared: - (Present State Register) - Command Inhibit (CMD) - (Normal Interrupt Status Register) - Command Complete

SDHC_CTRL2 - RW - 32 bits - SD_HOST_STD:0x2C			
Field Name	**Bits**	**Default**	**Description**
SOFT_RST_DAT	26	0b	Software Reset for DAT Line. The following registers will be cleared: - (Buffer Data Port Register) (Buffer is cleared) - (Present State Register) - Buffer Read Enable - Buffer Write Enable - Read Transfer Active - Write Transfer Active - DAT Line Active - Command Inhibit (DAT) - (Block Gap Control Register) - Continue Request - Stop At Block Gap Request - (Normal Interrupt Status Register) - Buffer Read Ready - Buffer Write Ready - Block Gap Event - Transfer Complete
UNUSED2 (R)	31:27	00h	This field is not used

Clock Control, Timeout Control and Soft Reset

SDHC_INT_STATUS - RW - 32 bits - SD_HOST_STD:0x30			
Field Name	**Bits**	**Default**	**Description**
CMD_DONE (R)	0	0b	Command Complete. The end bit of the command response is received. In the case of commands with no response, the end of the command.
DAT_DONE (R)	1	0b	Data Transfer Complete. Indicates the timing for completion of data transaction, which includes the completion at the block gap by the Stop At Block Gap Request. When some errors are detected during data transaction, this bit will not be set. In the case where Auto CMD12 is enabled, Auto CMD12 will be issued prior to this bit being set to 1.
BLOCK_GAP_EVT (R)	2	0b	Block Gap Event. It indicates the timing of next block gap, which was requested by the Stop At Block Gap Request. In case of write transaction, this interrupt will be generated before busy completion.
DMA_EVT (R)	3	0b	DMA Interrupt. It is set when internal counter reaches the value designated by Host DMA Buffer Boundary. It should be cleared by Host Driver after System Address Register is updated.
BUF_WR_RDY (R)	4	0b	Buffer Write Ready. Clearing this bit should be done before buffer writing, because SD controller has dual buffer and the next Buffer Write Ready interrupt may occur immediately.
BUF_RD_RDY (R)	5	0b	Buffer Read Ready. In the case where Auto CMD12 is enabled and last block has been transferred, Auto CMD12 will be issued prior to this bit being set to 1. Clearing this bit should be done before buffer reading, because SD controller has dual buffer and the next Buffer Read Ready interrupt may occur immediately.
CARD_INS (R)	6	0b	Card Insertion.
CARD_REM (R)	7	0b	Card Removal.

SDHC_INT_STATUS - RW - 32 bits - SD_HOST_STD:0x30			
Field Name	**Bits**	**Default**	**Description**
SDIO (R)	8	0b	SDIO Card Interrupt. Writing 1 to this register does not clear this bit. To clear this bit, interrupt factor of SDIO cards should be cleared. The value of this bit is latched internally as long as the Card Interrupt bit (D08) in the Normal Interrupt Status Enable register is 1.
UNUSED0 (R)	14:9	00h	This field is not used.
ERROR (R)	15	0b	Error Interrupt.
CMD_TO_ERR (R)	16	0b	Command Timeout Error. Response not returned within 128 SDCLK cycles.
CMD_CRC_ERR (R)	17	0b	Command CRC Error. If both CMD_TO_ERR and CMD_CRC_ERR are set, this indicates Command Conflict Error.
CMD_END_ERR (R)	18	0b	Command End Bit Error.
CMD_IDX_ERR (R)	19	0b	Command Index Error. Mismatch of Command Index and index of response.
DAT_TO_ERR (R)	20	0b	Data Timeout Error.
DAT_CRC_ERR (R)	21	0b	Data CRC Error.
DAT_END_ERR (R)	22	0b	Data CRC Error.
UNUSED1 (R)	23	0b	This field is not used.
ACMD12_ERR (R)	24	0b	Auto CMD12 Error. Logical OR of Auto CMD12 Error Status Register.
ADMA_ERR (R)	25	0b	ADMA Error.
UNUSED2 (R)	27:26	00b	This field is not used..
SDMA_ERR (R)	28	0b	SDMA Error.
CE_ATA_ERR (R)	29	0b	CE-ATA Error.
UNUSED3 (R)	31:30	00b	This field is not used.

Normal and Error Interrupt Status.
All bits are cleared by writing 1, except the Error Interrupt and the Card Interrupt. An interrupt (the XINT output) will be generated when the Interrupt Status Enable and the Interrupt Signal Enable are set and also one of these bits is set to 1.

SDHC_INT_MASK - RW - 32 bits - SD_HOST_STD:0x34			
Field Name	**Bits**	**Default**	**Description**
CMD_DONE_MASK	0	0b	Command Complete. 0 = Masked 1 = Enable
DAT_DONE_MASK	1	0b	Transfer Complete. 0 = Masked 1 = Enable
BLOCK_GAP_EVT_MASK	2	0b	Block Gap Event. 0 = Masked 1 = Enable
DMA_EVT_MASK	3	0b	DMA Interrupt. 0 = Masked 1 = Enable
BUF_WR_RDY_MASK	4	0b	Buffer Write Ready. 0 = Masked 1 = Enable
BUF_RD_RDY_MASK	5	0b	Buffer Read Ready. 0 = Masked 1 = Enable
CARD_INS_MASK	6	0b	Card Insertion. 0 = Masked 1 = Enable
CARD_REM_MASK	7	0b	Card Removal. 0 = Masked 1 = Enable

SDHC_INT_MASK - RW - 32 bits - SD_HOST_STD:0x34			
Field Name	**Bits**	**Default**	**Description**
SDIO_MASK	8	0b	Card Interrupt. 0 = Masked 1 = Enable
UNUSED0 (R)	15:9	00h	This field is not used.
CMD_TO_ERR_MASK	16	0b	Command Timeout Error. 0 = Masked 1 = Enable
CMD_CRC_ERR_MASK	17	0b	Command CRC Error. 0 = Masked 1 = Enable
CMD_END_ERR_MASK	18	0b	Command End Bit Error. 0 = Masked 1 = Enable
CMD_IDX_ERR_MASK	19	0b	Command Index Error. 0 = Masked 1 = Enable
DAT_TO_ERR_MASK	20	0b	Data Timeout Error. 0 = Masked 1 = Enable
DAT_CRC_ERR_MASK	21	0b	Data CRC Error. 0 = Masked 1 = Enable
DAT_END_ERR_MASK	22	0b	Data End Bit Error. 0 = Masked 1 = Enable
CUR_LIM_ERR_MASK	23	0b	Current Limit Error. 0 = Masked 1 = Enable
ACMD12_ERR_MASK	24	0b	Auto CMD12 Error 0 = Masked 1 = Enable
ADMA_ERR_MASK	25	0b	ADMA Error. 0 = Masked 1 = Enable
UNUSED1 (R)	27:26	00b	This field is not used.
SDMA_ERR_MASK	28	0b	SDMA Error 0 = Masked 1 = Enable
CE_ATA_ERR_MASK	29	0b	CE-ATA Error 0 = Masked 1 = Enable
UNUSED2 (R)	31:30	00b	This field is not used.

Normal and Error Interrupt Status Enable.
Enables interrupt status and interrupt outputs.

SDHC_SIG_MASK - RW - 32 bits - SD_HOST_STD:0x38			
Field Name	**Bits**	**Default**	**Description**
CMD_DONE_EN	0	0b	Command Complete. 0 = Masked 1 = Enable
DAT_DONE_EN	1	0b	Transfer Complete. 0 = Masked 1 = Enable
BLOCK_GAP_EVT_EN	2	0b	Block Gap Event. 0 = Masked 1 = Enable

SDHC_SIG_MASK - RW - 32 bits - SD_HOST_STD:0x38			
Field Name	**Bits**	**Default**	**Description**
DMA_EVT_EN	3	0b	DMA Interrupt. 0 = Masked 1 = Enable
BUF_WR_RDY_EN	4	0b	Buffer Write Ready. 0 = Masked 1 = Enable
BUF_RD_RDY_EN	5	0b	Buffer Read Ready. 0 = Masked 1 = Enable
CARD_INS_EN	6	0b	Card Insertion. 0 = Masked 1 = Enable
CARD_REM_EN	7	0b	Card Removal. 0 = Masked 1 = Enable
SDIO_EN	8	0b	Card Interrupt. 0 = Masked 1 = Enable
UNUSED0 (R)	15:9	00h	This field is not used.
CMD_TO_ERR_EN	16	0b	Command Timeout Error. 0 = Masked 1 = Enable
CMD_CRC_ERR_EN	17	0b	Command CRC Error. 0 = Masked 1 = Enable
CMD_END_ERR_EN	18	0b	Command End Bit Error. 0 = Masked 1 = Enable
CMD_IDX_ERR_EN	19	0b	Command Index Error. 0 = Masked 1 = Enable
DAT_TO_ERR_EN	20	0b	Data Timeout Error. 0 = Masked 1 = Enable
DAT_CRC_ERR_EN	21	0b	Data CRC Error. 0 = Masked 1 = Enable
DAT_END_ERR_EN	22	0b	Data End Bit Error. 0 = Masked 1 = Enable
CUR_LIM_ERR_EN	23	0b	Current Limit Error. 0 = Masked 1 = Enable
ACMD12_ERR_EN	24	0b	Auto CMD12 Error. 0 = Masked 1 = Enable
ADMA_ERR_EN	25	0b	ADMA Error. 0 = Masked 1 = Enable
UNUSED1 (R)	27:26	00b	This field is not used.
SDMA_ERR_EN	28	0b	SDMA Error. 0 = Masked 1 = Enable
CE_ATA_ERR_EN	29	0b	CE-ATA Error. 0 = Masked 1 = Enable
UNUSED2 (R)	31:30	00b	This field is not used

Normal and Error Signal Enable.
Enables interrupt signal outputs

SDHC_ACMD12_ERR - RW - 32 bits - SD_HOST_STD:0x3C			
Field Name	**Bits**	**Default**	**Description**
EXE_ERR (R)	0	0b	Auto CMD12 Not Executed Error.
TO_ERR (R)	1	0b	Auto CMD12 Timeout Error.
CRC_ERR (R)	2	0b	Auto CMD12 CRC Error.
END_ERR (R)	3	0b	Auto CMD12 End Bit Error.
INDEX_ERR (R)	4	0b	Auto CMD12 Index Error.
UNUSED0 (R)	6:5	00b	This field is not used.
CMD_ERR (R)	7	0b	Command Not Issued By Auto CMD12 Error.
UNUSED1 (R)	31:8	0000000h	This field is not used.

Auto CMD12 Error Status.
This register is valid when Auto CMD12 Error bit (D08) in the Error Interrupt Status Status Register is 1. Once next Auto CMD12 is issued, this register will be cleared.

SDHC_CAPABILITY - RW - 32 bits - SD_HOST_STD:0x40			
Field Name	**Bits**	**Default**	**Description**
TO_CLK_FREQ (R)	5:0	32h	Timeout Clock Frequency.
UNUSED0 (R)	6	0b	This field is not used.
TO_CLK_UNIT (R)	7	1b	Timeout Clock Unit.
BASE_CLK_FREQ (R)	13:8	32h	Base Clock Frequency for SD Clock.
UNUSED1 (R)	15:14	00b	This field is not used..
MAX_BLK_LEN (R)	17:16	10b	Max Block Length. 0 = 512 bytes 1 = 1K bytes 2 = 2K bytes 3 = Reserved
MMC8_SUPPORT (R)	18	0b	Extended Media Bus Support (MMC)
ADMA2_SUPPORT (R)	19	1b	ADMA2 Support.
ADMA_SUPPORT (R)	20	1b	ADMA Support.
HISPEED_SUPPORT (R)	21	1b	High Speed Support.
DMA_SUPPORT (R)	22	1b	DMA Support.
SUS_RES_SUPPORT (R)	23	1b	Suspend and Resume Support.
SUPPORT_3_3V (R)	24	1b	Voltage Support for 3.3V.
SUPPORT_3_0V (R)	25	0b	Voltage Support for 3.0V.
SUPPORT_1_8V (R)	26	0b	Voltage Support for 1.8V.
UNUSED2 (R)	31:27	0h	This field is not used.

Capabilities. The value of this register is loaded upon initialization.

SDHC_CURR_CAPABILITY - RW - 32 bits - SD_HOST_STD:0x48			
Field Name	**Bits**	**Default**	**Description**
MAX_CURR_3_3V (R)	7:0	64h	Max Current for 3.3V.
MAX_CURR_3_0V (R)	15:8	00h	Max Current for 3.0V.
MAX_CURR_1_8V (R)	23:16	00h	Max Current for 1.8V.
UNUSED0 (R)	31:24	00h	This field is not used.

Maximum Current Capabilities. The value of this register is loaded upon initialization

SDHC_FORCE_EVT - RW - 32 bits - SD_HOST_STD:0x50			
Field Name	**Bits**	**Default**	**Description**
ACMD12_EXE_ERR_FRC (W)	0	0b	Force Auto CMD12 Not Executed Error.
ACMD12_TO_ERR_FRC (W)	1	0b	Force Auto CMD12 Timeout Error.
ACMD12_CRC_ERR_FRC (W)	2	0b	Force Auto CMD12 CRC Error.
ACMD12_END_ERR_FRC (W)	3	0b	Force Auto CMD12 End Bit Error.
ACMD12_IDX_ERR_FRC (W)	4	0b	Force Auto CMD12 Index Error.

SDHC_FORCE_EVT - RW - 32 bits - SD_HOST_STD:0x50			
Field Name	**Bits**	**Default**	**Description**
UNUSED0 (R)	6:5	00b	This field is not used.
ACMD12_CMD_ERR_FRC (W)	7	0b	Force Command Not Issued By Auto CMD12 Error.
UNUSED1 (R)	15:8	00h	This field is not used.
CMD_TO_ERR_FRC (W)	16	0b	Force Command Timeout Error.
CMD_CRC_ERR_FRC (W)	17	0b	Force Command CRC Error.
CMD_END_ERR_FRC (W)	18	0b	Force Command End Bit Error.
CMD_IDX_ERR_FRC (W)	19	0b	Force Command Index Error.
DAT_TO_ERR_FRC (W)	20	0b	Force Data Timeout Error.
DAT_CRC_ERR_FRC (W)	21	0b	Force Data CRC Error.
DAT_END_ERR_FRC (W)	22	0b	Force Data End Bit Error.
CUR_LIM_ERR_FRC (W)	23	0b	Force Current Limit Error.
ACMD12_ERR_FRC (W)	24	0b	Force Auto CMD12 Error.
ADMA_ERR_FRC (W)	25	0b	Force ADMA Error.
UNUSED2 (R)	27:26	00b	This field is not used.
SDMA_ERR_FRC (W)	28	0b	Force SDMA Error.
CE_ATA_ERR_FRC (W)	29	0b	Force CE-ATA Error.
UNUSED3 (R)	31:30	00b	This field is not used.

Force Event for Auto CMD12 Error and Error Interrupt Status.

Auto CMD12 Error Status can be set by setting the corresponding bit in this register while bit[8] (Auto CMD12 Error Status Enable) in the Error Interrupt Status Enable register is set. If bit[8] in the Error Interrupt Signal Enable register is set, the XINT signal will be asserted. The Error Interrupt Status can be set by setting the corresponding bit in this register while the Error Interrupt Status Enable register is set. If the Error Interrupt Signal Enable register is set, XINT signal will be asserted.

SDHC_ADMA_ERR - RW - 32 bits - SD_HOST_STD:0x54			
Field Name	**Bits**	**Default**	**Description**
ADMA_STATE (R)	1:0	00b	ADMA State when error has occurred. 00 - Stop DMA 01 - Fetch Descriptor 10 - Change Address 11 - Transfer Data
ADDR_LEN_MISMATCH (R)	2	0b	ADMA Address Length Mismatch Error. This error occurs in the following 2 cases: 1. While Block Count Enable being set, the total data length specified by the descriptor table is different from that specified by the Block Count and Block Length. 2. Total data length cannot be divided by the block length.
UNUSED0 (R)	31:3	0h	This field is not used.

ADMA Error Status.

SDHC_ADMA_SAD - RW - 32 bits - SD_HOST_STD:0x58			
Field Name	**Bits**	**Default**	**Description**
ADMA_SYS_ADDR0	15:0	0000h	Lower bits.
ADMA_SYS_ADDR1	31:16	0000h	Upper bits. ADMA System Address. Before ADMA data transfer, the descriptor address should be set by the Host Driver. This address needs to be set with 4-byte alignment, since the descriptor table has 32-bit (4 byte) information formatted.

SDHC_VER_SLOT - RW – 32 bits - SD_HOST_STD:0xFC			
Field Name	**Bits**	**Default**	**Description**
SLOT_INTRPT (R)	7:0	00h	Interrupt Signal for Each Slot. The value of XSLT_INT7-0 inputs, which indicates the logical OR of Interrupt signal and Wakeup signal, are inverted and referred to by this register. In case of multiple slots, Interrupt signal and Wakeup signal should be logical ORed externally and should be inputted to each of XSLT_INT7-0.
UNUSED0 (R)	15:8	00h	This field is not used.
SPEC_VERSION (R)	23:16	00h	Specification Version.
VENDOR_VERSION (R)	31:24	00h	Vendor Version

Slot Interrupt Status and Host Controller Version

Chapter 3
System Resources

To go to a section of interest, click on the following links:

3.1 SMBus Module

Even though SMBus is exposed to software as a PCI device, its SMBus control register address space is actually defined as dual address space; one is IO address and the other is memory address space. The IO address is defined by PMIO_ 2C, while the memory address space is part of system resource MMIO space defined by PMIO_24 (as shown below). Default value of MMIO is set to FED1_0000, which means SMBus control registers are accessed through memory address 0xFED1_0A00:FED1_0AFF. SMBus PCI configuration registers have dual address space at both PCI configuration address as well as mirrored onto MMIO offset 000:0FF.

AcpiMmioEn - RW – 8/16/32 bits - [PM_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
AcpiMMioDecodeEn	0	0b	Set to1 to enable AcpiMMio space.
AcpiMMIoSel	1	0b	Set AcpiMMio registers to be in memory-mapped or IO-mapped space. 0: Memory-mapped space 1: I/O-mapped space
AcpiMMioAddr	31:13	FED8_00h	System Resource MMIO Base register offset 000:0FF SM PCI configuration registers 100:1FF GPIO 200: 2FF SMI 300: 3FF PMIO 400: 4FF PMIO2 500: 5FF BIOS_RAM 600: 6FF CMOS_RAM 700: 7FF CMOS 800: 8FF ACPI 900: 9FF ASF registers A00: AFF SMBus registers B00: BFF WatchDog registers C00: CFF HPET (new) D00: DFF IoMux (new) E00: EFF Misc (new) 1000:10FF Serila Debug bus 1400:14FF DP-VGA registers (new) 1800:18FF Reserved 1C00:1CFF USB3 Phy (new)

Most of the system resource registers have dual address decoding. They would have their own native address space as well as mirrored addresses in the system resource MMIO space. For example, PMIO registers have dual address decoding: one interface at IO 0xCD6/0xCD7, which are the index/data ports, and the other is mirrored at MMIO + 0x300:3FF. MMIO address is enabled and defined at PMIO offset 0x24.

3.1.1 PCI Configuration Registers

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
STATUS	06h
Revision ID/Class Code	08h
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh

Register Name	Offset Address
BIST	0Fh
Base Address 0	10h
Base Address 1	14h
Base Address 2	18h
Base Address 3	1Ch
Base Address 4	20h
Base Address 5	24h
Cardbus CIS Pointer	28h
Subsystem Vendor	2Ch
Subsystem ID	2Eh
Expansion ROM Base Address	30h
Capability Pointer	34h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min_Gnt	3Eh
Max_Lat	3Fh

VendorID - R - 16 bits - [PCI_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
VendorID	15:0	1022h	Vendor Identifier. The vendor ID is 0x1022.

DeviceID - R - 16 bits - [PCI_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
DeviceID	15:0	780Bh	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.

Command- RW - 16 bits - [PCI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
I/O Space	0	1b	This bit controls a device's response to I/O space accesses. A value of 1 enables it and a value of 0 disables it. Since this module does claim certain legacy IO cycles, this bit's default value is 1.
Memory Space	1	1b	This bit controls a device's response to memory space accesses. A value of 1 enables it and a value of 0 disables it.
Bus Master	2	0b	A value of 0 disables the device from generating PCI accesses. A value of 1 allows it to behave as a bus master. ACPI/SMBus does not have PCI master and so the bit is always 0. [Read-only]
Special Cycle	3	0b	A value of 0 causes the devices to ignore all special cycle operations. A value of 1 allows the device to monitor Special Cycle operations. This module does not respond to special cycle and so the bit is hardcoded to 0
Memory Write & Invalidate Enable	4	0b	This bit is an enable bit for using the Memory Write and Invalidate command. This module will not generate this command and so the bit is always 0. [Read-only]
VGA Palette Snoop	5	0b	This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. This does not apply to this module and so the bit is always 0. [Read-only]

Command- RW - 16 bits - [PCI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Parity Error Response	6	0b	This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device must ignore any parity errors that it detects and continue normal operation.
Wait Cycle Control	7	0b	This bit is used to control whether or not a device does address/data stepping. This module does not use address stepping and so the value is always 0. [Read-only]
SERR# Enable	8	0b	This bit is an enable bit for SERR# driver. A value of 0 disables the SERR# and a value of 1 enables it.
Fast Back-to-Back Enable	9	0b	This bit indicates whether device is fast back-to-back capable. ACPI/SMbus does not support this function and so this bit is always 0. [Read-only]
Reserved	15:10	00h	Reserved

STATUS- RW - 16 bits - [PCI_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0000b	Reserved
MSI Mapping Capability	4	0b	[Read-only] This bit indicates whether the device can support MSI mapping.
66 MHz Capable	5	1b	This bit indicates whether the device can support 66 MHz. This device is 66 MHz capable. [Read-only]
UDF Supported	6	0b	This bit indicates whether the device supports user-definable feature. This module does not support this feature and so the bit is always 0. [Read-only]
Fast Back-to-Back Capable	7	0b	This bit indicates whether the device is capable of fast back-to-back cycles. This module does not support this feature and so the bit is always 0. [Read-only]
Data Parity Error Detected	8	0b	Set to 1 if the Parity Error Response bit is set and the module has detected PERR# asserted while acting as a PCI master (regardless of whether PERR# was driven by this module).
DEVSEL Timing	10:9	01b	These bits encode the timing of DEVSEL#. This module will always respond in medium timing and so these bits are always 11.
Signaled Target Abort	11	0b	This bit is set by a slave device whenever it terminates a cycle with a Target-Abort.
Received Target Abort	12	0b	This bit is set by a master device whenever its transaction is terminated with a Target-Abort.
Received Master Abort	13	0b	This bit is set by a slave device whenever it terminates its transaction with Master-Abort.
Signaled System Error	14	0b	This bit is set by the device whenever the device asserts SERR#.
Detected Parity Error	15	0b	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled.

Revision ID/Class Code- R - 32 bits - [PCI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
RevisionID	7:0	15h	Revision ID
Class Code	31:8	0C0500h	0C0500h denotes a SMBUS controller.

Cache Line Size- R - 8 bits - [PCI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This register specifies the system cacheline size. This module does not use Memory Write and Invalidate command and so this register is not applicable. It is hardcoded to 0.

Latency Timer- R - 8 bits - [PCI_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Latency Timer	7:0	00h	This register specifies the value of the Latency Timer. This is not used in this module and so it is always 0.

Header Type- R - 8 bits - [PCI_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	80h	This device is a multifunction device.

BIST- R - 8 bits - [PCI_Reg: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
BIST	7:0	00h	The module has no built-in self-test and so this is always 0.

Base Address 0- R - 32 bits - [PCI_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 0	31:0	00000000h	Not used and is hardcoded to 0.

Base Address 1- R - 32 bits - [PCI_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 1	31:0	000h	Not used and is hardcoded to 0.

Base Address 2- R - 32 bits - [PCI_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 2	31:0	0000_0000h	Not used and is hardcoded to 0.

Base Address 3- R - 32 bits - [PCI_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
Base Address 3	31:0	0000_0000h	Not used and is hardcoded to 0.

Base Address 4- R - 32 bits - [PCI_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 4	31:0	0000_0000h	Not used and is hardcoded to 0.

Base Address 5- R - 32 bits - [PCI_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 5	31:0	0000_0000h	Not used and is hardcoded to 0.

Cardbus CIS Pointer- R - 32 bits - [PCI_Reg: 28h]			
Field Name	**Bits**	**Default**	**Description**
Cardbus CIS Pointer	31:0	0000_0000h	Not used and is hardcoded to 0.

Subsystem Vendor ID- W - 16 bits - [PCI_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	1022h	Write once.

Subsystem ID- W - 16 bits - [PCI_Reg: 2Eh]			
Field Name	**Bits**	**Default**	**Description**
Subsystem ID	15:0	780Bh	Write once.

Expansion ROM Base Address - R - 8 bits - [PCI_Reg: 30h]			
Field Name	**Bits**	**Default**	**Description**
Expansion ROM Base Address	7:0	00h	Not used and is hardcoded to 0.

Capability Pointer - R - 8 bits - [PCI_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
Capability Pointer	7:0	00	Default value is 00h

Interrupt Line - R - 8 bits - [PCI_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	This module does not generate interrupt. This register is hardcoded to 0.

Interrupt Pin – R - 8 bits - [PCI_Reg: 3Dh]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin	7:0	00h	This register specifies which interrupt pin the device issues. This module does not generate interrupt but contains the actual interrupt controller. This register is hardcoded to 0.

Min_Gnt - R - 8 bits - [PCI_Reg: 3Eh]			
Field Name	**Bits**	**Default**	**Description**
Min_Gnt	7:0	00h	This register specifies the desired settings for Latency Timer values. Value of 0 indicates that the device has no major requirements for the setting. This register is hardcoded to 0.

Max_Lat - R - 8 bits - [PCI_Reg: 3Fh]			
Field Name	**Bits**	**Default**	**Description**
Max_Lat	7:0	00h	This register specifies the desired settings for Latency Timer values. Value of 0 indicates that the device has no major requirements for the setting. This register is hardcoded to 0.

3.2 ACPI Registers

These are the standard registers defined by the ACPI specification. ACPI register address locations are defined by PMIO 60:6F. These registers can also be accessed through MMIO + 0x800:8FF. In order for FCH to decode these ACPI addresses, PMIO_74[0] must be set to 1.

Register Name	Offset Address*
Pm1Status	00h
Pm1Enable	02h
PmControl	00h
Pm2Control	00h
TmrValue/ETmrValue	00h
CLKVALUE	00h
PLvl2	04h
PLvl3	05h
EVENT_STATUS	00h
EVENT_ENABLE	04h
*** Note**: The offset addresses listed here for the ACPI registers belong to different apertures/decodes. Check the register descriptions for details.	

Pm1Status - RW - 16 bits - [AcpiPmEvtBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
TmrStatus	0	0b	Timer carry status bit. This bit gets set anytime the 31st bit of 32 bit counter changes (whenever the MSB changes from low to high or high to low. While TmrEn and TmrStatus are set, an interrupt event is raised). [Read-only]
Reserved	3:1		
BmStatus	4	0b	Bus master status bit. This bit is set any time a system bus master requests the system bus, and can only be cleared by writing an one to this bit position.
GblStatus	5	0b	This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. This is set by writing 1 to PM_Reg: 74h bit [7].
Reserved	7:6		
PwrBtnStatus	8	0b	Power button status bit
Reserved	9		
RtcStatus	10	0b	This bit is set when RTC generates an alarm.
Reserved	13:11		
PciExpWakeStatus	14	0b	This bit is set by hardware to indicate that the system wake is due to a PCI Express wakeup event.
WakeStatus	15	0b	This bit is set when the system is in the sleep state and a wake-up event occurs.
This register is located at the base address defined by AcpiPm1EvtBlk.			

Pm1Enable - RW - 16 bits - [AcpiPmEvtBlk:02h]			
Field Name	**Bits**	**Default**	**Description**
TmrEn	0	0b	This is the timer carry interrupt enable bit. When this bit is set then an SCI event is generated anytime the TmrStatus is set. When this bit is reset then no interrupt is generated when the TmrStatus bit is set.
Reserved	4:1		
GblEn	5	0b	If this bit is set, SCI is raised whenever both GblEn and GblStatus are true.
Reserved	7:6		
PwrBtnEn	8	0b	If this bit is set, SCI is generated whenever PwrBtnStatus is true.

Pm1Enable - RW - 16 bits - [AcpiPmEvtBlk:02h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	9		
RtcEn	10	0b	RTC enable. If this bit is set, SCI is generated whenever RtcStatus is true.
Reserved	13:11		
PciExpWakeDis	14	1b	This bit disables the inputs to the PciExpWakeStatus from waking the system.
Reserved	15		
This register is located at the base address defined by AcpiPm1EvtBlk.			

PmControl - RW - 16 bits - [AcpiPm1CntBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
SCI_EN	0	0b	Selects the power management event to be either an SCI or SMI# interrupt for the following events. When this bit is set, then PM events will generate an SCI interrupt; otherwise, it will be SMI#.
BmRld	1	0b	If this bit is set, any bus master activity will cause the C state logic to break out from C3. This is no longer needed for current C state implementation
GBL_RLS	2	0b	If SMI_Reg:B0h[17:16] is set to 01b, writing 1 to this bit will generate SMI# and set SMI_Reg:88h bit[8]. Reading, this bit will always return 0.
Reserved	9:3		
SLP_TYP	12:10	000b	Defines the sleep state the system enters when the SLP_TYPEn is set to one. This design currently implements 5 states: S0, S1, S3, S4, and S5.
SLP_En	13	0b	This is a write-only bit and reads from it always return zero. If PM_Reg:04h bit7 (SLP_SMI_EN) is 0, setting this bit will cause the system to sequence into the sleeping state associated with the SLP_TYP fields programmed. If SLP_SMI_EN is 1, setting this bit will cause SMI#. Writing 0 to this bit has no effect.
Reserved	15:14		
This register is located at the base address defined by AcpiPm1CntBlk (PM_Reg:62h).			

Pm2Control - RW - 8 bits - [AcpiPm2CntBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
ARB_DIS	0	0b	System arbiter is disabled when this bit is set. **Note:** under this current AMD C state implementation, this is no longer used and should not be reported to OS.
Reserved	7:1		
AcpiPm2CntBlk is defined in PM_Reg:6Eh			

TmrValue/ETmrValue – R - 32 bits - [AcpiPmTmrBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
TmrValue	31:0	-	This read-only field returns the running count of the power management timer (ACPI timer)
AcpiPmTmrBlk is defined in PM_Reg:64h			

CLKVALUE - RW - 32 bits - [CpuControl:00h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0		
ClkValue	3:1	000b	These bits define throttle interval for STPCLK# (Software throttling) 000b: 50% 001b: 12.5% 010b: 25% 011b: 37.5% 100b: 50% 101b: 62.5% 110b: 75% 111b: 87.5%
ThtEn	4	0b	This bit enables clock throttling as set in the ClkValue (bit 3:1).
Reserved	31:5		
CpuControl Io base is defined in PM_Reg 0x66			

PLvl2 - R - 8 bits - [CpuControl:04h]			
Field Name	**Bits**	**Default**	**Description**
PLvl2	7:0	00h	Reads to this register return all zeros and generate a “enter C2” sequence to APU; writes to this register have no effect.
CpuControl Io base is defined in PM_Reg 0x66			

PLvl3 – R – 8 bits - [CpuControl:05h]			
Field Name	**Bits**	**Default**	**Description**
PLvl3	7:0	00h	Reads to this register return all zeros and generate a “enter C3” sequence to APU; writes to this register have no effect.
CpuControl Io base is defined in PM_Reg 0x66			

EVENT_STATUS - RW - 32 bits - [AcpiGpe0Blk:00h]			
Field Name	**Bits**	**Default**	**Description**
EventStatus	31:0		Each bit represents an ACPI event status. Writing 1 to any bit clears it. Each event status is set when the selected event input equals to the corresponding value in SciTrig. **Note:** configuration for EVENTs are located at SMI_Reg: 08h through 70h. The status bits are also mirrored in SMI_Reg: 00h

EVENT_ENABLE - RW - 32 bits - [AcpiGpe0Blk:04h]			
Field Name	**Bits**	**Default**	Description
EventEnable	31:0	32’h0	Each bit controls whether ACP should generate wakeup and SCi interrupt. The enable bits are also mirrored in SMI_Reg: 04h

SmiCmdPort - RW – 8 bits – [SmiCmdBlk: 00h]			
Field Name	**Bits**	**Default**	**Description**
SmiCmdPort	7:0	00h	Writing the Port can generate Smi.
This register is located at the base address defined by AcpiSmiCmd [PM_Reg:6Ah] + offset 0. When SMI command port is enabled, write to this port will generate SMI#. A read of this address will return the previously written value but will not generate SMI. The SMI command port has to be located at an even address (ie, 0, 2, 4, 6, 8, A, C, or E). SmiCmdStatus is always located one byte immediately after the SmiCmdPort. The implementation actually contains four (4) bytes of address space. If SMI command port is assigned to byte 0, then byte 1 is SmiCmdStatus. Byte 2 and 3 can be used as scratch. If SmiCmdPort is assigned to byte 2, then bytes 0 and 1 are not available.			

SmiCmdStatus - RW - 8 bits – [SmiCmdBlk: 01h]			
Field Name	**Bits**	**Default**	**Description**
SmiCmdStatus	7:0	00h	Used by BIOS and OS
This register is located at the base address defined by AcpiSmiCmd [PM_Reg:6Ah] + offset 1.			

3.3 Power Management (PM) Registers

Bolton supports two ways of accessing the PM registers: by legacy indirect IO access or by direct memory-mapped (or IO-mapped) IO access.

The indirect IO access is through CD6 (index) and CD7 (data) in the IO space. Software first programs the offset into the index register (IO space – 0xCD6) and then reads/writes to the data register (IO space – 0xCD7).

The second way of accessing the PM registers is through the new direct mapping scheme. The direct mapping is disabled at initial power up. Software needs to first program the “AcpiMmioEn” register in PM_reg offset 0x24 by using the indirect IO (CD6/CD7) programming sequence to enable the direct mapping (AcpiMMioDecodeEn) and memory-mapped (or IO-mapped) base address.

Register Name	Offset Address
IsaDecode	00h
IsaControl	04h
PciControl	08h
StpClkSMAF	0Ch
SysErr	18h
SysCmd	1Ch
BiosRamEn	20h
AcpiMMioEn	24h
AsfEn	28h
SmBus0En	2Ch
SmBus0Sel	2Eh
Reserved	2Fh-33h
IoApicEn	34h
IoApicClk	38h
SmartVoltEn	3Ch
SmartVolt2En	40h
BootTimerEn	44h
WatchDogTimerEn	48h
WatchDogTimerConfig	4Ch
HPETEn	50h
SerialIrqConfig	54h
RtcControl	56h
VRT_T1	58h
VRT_T2	59h
IntruderControl	5Ah
RtcShawdow	5Bh
LLB Cntrl	5Ch
Reserved	5Dh
RtcExtIndex	5Eh
RtcExtData	5Fh
AcpiPm1EvtBlk	60h
AcpiPm1CntBlk	62h
AcpiPmTmrBlk	64h
P_CNTBlk	66h
AcpiGpe0Blk	68h
AcpiSmiCmdBlk	6Ah
AcpiPm2CntBlk	6Eh
AcpiConfig	74h
WakeIoAddr	78h
C1eWrPortAdr	7Ch
CStateEn	7Eh
BreakEvent	80h
Reserved	84h
CStateControl	88h
PopUpEndTime	8Eh
CStateTiming0	94h
CStateTiming1	98h
C2Counter	9Ch

Register Name	Offset Address
C3Counter	9Dh
Reserved	9Eh
MessageCState	A0h
TrafficMonitorEn / TrafficStatus	A4h
TrafficMonitorIdleTime	A8h
TrafficMonitorIntrTime	AAh
TrafficMonitorTrafficCount	ACh
TrafficMonitorIntrCount	AEh
TrafficMonitorTimeTick	B0h
Reserved	B2h
FidVidControl	B4h
Reserved	B6h
tpreset1b	B7h
Tpreset2	B8h
Reserved	B9h
S_StateControl	BAh
ThrottlingControl	BCh
ResetControl	BEh
S5/Reset Status	C0h
ResetCommand	C4h
Cf9Shadow	C5h
HTControl	C6h
Misc0	C8h
IoDrvSth	CCh
RstCntrl	D0h
RstLength / APURstLength / APUPwrGdLength	D1h
PmioDebug	D2h
ManualReset	D3h
IMCGating	D6h
Eprom/EfuseIndex	D8h
Eprom/EfuseData	D9h
SataConfig	DAh
DacCntrl	DCh
Reserved	DEh
BlinkControl	DFh
ABRegBAR	E0h
Reserved	E6h
SDFlashCntrl	E7h
PcibConfig	EAh
AzEn	EBh
LpcGating	ECh
UsbGating	EDh
Usb3Cntrl	EEh
UsbEn	EFh
UsbControl	F0h
UsbDebug	F3h
GecEn	F6h
GecConfig	F8h
TraceMemoryEn	FCh

IsaDecode - RW – 8/16/32 bits - [PM_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Obsolete	0	0b	This is an obsolete function; BIOS should leave it as 0.
Intr_enable	1	1b	Set to 1 to enable PIC interrupt function
tmr_enable	2	1b	Set to 1 to enable 8254 timer function.
pm_enable	3	1b	Set to 1 enable Io CD6/CD7 decoding in internal Isa bus. The bit has to be set all the time
Reserved	5:4	-	
IndexPortEn	6	0b	If set, FCH will decode IO CE0:CE4. These two ports are for debugging purpose only
IsaPmDebugEn	7	0b	Debug function only.

IsaDecode - RW – 8/16/32 bits - [PM_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:8	-	
DmaAddr_En	16	1b	Enable the decoding of I/O Port 0x000:0x01F, 0x080:0x08F, 0x0C0:0xCF, 0x0D0:0x0DF, 0x40B, 0x4D6.
PitAddr_En	17	1b	Enable the decoding of I/O Port 0x40, 0x41, 0x42, 0x43.
NmiAddr_En	18	1b	Enable the decoding of I/O Port 0x61.
RtcAddr_En	19	1b	Enable the decoding of I/O Port 0x70 and 0x71.
Reserved	24:20	-	
PM_Addr_Enable	25	1b	Enable the decoding of I/O Port 0xCD6, xCD7.
Reserved	27:26	0b	Reserved
Reserved	29:28	00b	Spare bits.
Port92Enable	30	1b	Enable the decoding of I/O Port 92.

IsaControl - RW – 8/16/32 bits - [PM_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Dma_limit	6:0	00h	Specify the legacy DMA transfer size.
Dma_limit_en	7	0b	Set to 1 to enable the Dma_limit on the legacy DMA transfer on the LPC bus.
Reserved	9:8	-	.
Debug	10	1b	Debug purpose, always leave it as 1
Bm_req_en	11	0b	Legacy BM_REQ# function enable bit; it is now for debug purpose only.
Reserved	13:12	-	
Reserved	24	-	
PCIB_SReset_En Mask	25	0b	When set, PCIBridge reset control bit PCIB_SReset_En (x3e bit 22 of PCI Bridge) will be writable
Reserved	27:26	-	

PciControl - RW – 8/16/32 bits - [PM_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	-	
DmaVerifyEn	2	0b	Set to1 to enable mimicking of legacy DMA VERIFY function. This is only needed for old LPC driver (such as floppy) that requires VERIFY function
Mask_msg_bmsts_en	3	0b	Set to 1 to enable A20#, IGNNE#, INIT#, NMI, SMI# message delivery.
Msg_intr_enable	4	0b	Set to 1 to deliver legacy PIC interrupt as message type.
Mts_set	5	1b	1: Encode PIC interrupt request as Legacy PIC ExtInt message type and NMI request as legacy NMI message type. 0: encode PIC interrupt request as ExtInt message type and NMI request as NMI message type.
Mts_auto	6	0b	Set to 1 to encode PIC Intr request as Legacy PIC ExtInt message type and PIC Nmi request as legacy PIC NMI message type if IOAPIC is enabled and Mts_set is zero.
Force_smaf_match	7	0b	Set to 1 to enable STPGNT message matching to the expected SMAF.
Pic_apic_arbiter	8	1b	Set to 1 to arbitrate between PIC request and IOAPIC request
Debug	10	1b	Debug use only, SW should leave this bit as 1
Reserved	11	-	
Ext_intr_time	14:12	000b	Specify the extended interrupt time in 2 microsecond intervals. This is used for preventing APU from re-entering C state right away when it just breaks out from a C state
Reserved	18:15	-	
Ab_stall_en	23	0b	Set to 1 to allow the legacy DMA engine to hold the internal bus before completing legacy DMA on the LPC bus. This is only needed for certain old LPC devices.

PciControl - RW – 8/16/32 bits - [PM_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Force_stpclk_retry	24	1b	Set to 1 to send out STPCLK message before the completion response of the following 3 types of request: 1. I/O write to Slp_typ register 2. I/O write Ldt_stp command 3. C1e cycle Normally it is required to send out STPCLK before completion of the cycles listed above, except for the case of SMI trapping. In that case, this bit should be left as 0
Force_slpstate_retry	25	0b	Set to 1 to send out SMI message before the completion response of IO write to SLP_TYP register. This is to be used in conjunction with SMI trapping on write to SLP_TYP register
Note: SLP_TYP is located in AcpiPm1CntBlk offset 00h, bits 10~12.			

StpClkSmaf - RW – 8/16/32 bits - [PM_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
S4S5SMAF	2:0	110b	System management action field for S4/5 STPCLK message
C2SMAF	6:4	0h	System management action field for C2 STPCLK message
C3SMAF	10:8	001b	System management action field for C3 STPCLK message
VFSMAF	14:12	010b	System management action field for VFID STPCLK message
S1SMAF	18:16	011b	System management action field for S1 STPCLK message
S3SMAF	22:20	100b	System management action field for S3 STPCLK message
NSSMAF	26:24	101b	System management action field for Normal Throttling STPCLK message
TTSMAF	30:28	101b	System management action field for Thermal Throttling STPCLK message

BiosRamEn - RW – 8/16/32 bits - [PM_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
Bios_ram_mem_enable	0	0b	Set to 1 to enable BIOS RAM access.
Bios_ram_mem_Addr	31:8	FED1_00h	Specify the BIOS RAM base address[31:8].

AcpiMmioEn - RW – 8/16/32 bits - [PM_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
AcpiMMioDecodeEn	0	0b	Set to1 to enable AcpiMMio space.
AcpiMMIoSel	1	0b	Set AcpiMMio registers to be in memory-mapped or IO-mapped space. 0: Memory-mapped space 1: I/O-mapped space

AcpiMmioEn - RW – 8/16/32 bits - [PM_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
AcpiMMioAddr	31:13	FED8_00h	SBResourceMMIO_Base register Offset 000:0FF SM PCI configuration registers 100:1FF GPIO 200: 2FF SMI 300: 3FF PMIO 400: 4FF PMIO2 500: 5FF BIOS_RAM 600: 6FF CMOS_RAM 700: 7FF CMOS 800: 8FF ACPI 900: 9FF ASF registers A00: AFF SMBus registers B00: BFF WatchDog registers C00: CFF HPET (new) D00: DFF IoMux (new) E00: EFF Misc (new) 1000:10FF Serila Debug bus 1400:14FF DP-VGA registers (new) 1800:18FF Reserved 1C00:1CFF USB3 Phy (new)

AsfEn - RW – 8/16/32 bits - [PM_Reg: 28h]			
Field Name	**Bits**	**Default**	**Description**
AsfEn	0	1b	Set to 1 to enable ASF function and I/O decoding.
AsfClkStretchEn	1	0b	Set to 1 to enable clock stretching support.
AsfSmMasterEn	2	0b	Set to 1 to enable ASF SMBUS master function.
AsfIoBase	15:5	059h	Specify the AsfIoBase[15:5]. By default AsfIoBase is B20h.
AsfClkSel	22:16	00000h	The value controls the frequency of ASF master clock; its definition is: 0: ~100KHz 1: ~200KHz 2: ~300kHz 3:~ 400kHz 4:~ 600kHz 5:~ 800kHz 6:~ 900kHz 7:~1MHz Others: 66.67M/((AsfClkSel + 1) * 2)
AsfClkSwitchEn	23	1b	Set to 1 to change ASF master clock from RTC(32k) to the clock defined in AsfClkSel of the same register.

Smbus0En - RW – 16 bits - [PM_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
SmBus0En	0	0b	Set to 1 to enable SMBUS0 function and decoding.
Reserved	2:1	00b	
SmBus0_baddr	15:5	058h	Specify the Smbus0IoBase[15:5]. By default Smbus0IoBase is B00h.

Smbus0Sel - RW – 8 bits - [PM_Reg: 2Eh]			
Field Name	**Bits**	**Default**	**Description**
SmBus0Sel	2:1	00b	SmBus port selection. 00: Port 0 01: Port 2 10: Port 3 11: Port 4

IoApicEn - RW – 8/16/32 bits - [PM_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
Ioapic_enable	0	0b	Set to 1 to enable IoApic decoding.
Ioapic_mode	1	1b	XIOAPIC enable; this bit is only valid if bit 0 is set.
Ioapic_m_io_	2	1b	0: I/O space 1: Memory space
Ioapic_id_ext_en	4	1b	Set to1 to extend APIC ID from 4 bits to 8 bits.
IoapicBaseAddr	31:5	07F6000h	Specify the IoApic base address[31:5]. By default IoApic base[31:0] is FEC0_0000h.

SmartVoltEn - RW – 8/16/32 bits - [PM_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
SmartVoltIdleTime	6:0	0h	Amount of “idle” time (in 2us increment) the SmartPower function should wait before it assert SmartVolt.
SmartVoltEnable	7	0b	Enable bit for the SmartPower function. When set, the logic will monitor the logic defined by the “Check*” bits (bit8 ~ bit23). If all of the corresponding modules are idle, an internal SmartVoltEvent will be generated and the corresponding modules can use the SmartVoltEvent to do board level voltage control.
CheckVIN0	8	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN0 has reached or passed the threshold.
CheckVIN1	9	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN1 has reached or passed the threshold.
CheckVIN2	10	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN2 has reached or passed the threshold.
CheckVIN3	11	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN3 has reached or passed the threshold.
CheckVIN4	12	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN4 has reached or passed the threshold.
CheckVIN5	13	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN5 has reached or passed the threshold.
CheckVIN6	14	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN6 has reached or passed the threshold.
CheckVIN7	15	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN7 has reached or passed the threshold.

SmartVoltEn - RW – 8/16/32 bits - [PM_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
CheckC3	16	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if APU is in C3 state.
Reserved	17	0b	Reserved
CheckSata	18	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if SATA is idle
CheckUsb	19	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if USB is idle.
CheckPciBridge	20	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if HD audio PCIBridge is idle.
Reserved	21	0b	Reserved
CheckAz	22	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if HD audio is idle.
CheckLpc	23	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if LPC is idle.
SmartVolt function is meant to provide a mechanism to control the external power supply in order to reduce additional system power consumption. For example, software can set Smart Power Control1 bit [6] and [7]. Whenever APU enters C3 state and SATA controller is not active, this function will assert SMARTVOLT/GPIO4. System design can use this signal to control the power supply to reduce the ATA power by 5~10%. Another example is to connect an ambient light sensor to one of the VIN inputs. When the circuit has detected the ambient light is below certain threshold, this function can automatically dim the LCD back light. Note this is an aggressive power management function outside of OS control and it is platform specific.			

SmartVolt2En - RW – 8/16/32 bits - [PM_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
SmartVoltIdleTime	6:0	0h	Amount of “idle” time (in 2us increment) the SmartPower function should wait before it assert SmartVolt
SmartVoltEnable	7	0b	Enable bit for the SmartPower function. When set, the logic will monitor the logic defined by the “Check*” bits (bit8 ~ bit23). If all of the corresponding modules are idle, an internal SmartVoltEvent will be generated and the corresponding modules can use the SmartVoltEvent to do board level voltage control.
CheckVIN0	8	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN0 has reached or passed the threshold.
CheckVIN1	9	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN1 has reached or passed the threshold.
CheckVIN2	10	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN2 has reached or passed the threshold.
CheckVIN3	11	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN3 has reached or passed the threshold.
CheckVIN4	12	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN4 has reached or passed the threshold.
CheckVIN5	13	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN5 has reached or passed the threshold.
CheckVIN6	14	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN6 has reached or passed the threshold.

SmartVolt2En - RW – 8/16/32 bits - [PM_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
CheckVIN7	15	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN7 has reached or passed the threshold.
CheckC3	16	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if APU is in C3 state.
SmiCmdFixDisReserved	17	0b	Reserved
CheckSata	18	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if SATA is idle.
Reserved	19	0b	Reserved
CheckPciBridge	20	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if HD audio PCIBridge is idle.
Reserved	21	0b	Reserved
CheckAz	22	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if HD audio is idle.
CheckLpc	23	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if LPC is idle.
SmartVolt function is meant to provide a mechanism to control the external power supply in order to reduce additional system power consumption. For example, software can set Smart Power Control1 bit [6] and [7]. Whenever APU enters C3 state and SATA controller is not active, this function will assert SMARTVOLT/GPIO4. System design can use this signal to control the power supply to reduce the ATA power by 5~10%. Another example is to connect an ambient light sensor to one of the VIN inputs. When the circuit has detected the ambient light is below certain threshold, this function can automatically dim the LCD back light. Note this is an aggressive power management function outside of OS control and it is platform specific			

BootTimerEn - RW – 32 bits - [PM_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
FailBootTimer	24:0	0000000h	The counter of APU Boot timer (14.318MHz), which starts counting when all of the the following conditions are met: 1. Bit[31] of this register is set. 2. PCI reset is not asserted.
BootTmrFuncEn	27	1b	0: Disable boot timer function. 1: Enable boot timer function.
BootTmrStopOnGAlink	28	1b	Set to 1 to stop boot timer when FCH observes the good boot after PCI reset.
ExpireBootTmr	29	0b	Set to 1 to force boot timer to expire
FailBootRstSts	30	0b	0: Boot timer has not been fired. 1: Boot timer has been fired. Write 1 to clearit to 0.
BootTmrDisable	31	0b	Set to 1 to stop boot timer.

WatchDogTimerEn - RW – 32 bits - [PM_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
WatchDogDecodeEn	0	0b	Set to 1 to enable decoding of WatchDogTimer address. WatchDogTimer is a standard defined by Microsoft®
WatchDogFunDisable	1	0b	1: Disable WatchDog function 0. Enable WatchDog function
Reserved	2		
WatchDogBase	31:3	0000000h	WatchDogTimer base address

WatchDogTimerConfig - RW – 8 bits - [PM_Reg: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
WatchDogFreq	1:0	11b	Defines the clock frequency used by the WatchDogTimer. 00: 32KHz 11: 1Hz
TempScratch	3:2	xx	Scratch registers - can be used for temporary data
Reserved	7:4	00b	

HPETEn - RW – 8 bits - [PM_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
HPETDecodeEn	0	0b	Set to1 to enable HPET MMIO space decoding.
HPETIRQEn	1	0b	Set to1 to enable HPET IRQ output.
HPET_Timer0_MSI_en	2	0b	Set to1 enable HPET timer0 MSI capability.
HPET_Timer1_MSI_en	3	0b	Set to1 enable HPET timer1 MSI capability.
HPET_Timer2_MSI_en	4	0b	Set to1 enable HPET timer2 MSI capability.
Reserved	7:5	-	
HPETBaseAddress	31:10	3FB400h	HPET MMIO base is FED0_0000h by default.

SerialIrqConfig - RW – 8/16 bits - [PM_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
NumStartBits	1:0	00b	This field defines the number of clocks in the start frame. Start Frame Width = 4 + 2 * NumStartBits
NumSerIrqBits	5:2	0h	Total number of serial IRQ's = 17 + NumSerIrqbits 0: 17 serial IRQ's (15 IRQ, SMI#, + IOCHK#) 1: 18 serial IRQ's (15 IRQ, SMI#, IOCHK#, INTA#) ... 15: 32 serial IRQ's The serial IRQ can support 15 IRQ#, SMI#, IOCHK#, INTA#, INTB#, INTC#, and INTD#. When serial SMI# is used, BIOS will need to check SIO (or device that generates serial SMI#) for status.
SerIrqMode	6	0b	0: Continuous mode 1: Active (quiet) mode
SerialIrqEnable	7	0b	Setting this bit to 1 enable the serial IRQ function.
Reserved	13:12	-	

RtcControl - RW – 8 bits - [PM_Reg: 56h]			
Field Name	**Bits**	**Default**	**Description**
Rt cProtect38_3F	0	0b	When set, RTC RAM index 38:3Fh will be locked from read/write. This bit can only be written once.
RtcProtectF0_FF	1	0b	When set, RTC RAM index F0:FFh will be locked from read/write. This bit can only be written once.
RtcProtectE0_EF	2	0b	When set, RTC RAM index E0:EFh will be locked from read/write. This bit can only be written once.
RtcProtectD0_DF	3	0b	When set, RTC RAM index D0:DFh will be locked from read/write. This bit can only be written once.
RTCProtectC0_CF	4	0b	When set, RTC RAM index C0:CFh will be locked from read/write. This bit can only be written once.
Rtc_test_en	6	0b	This is the test enable for the RTC 32KHz oscillator control bits (rtc_osc_set0, rtc_osc_set1).
Rtc_osc_set_en	7	0b	This is the latch enable for the RTC 32KHz oscillator control bits (rtc_osc_set0, rtc_osc_set1).
Rtc_osc_set0	8	0b	RTC oscillator control bit

RtcControl - RW – 8 bits - [PM_Reg: 56h]			
Field Name	**Bits**	**Default**	**Description**
Rtc_osc_set1	9	0b	RTC oscillator control bit
RtcClkDrive	10	1b	0: HIGHDRIVE tied low for RtcClkOut pad 1: HIGHDRIVE tied high for RtcClkOut pad
Mask_rtc_clk_out	11	0b	Set to1 to disable RtcClk output.
CenturyEn	12	1b	Enable RTC Century support.
AltCmosMapEn	13	0b	When enabled, bank 1 of CMOS RAM is changed. Index 00:0D will still return the time and alarm settings. Index 0E:7F will return the absolute offset 8E:FF.
ExtraRTCCMOSEn	14	0b	When it is 1, SW can access the extra 16 bytes of RTC CMOS RAM.

VRT_T1 - RW – 8 bits - [PM_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
VRT_T1	7:0	01h	To conserve power, the RTC battery is sampled periodically for checking its state of health. VRT_T1 and VRT_T2 make up the interval of the checking. When VRT_Enable is high, the battery is being sampled. When VRT_enable is low, the battery is not being sampled. This register defines the time of VRT enable being high for RTC battery monitor circuit, in milliseconds.

VRT_T2 - RW – 8 bits - [PM_Reg: 59h]			
Field Name	**Bits**	**Default**	**Description**
VRT_T2	7:0	FFh	This register defines the time of VRT enable being low for the RTC battery monitor circuit, in 4 ms increments.

IntruderControl - RW – 8 bits - [PM_Reg: 5Ah]			
Field Name	**Bits**	**Default**	**Description**
IntruderAlertDis	0	1b	Set to 0 to enable IntruderAlert.
IntruderAlertClr	1	0b	Write 1 to clear the IntruderAlert status bit.
IntruderAlertSts	2	0b	The status bit will be set to 1 if an Intruder alter has been occurred Software need to set bit1 to clear the status bit.
CmosEraseDis	4	1b	Set to1 to disable CMOS Erase.
CmosEraseClr	5	0b	Write to 1 to clear CMOS Erase status.
CmosEraseSts	6	0b	Indicate that a CMOS Erase has been occurred.

RtcShadow - RW – 8 bits - [PM_Reg: 5Bh]			
Field Name	**Bits**	**Default**	**Description**
Writing to bits[3:0] will set the value onto bits[7:4]. Software should always set bit [2] = 1 for this operation.			
PwrFailShadow (Write only)	1:0	00b	These two bits will determine how system should resume after a power failure. 00: Always off—always power off after power resumes 01: Always on—always power on after power resumes 10: Always off—always power off after power resumes 11: Use previous—resume to same setting when power fails

RtcShadow - RW – 8 bits - [PM_Reg: 5Bh]			
Field Name	**Bits**	**Default**	**Description**
PowerState (Write only)	2	0b	This bit should be set to 1 by software. If this bit is '0' the Power fail function may not function correctly. Power state indicator. 0: Off 1: On
ForcePwrOn (Write only)	3	0b	0: If RTC AIE = 1, will wakeup when RTC alarm fires after a power failure/resume. (See Note) 1: If RTC AIE =1, will force power on after power resumes regardless of Bit[5:4] setting. (See Note)
Note: RTC_AIE is defined at RTC_Reg:0Bh[5].			
The following bits can be written to only by setting the corresponding 3:0 bits. Values written to bits [3:0] will be reflected and be Read-only in bits[7:4].			
PwrFailShadow (Read only)	5:4	00b	These two bits will determine how the system should resume after a power failure. 00: Always off—always power off after power resumes 01: Always on—always power on after power resumes 10: Always off—always power off after power resumes 11: Use previous—resume to same setting when power fails
Note: On the first power up of the VBAT and S5 3.3 V power rails (both power rails transition from Off to On) the contents of this register are not valid until the system BIOS writes valid settings to it.			
PwrFailShadow	3:0	0h	Writing to these four bits will set the value onto bits[7:4]. Software should always set bit [2] = 1.
PwrFailOption	5:4	00b	These two bits will determine how system should resume after a power failure. 00: Always off—always power off after power resumes 01: Always on—always power on after power resumes 10: Always off—always power off after power resumes 11: Use previous—resume to same setting when power fails
PowerState	6	0b	Power state indicator. 0: Off 1: On
ForcePwrOn	7	0b	0: If RTC AIE = 1, will wakeup when RTC alarm fires after a power failure/resume. (See Note) 1: If RTC AIE =1, will force power on after power resumes regardless of Bit[5:4] setting. (See Note)
Note: RTC_AIE is defined at RTC_Reg:0Bh[5].			

LLBCntrl - RW – 8 bits - [PM_Reg: 5Ch]			
Field Name	**Bits**	**Default**	**Description**
BlockWakeEn	0	0	Set 1 to block wake event if LLB# is asserted. But if UseAsWakeEn and AllowWakeS3En are all set to 1, LLB# and other wake events can wake the system up from S3.
UseAsWakeEn	1	0	Set to 1 to treat LLB# as wake event.
AllowWakeS3En	2	0	Set to 1 to allow LLB# as wake event in S3.

Reserved - RW – 8 bits - [PM_Reg: 5Dh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

RtcExtIndex - RW – 8 bits - [PM_Reg: 5Eh]			
Field Name	**Bits**	**Default**	**Description**
index	7:0	-	Specify the offset of RTC Extended Registers to be read/written from PM_REG:5Fh

RtcExtData - RW – 8 bits - [PM_Reg: 5Fh]			
Field Name	**Bits**	**Default**	**Description**
Data	7:0	-	Read data or writte data of RTC Extended Registers

AcpiPm1EvtBlk - RW – 8/16 bits - [PM_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
AcpiPm1EvtBlk	15:2	0000h	These bits define the least significant byte of the 16 bit I/O range base address of the ACPI power management Event Block. Bit 2 corresponds to Addr[2] and bit 7 corresponds to Addr[7].

AcpiPm1CntBlk - RW – 8/16 bits - [PM_Reg: 62h]			
Field Name	**Bits**	**Default**	**Description**
AcpiPm1CntBlk	15:1	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management Control block. Bit 1 corresponds to Addr[1] and bit 7 corresponds to Addr[7].

AcpiPmTmrBlk - RW – 8/16 bits - [PM_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
AcpiPmTmrBlk	15:1	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management Timer block. Bit 1 corresponds to Addr[1] and bit 7 corresponds to Addr[7].

P_CNTBlk - RW – 8/16 bits - [PM_Reg: 66h]			
Field Name	**Bits**	**Default**	**Description**
CpuControl	15:3	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management APU Control block. Bit 3 corresponds to Addr[3] and bit 7 corresponds to Addr[7]. Addr[2:0] are ignored because this register block is 6 byte long.

AcpiGpe0Blk - RW – 8/16 bits - [PM_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
AcpiGpe0Blk	15:2	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management General Purpose Event block. Bit 2 corresponds to Addr[2] and bit 7 corresponds to Addr[7]. Addr[1:0] are ignored because this register block is 4 byte long.

AcpiSmiCmd - RW – 8/16 bits - [PM_Reg: 6Ah]			
Field Name	**Bits**	**Default**	**Description**
AcpiSmiCmd	15:0	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI SMI Command block. Bit 0 corresponds to Addr[0] and bit 7 corresponds to Addr[7]. The address is required to be WORD-aligned (Addr[0]=0)

AcpiPm2CntBlk - RW – 16 bits - [PM_Reg: 6Eh]			
Field Name	**Bits**	**Default**	**Description**
AcpiPm2CntBlk	15:0	0000h	These bits define the most significant byte of the 16 bit I/O base address. Bit 0 corresponds to Addr[8] and bit 7 corresponds to Addr[15].

AcpiConfig - RW – 8/16/32 bits - [PM_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
Decen_acpi	0	0b	Set to 1 to enable decoding of the standard ACPI registers
Gbl_en_en	1	0b	Set to 1 to enable GBL function in the standard ACPI - PmControl register.
Rtc_en_en	2	0b	Set to1 to enable RTC_EN function in the standard ACPI register. This is designed as a backdoor for BIOS to control it.
Slpbtn_en_en	3	0b	Set to1 to enable SLPBTN_EN function in the standard ACPI register. This is designed as a backdoor for BIOS to control it
Tmr_en_en	4	0b	Set to 1 enable TMR_EN function in the standard ACPI register. This is designed as a backdoor for BIOS to control it.
Reserved	5	-	
MaskArbDis	6	1b	Set to1 to disable ArbDis function in the ACPI register. ArbDis is not really used, but it still needs to be accessible by OS.
BIOS_RLS	7	0b	Set to1 to generate SCI. Read always return 0
PCIeNative	24	0b	Setting to 1 will block PCIe GPP PME message and HotPlug message from generating SCI. This is used for supporting ACPI 3.0 specification. If ACPI 3.0 is not supported, this bit should be left as 0
PCIE_WAK_Mask	25	0b	Set to1 to disable PCIE_WAK_STS and PCIE_WAK_DIS function. This is used for supporting ACPI 3.0 specification. If ACPI 3.0 is not supported, this bit should be left as 1
Reserved	26		
WakePinAsGevent	27	0b	Set to 1 to treat Wake# pin as Gevent input.
PcieGeventMap	28	0b	Set to 1 to route pme message from NB to gevent 24, Hotplug message from APU to gevent 7.
RtcWakeAlarm	29	1b	Set to 1 to only rtc alarm to wake up the system.

WakeIoAddr - RW – 16 bits - [PM_Reg: 78h]			
Field Name	**Bits**	**Default**	**Description**
WakeIoBaseAddress	15:0	FFFFh	The register specifies the wake I/O address. Any I/O write to the I/O address can cause APU to wake from C state. This is an obsolete function that is not used anymore.

HaltCountEn - RW – 16 bits - [PM_Reg: 7Ah]			
Field Name	**Bits**	**Default**	**Description**
NumOfHalt	3:0	0000b	Defines the number of HALT messages to track before FCH should initiate C1e sequence. This is meant for server platform where message base C1e is used.
CountHaltMsgEn	15	0b	When set, FCH will keep track of APU state by counting HALT entering and exit messages. When the number of net HALT enter messages match with NumOfHalt, FCH will initiate C1e.

C1eWrPortAdr - RW – 16 bits - [PM_Reg: 7Ch]			
Field Name	**Bits**	**Default**	**Description**
C1eWrPortAdr	15:0	FFFFh	I/O write decoding Base address. Write to this IO address will cause FCH to initiate C1e sequence. This is an obsolete function that is not used anymore

CStateEn - RW – 16 bits - [PM_Reg: 7Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	-
C2ToC3Enable	2	0b	Set to 1 to put APU into C3 even it is P_LVL2 Io read.
C2EnhanceEn	3	0b	Set to1 to enable C2 enhancement.
C1eToC2En	4	0b	Set to 1 to put APU into C2 state in C1e state.
C1eToC3En	5	1b	Set to 1 to put APU into C3 state in C1e state.
CPopUpEn	6	1b	Set to1 to enable pop up capability, which means going to C2 if there is a traffic and back to C3 after idle for a while. This bit should be set to 0 when AltVid is not enabled.
Reserved	7	-	
oAllowLdtStpAsOut	8	0b	Control the input/output direction of pin AllowLdtStp. 0: (default) AllowLdtStp is input to FCH driven by APU. 1: AllowLdtStp as output pin to APU to indicate FCH traffic activities.
AllowLdtStpOutputEn	9	0b	Set to 1 to treat AllowLdtStp as output to notify APU that there is potential traffic from FCH
MaskCStateSys	14	0b	Set to 1 to skip C state if there is pending interrupt smi, nmi, init request.
Mask_intr_en	15	1b	If set, the APIC interrupt will be deferred until the first ACPI access after the system resumes from S state. In additional, A20M#, IGNNE#, INTR, NMI, INIT# messages will be deferred the same way, but SMI# will not be deferred. This is mainly to guard against unexpected interrupt being sent to OS during S1 resume.

BreakEvent - RW – 32 bits - [PM_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Bm_sts_rd_mask	0	0b	0: BM_STS bit in Pm1a_STS is set to1 if there is any DMA traffic in FCH. 1: Make BM_STS bit in Pm1a_STS always return 0 except for USB 1.1 traffic.
Auto_bm_rld	1	0b	When set, it will generate an internal BM_STS enable bit (that is similar to BM_RLD) upon entry to C1e. Depending on the configuration of other bits, bus master activity or IDLE_EXIT# pin could cause FCH to break out from C1e.

BreakEvent - RW – 32 bits - [PM_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Auto_clr_bm_sts	2	0b	It is used for PopUp and C1e function. Set to1 to automatically clear BM_STS before entering C1e state.
Reserved	3	-	
EnableBreak	4	0b	Set to 1 to skip the C state transition if there is break event when entering C state.
Reserved	6:5	-	Reserved.
BmReqEn	7	0b	Set to1 to treat BMREQ# as one source of Break Event
BmReqPopUpEn	8	0b	Set to 1 to allow PopUp if BMREQ# is toggled when PopUp function is enabled.
BusReqHoldEn	9	0b	Set to1 to extend BMREQ# until LDTSTP# is asserted.
MergeBMReqEn	10	0b	When set, the logic merges BMREQ# and AllowLdtStop together internally.
AutoStutterTimerEn	11	0b	This feature is specifically designed for multi-CPUs (as in server applications). Set to 1 to enable a AutoStutterTimer that will automatically count whenever LDTSTOP# is asserted during C3/C1e state. When the timer reaches the threshold (defined by AutoStutterLimit), it will stutter the C state machine. This feature is designed to periodically reconnect the HT link in the case of a long idle time.
AutoStutterTimeSel	12	0b	This bit selects the time increment used by the AutoStutterTimer 0: 2µs increment 1: 1ms increment
Reserved	13		
Usb11_BmStsEn *	16	0b	If this bit is set, any OHCI activity will cause ACPI.BM_STS to be set.
Usb11_SetBmSts *	17	1b	If this bit is set and AllowLdtStop/DMAACTIVE# pin is configured as output, any OHCI activity will assert DMAACTIVE#; this is to serve as a quicker way to bring the link between FCH and Fusion back to the active state. Under non-Fusion CPU, any activity from OHCI will cause FCH's C state logic to deassert LDT-STOP#.
Usb20_SetBmSts *	18	1b	If this bit is set and AllowLdtStop/DMAACTIVE# pin is configured as output, any EHCI activity will assert DMAACTIVE#; this is to serve as a quicker way to bring the link between FCH and Fusion back to the active state. Under non-Fusion CPU, any activity from OHCI will cause FCH's C state logic to deassert LDT-STOP#.
Reserved	19	0b	
Reserved	20	0b	Reserved
UsbIsoc_SetBmSts *	21	1b	This is similar to Usb11_SetBmSts except it only applies to USB isochronous traffic.
AutoStutterLimit	30:24	00h	This defines the limit for the AutoStutterTimer. Time unit is defined by bit 12
Reserved	31		
* These bits are not used by USB directly; rather they are only used inside ACPI for USB related functions.			

CStateControl - RW – 32 bits - [PM_Reg: 88h]			
Field Name	**Bits**	**Default**	**Description**
WaitStpGntEnB	0	0b	Set to1 to wait for STPGNT# in ACPI S state.
Reserved	1	0b	-
DlySlpEn	2	0b	Set to 1 to delay recognition of STPGNT# until there is no pending read in AB
Reserved	3	0b	-
Cc_en	4	0b	C State enable; must be set in order to exercise C state
Slp_en	5	0b	Enable LDTSTOP# as an output

CStateControl - RW – 32 bits - [PM_Reg: 88h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	11:6	-	.
StutterMode	12	0b	Set to 1 to enable stutter mode.
LdtStpCmd	13	0b	Set to 1 from 0 to force FCH to toggle LDTSTP#.

PopUpEndTime - RW – 8 bits - [PM_Reg: 8Eh]			
Field Name	**Bits**	**Default**	**Description**
PopUpEndTime	7:0	10h	During C1e pop-up, FCH monitors internal DMA traffic. If there has been no traffic for PopUpEndTime, FCH will bring system back to C1e. The time is counted by 14.318MHz clock. This can considered as a minimum LDTSTOP deassertion time; however, this has been combined into LdtStartTime (PMIO_94[23:16]), and is not really required.

CStateTiming0 - RW – 8/16/32 bits - [PM_Reg: 94h]			
Field Name	**Bits**	**Default**	**Description**
StutterTime	7:0	01h	LDTSTP# duration in 1µs increments. This is basically the minimum LDTSTOP assertion time
S_LdtStartTime	15:8	00h	This register defines the delay between LPC_PD# (previously called LPC_PD#) assertion and LDTSTP# assertion when the system enters ACPI S states, in 1µs increments, with 1µs uncertainty.
LdtStartTime	23:16	10h	LDTSTP# deassertion time (in 1µs increments) in C state
LdtEndTime	25:24	00b	LDTSTP# de-assertion delay select. 00: 0µs 01: 1µs 10: 32µs 11: 64µs This is the delay from deassertion of LDTSTOP# till the deassertion of STPCLK

CStateTiming1 - RW – 8/16/32 bits - [PM_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
StpClkDlyTime	7:0	00h	Additional STPCLK# deassertion delay in number of OSC clocks for S1 resume.
FirstLdtStartTime	15:8	10h	Very first LDTSTOP# assertion delay (in 1µs increments) from reception of STPGNT.
Reserved	25:24	-	
VidFidTime	30:28	01b	VID/FID LDTSTP# duration select. 000: 1µs 001: 2µs 010: 4µs 011: 8µs 100: 16µs 101: 32µs 110: 64µs 111: 128µs

C2Count - R – 8 bits - [PM_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
C2Count	7:0	00h	The value shows the amount of time the APU spends in STPGNT state (but LDT_STOP# is not asserted) during C1e. Each increment represents approximately 0.39% (1/256). This register is updated by HW automatically every second.

C3Count - R – 8 bits - [PM_Reg: 9Dh]			
Field Name	**Bits**	**Default**	**Description**
C3Count	7:0	00h	The value shows the amount of time LDT_STOP# is asserted during C1e. Each increment represents approximately 0.39% (1/256). This register is updated by HW automatically every second.

Reserved- R – 8 bits - [PM_Reg: 9Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

MessageCState - RW – 8/16/32 bits - [PM_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
oBattModeChgMsgEn	0	0b	When enabled, FCH will automatically send a message to CPU indicating the power mode (AC vs battery). In addition, every time it is changed, FCH will generate a message to indicate the update.
TimerTickChgMsgEn	1	0b	When enabled, FCH will send a message to APU indicating the latest periodic timer interval. FCH will automatically determine which timer (PIT, RTC, or HPET) is being used.
FusionCEnable	2	0b	Set to1 to enable the FCH Fusion C state coordination logic. Fusion CPU contains the actual C state logic and FCH contains the coordination logic which sends handshake message to CPU to help it to decide which C state to go into.
FusionPerr_en	3	0b	When enabled, FCH C state coordination logic will cause CPU to exit from C state when there is a parity error within the FCH.
FusionSerr_en	4	0b	When enabled, FCH C state coordination logic will cause CPU to exit from C state when there is a system error within the FCH.
Reserved	5	0b	Reserved.
BatteryModeEn	6	0b	When set, a change in power mode (battery vs AC) will cause FCH to tell CPU to exit from C state.
SelfExitEnable	7	0b	When set, FCH will exit to C0 state from non-C0 state when there is a break event and exit to C1 state from non-C0 state when there is traffic.
WakeByIMC	8	0b	A static bit that can be written by IMC to cause FCH to generate C state exit message to CPU.
PopUpByIMC	9	0b	A static bit that can be written by IMC to cause FCH to pop up C state message to CPU.
ClkIntrTagEn	10	0b	When enabled, FCH will mark the periodic timer interrupt.
ExtendEnable	11	0b	When enabled, FCH will start a timer whenever the C state is exited. The purpose is to prevent CPU from going back to C state before the timer expires.

MessageCState - RW – 8/16/32 bits - [PM_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
UsbOhciModeFusion[1:0]	13:12	00b	These bits are to be used with Fusion CPU C state. If bit 0 is set, FCH will stutter the CPU C state whenever USB OHCI has pending traffic. If bit 1 is set, FCH will cause CPU to break out from C state when USB OHCI has pending traffic. These bits affect AltVid entry and should be set to 01 only when AltVid is enabled; otherwise leave at 00.
UsbEhciModeFusion[1:0]	15:14	00b	These bits are to be used with Fusion CPU C state. If bit 0 is set, FCH will stutter the CPU C state whenever USB EHCI has pending traffic. If bit 1 is set, FCH will cause CPU to break out from C state when USB EHCI has pending traffic. These bits affect AltVid entry and should be set to 01 only when AltVid is enabled; otherwise leave at 00.
TmrSelOverride	20:16	00000b	This is to be used with bit TimerTickChgMsgEn. In case FCH auto-timer detection logic is not functioning properly, one can use these bits to override the logic and force the logic to monitor the specific timer. Bit 0 - When set, use HPET Bit 1 - When set, use RTC Bit 2 - if HPET is selected, setting bit 2 will force the logic to monitor HPET timer 0. Bit 3 - if HPET is selected, setting bit 3 will force the logic to monitor HPET timer 1. Bit 4 - if HPET is selected, setting bit 4 will force the logic to monitor HPET timer2.
FusionReadState	22	0b	This is for debugging purpose. When set, bits [15:0] of this register will return Fusion C state logic signals.
MultiCoreEn	23	0b	When set, C state control logic inside FCH will assume multi-core configuration. NumOfCpu (PM_Reg x7A) should be programmed accordingly. FCH keeps track of CPU C state by monitoring each core's C state message instead of package state.
ExtendValue	30:24	00000000b	Timer value to be used with ExtendEnable. The value is the number of 66MHz clocks.
CheckCoreIdDis	31	0b	1: Ignore Core Id check when MultiCoreEnbit set 1. 0: Enable Core Id check when MultiCoreEnbit set 1.

TrafficMonitorEn - RW – 8/16/32 bits - [PM_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
PerfMonEn	0	0b	When set, FCH will monitor the amount of DMA traffic by the individual enable bits (bits 5 through 12) and the number of interrupts within the monitored interval (defined by bits 25:24)
TrafficSciEn	1	0b	When set, FCH will generate an SCI when the amount of traffic is less than idleTimeLimit (PM_Reg A8h)
InterruptSciEn	2	0b	When set, FCH will monitor the number of interrupts occurring within the monitor period. If the number of interrupts is less than the number defined in IntrTimeLimit (PM_Reg AAh), FCH will generate an SCI.
CheckInterrupt	3	0b	To be used with bit 2 to monitor interrupts.
CheckC3	4	0b	To be used with bit 1. When set, FCH will only consider the system is in idle state if CPU is in C state.
CheckGec	5	0b	To be used with bit 1. When set, FCH will monitor GMAC traffic.
CheckSata	6	0b	To be used with bit 1. When set, FCH will monitor SATA traffic.
CheckUsb	7	0b	To be used with bit 1. W hen set, FCH will monitor USB traffic.
CheckPcib	8	0b	To be used with bit 1. When set, FCH will monitor PCIBridge traffic.

TrafficMonitorEn - RW – 8/16/32 bits - [PM_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
CheckAz	9	0b	To be used with bit 1. When set, FCH will monitor HD audio traffic.
CheckLpc	10	0b	To be used with bit 1. When set, FCH will monitor LPC traffic.
CheckGpp	11	0b	To be used with bit 1. W hen set, FCH will monitor GPP traffic.
CheckFc	12	0b	To be used with bit 1. W hen set, FCH will monitor FC (NAND flash) traffic.
LanEnergyDetectEn	13	0b	Enable SCI generation due to LAN energy detect status change.
MaskIntrToCState	14	0b	When set, interrupt will be masked off internally and will not cause FCH to generate Exit message to FusionCPU. This function is only applicable to FusionCPU configuration.
Reserved	23:15	0	Reserved.
PerfMonPeriodSel	25:24	00b	Traffic monitor period selection. To be used when PerfMonEn (bit0) is set to enable. 00: 15ns between each count and the monitored interval is ~1ms. 01: 240ns between each count and the monitored interval is 15.67ms. 10: 1.92µs between each count and the monitored interval is 125.3ms. 11: 15.36µs between each count and the monitored interval is ~1 second.
TrafficLess	26	0b	0: Monitor whether idle number is less than IldeTimeLimit. 1: Monitor whether Idle number is more than IdleTimeLimit.
IntrLess	27	0b	0: Monitor whether interrupt number is more than IntrTimeLimit. 1: Monitor whether interrupt number is less than IntrTimeLimit
ModFusionCHandShakeEn	28	0b	0: Fusion C-state logic will use a 3-way handshake protocol: CPU->C1 entry message FCH -> C-state allow message CPU -> C-state taken message 1: Fusion C-state logic will use a 2-way handshake protocol CPU -> C1 entry message FCH -> C-state allow message From there, FCH will assume CPU will take the highest C state indicated by the C-state allow message
TrafficSciSts	29	0b	Read only. Can be cleared by set TrafficSciEn to 0. 0: Traffic monitor Sci event doesn't happen 1: Traffic monitor Sci event has been fired
IntrSciSts	30	0b	Read only. Can be cleared by set InterruptEn to 0. 0: Interrupt monitor Sci event doesn't happen 1: Interrupt monitor Sci event has been fired
PMIO_A4_Sel	31	0b	When it is 0, this register (PM_Reg:A4h) is the TrafficMonitorEn register. When it is 1, this register (PM_Reg:A4) is selected to be TrafficStatus register. In both cases, this bit has same definition.
The register is TrafficMonitorEn when bit 31 is 0. If bit 31 is 1, it returns the traffic status of the respective status.			

TrafficStatus - RW – 8/16/32 bits - [PM_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	4:0	00000b	Reserved.
GecTrafficStatus	5	-	Indicates whether GEC is active. 0: Inactive 1: Active
SataTrafficStatus	6	-	Indicates whether SATA is active. 0: Inactive 1: Active
UsbTrafficStatus	7	-	Indicates whether USB is active. 0: Inactive 1: Active
PcibTrafficStatus	8	-	Indicates whether PCIBridge is active. 0: Inactive 1: Active
AzTrafficStatus	9	-	Indicates whether HD audio is active. 0: Inactive 1: Active
LpcTrafficStatus	10	-	Indicates whether LPC is active. 0: Inactive 1: Active
GppTrafficStatus	11	-	Indicates whether GPP is active. 0: Inactive 1: Active
FcTrafficStatus	12	-	Indicates whether FC is active. 0: Inactive 1: Active
GecEnergyDetectStatus	13	-	Indicates whether LAN energy detect is active. 0: Inactive 1: Active
FusionCState	15:14	00b	Status of fusion C state monitor
FusionCState0	17:16	00b	Status of fusion C state monitor for core pair 0
FusionCState1	19:18	00b	Status of fusion C state monitor for core pair 1
FusionCState2	21:20	00b	Status of fusion C state monitor for core pair 2
FusionCState3	23:22	00b	Status of fusion C state monitor for core pair 3
Reserved	30:24	0	Reserved.
PMIO_A4_Sel	31	0b	When it is 0, this register (PM_Reg:A4h) is the TrafficMonitorEn register. When it is 1, this register (PM_Reg:A4) is selected to be TrafficStatus register. In both cases, this bit has the same definition.
The register is TrafficStatus when bit 31 is 1. If bit 31 is 0, it is TrafficMonitorEn.			

TrafficMonitorIdleTime - RW – 8/16 bits - [PM_Reg: A8h]			
Field Name	**Bits**	**Default**	**Description**
IdleTimeLimit	15:0	0000h	To be used with PerfMonEn. This defines the amount of DMA traffic limit that will cause FCH to generate SCI. Time granularity is defined by PerfMonPeriodSel.

TrafficMonitorIntTime - RW – 8/16 bits - [PM_Reg: AAh]			
Field Name	**Bits**	**Default**	**Description**
IntrTimeLimit	15:0	0000h	To be used with PerfMonEn. This defines the amount of interrupt limit that will cause FCH to generate SCI. Time granularity is defined by PerfMonPeriodSel.

TrafficMonitorTrafficCount - RW – 8/16 bits - [PM_Reg: ACh]			
Field Name	**Bits**	**Default**	**Description**
TrafficCount	15:0	0000h	Actual recorded value of the combined DMA traffic during the monitored period.

TrafficMonitorIntrCount - RW – 8/16 bits - [PM_Reg: AEh]			
Field Name	**Bits**	**Default**	**Description**
IntrCount	15:0	0000h	Actual recorded value of the number of interrupts during the monitored period.

TrafficMonitorTimeTick - RW – 8/16 bits - [PM_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
DeferTimerTickEn	0	0b	When set, FCH will skip a number of timer tick interrupts based on the defined value in DeterTimeTickValue when CPU is in C state. When CPU is not in C state, FCH will not skip any timer tick interrupts.
ForceTmrTickEn	1	0b	If bit 0 is set along with this bit and FCH has skipped a timer tick interrupt, FCH will immediately generate the timer tick interrupt upon C state exit
DeferTimerTickValue	10:8	000b	000: No skipping 001: Skip 1 timer tick 010: Skip 2 timer ticks 011: Skip 3 timer ticks 100: Skip 4 timer ticks 101: Skip 5 timer ticks 110: Skip 6 timer ticks 111: Skip 7 timer ticks

Reserved - RW – 8 bits - [PM_Reg: B2h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

FidVidControl - RW – 8/16 bits - [PM_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
Fid_protect_en	0	0b	Set to 1 to skip C-state transition when FID/VID message is received concurrently.
LDTSTPBTmrSel	1	0b	Configure the behavior of “DMA/Interrupt indicator”: Select 2us or 4us toggling on DMAACTIVE_L (ALLOWLDTSTP) or LDTSTPB_L according to Merge_Interrupt_Dma_Reg value. 0: 2µs 1: 4µs

FidVidControl - RW – 8/16 bits - [PM_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
IntrOnLdtStpBEn	2	0b	Configure the behavior of “DMA/Interrupt indicator” : Change the definition of LdtStpB pin to “interrupt indicator”. 0: LdtStpB behaves as C1e function 1: LdtStpB behaves as interrupt indicator When this bit is 1 and there is an interrupt, LdtStpB pin will toggle in the rate defined in LDTSTPBTmrSel.
MergeAllowLdtStpWithLdtStp	3	0b	Configure the behavior of “DMA/Interrupt indicator” : Change the definition of pin DMAACTIVE_L (ALLOWLDTSTP). 0: Drive DMAACTIVE_L to low when there is pending upstream request. 1: Output 2us/4us toggling on DMAACTIVE_L (ALLOWLDTSTP) when there is a pending interrupt request and not in C0 state to DMAACTIVE_L, othwewise drive DMAACTIVE_L to low when there is pending upstream request
WakeCStateInSlp	4	0b	Configure the behavior of “DMA/Interrupt indicator” : 0: Do not check C State before entering S State. 1: Force to C0 State before entering S State.
LdtStpBOutputDis	5	0b	Configure the behavior of “DMA/Interrupt indicator” : Disable LdtStpB output: 0: LdtStpB output enabled 1: LdtStpB output disabled
ServerCGateWhenThrot_en	6	0b	Set to 1 to force ServerCGate to not assert when sending StpClk message for throttling.
	7	0b	Reserved
DelayLDTSTP	8	0b	Set to 1 to enable LDTSTP# assertion time
FidVidOption	11:9	000b	Additonal FIDVID exit delay 3’b000: 0ns 3'b001: 140ns 3'b010: 210ns 3'b011: 280ns 3'b110: 350ns 3'b111: 420ns 3'b100: 490ns 3'b101: 560ns
LinearRangeOutLimit	23:20	0000b	This register specifies the temperature threshold to control Fan0 duty cycle change when the current temperature for Fan0 has been out of LinearRange limit and Fan0 is trying to capture the current temperature.
Tpreset1b	29:24	000101b	Timing parameter used for S* -> S0 state transition. This determines the delay between CPU_STP# de-assertion and LPC_PD# de-assertion, in 8µs increment with 8µs uncertainty.

TPRESET2 - RW – 8 bits - [PM_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
TPRESET2	5:0	08h	Timing parameter used for S* -> S0 state transitions. This register determines the LDTSTOP# deassertion delay in 8µs increment with 8µs uncertainty.
ClkGateCntrl	7:6	10b	These two bits control whether SMBUS module will allow clock gating to the internal 66Mhz core clock 00: Disable the clock gating function 01: Wait 16 clocks before allowing clock gating to the SMBUS module 10: Wait 64 clocks before allowing clock gating to the SMBUS module 11: Wait 256 clocks before allowing clock gating to the SMBUS module

Reserved – RW – 8 bits - [PM_Reg: B9h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	000	
ClkRunDisable	3	0	Legacy DMA and serial IRQ logic reside in this module and they are running on the 33Mhz LPCCLK. Setting this bit will disable this module's ability to support CLKRUN# function from PCIBridge. In other words, when this bit is set, this module will prevent PCIBridge from stopping the 33Mhz clock
Reserved	7:4	0000	

S_StateControl - RW – 8/16 bits - [PM_Reg: BAh]			
Field Name	**Bits**	**Default**	**Description**
LongSLPS3	0	0b	Set to 1 to extend SLP_S3# assertion to 1s minimum.
AllowOffset	1	0b	Set to 1 to add extra delay for STPCLK. Only valid if AgpTimeAdj is set.
Reserved	2	-	
PmeMsgEn	3	0b	Set to 1 to enable PmeTurnOff/PmeMsgAck handshake.
Reserved	11:5	-	
Reserved	13		
WakePinEnable	14	0b	Set to 1 to enable wakeup from WAKE# pin.
MaskPmeMsgEn	15	0b	When set (along with PmeMsgEn=1), PmeAck message coming from PCIe device will be ignored and ACPI S state logic will solely use the timeout mechanism to sequence through the S3 state. This bit is used as an option to guard against multiple PmeAck messages coming from CNB and internal FCH PCIe bridge so FCH S state logic will not sequence into S3 state prematurely.

ThrottlingControl - RW – 16 bits - [PM_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**
AcpiThrotPeriod	1:0	00b	Selects the clock throttling period for both SW and HW thermal throttling 00: 15µs 01: 30µs 10: 244µs 11: Reserved
ThrottleControl	7:4	000b	Bit[4] Enable HW-based thermal clock throttle. This function is used in conjuction with TALERT#, PROCHOT#, or TEMPIN0. This HW-based thermal clock throttling has the same behavior as SW function (CLKVALUE register in ACPI register group) Bit[3:1] Throttle interval for STPCLK# de-assertion 000b: 50% 001b: 12.5% 010b: 25% 011b: 37.5% 100b: 50% 101b: 62.5% 110b: 75% 111b: 87.5%
ThermThrotPeriod	13	0b	Selects the thermal clock throttle period 0: 30µs 1: 244µs
NoWaitStpGntEn	14	0b	0: Wait for STPGNT after asserting STPCLK. 1: Do not wait for STPGNT after asserting STPCLK.
Therm2SecDelay	15	0b	Enable 2 second delay for thermal clock throttle.
Bits 15:4 are for controlling auto HW-initiated thermal throttling. When enabled, it will generate automatic thermal throttling on CPU if any of the hardware thermal events such as TALERT#, PROCHOT#, or themal diode sensor (TEMPIN0) is triggered			

ResetControl1 - RW – 8/16 bits - [PM_Reg: BEh]			
Field Name	**Bits**	**Default**	**Description**
SoftResetEn	0	0b	When this bit is set to 1, FCH will generate a break event to wake up CPU C-State before every warm reset.
Kb_pcirst_en	1	1b	Set to 1 to make PCI reset if KBRST# is asserted
CpuRstControl	3:2	0b	00: CpuReset is deasserted after PciReset. 01: CpuReset is deasserted as PciReset. 10: CpuReset is deasserted before PciReset. 11: CpuReset is deasserted after PciReset.
KbRstEn	4	1b	Set to 1 allow KB_RST# to do the PCI reset.
SLP_TYPEn Control	5	1b	Set to 1 to enable the function of SLP_TYPEn bit in PmControl register [AcpiPm1CntBlk:00h]. The SLP_TYPEn bit in PmControl register has no effect if this bit is clear.
HWM_ResetOption	6	1b	0: Hwm function(Pmio2 register block) is reset by RsmRst. 1: Hwm function(Pmio2 register block) is reset by PciRst.
RstToCpuPwrGdEn	7	0b	If set to 1, FCH toggles CPUPG on every reset.

ResetControl2 - RW – 8/16 bits - [PM_Reg: BFh]			
Field Name	**Bits**	**Default**	**Description**
UsrRstToNBPwrGdEn	0	1b	If set to 1, FCH toggles NB_PwrGD when reset button is pressed.
DelayRomRstEn	1	0b	0: ROM_RST functions the same as PciRst# 1: 30ms ahead of deassertion of PciRst#
DelayLanRstEn	2	0b	0: Lan_RST functions the same as PciRst# 1: 20ms ahead of deassertion of PciRst#
Gpio51ShutdownEn	3	0b	Shutdown system if seeing a negative edge on SHUTDOWN#/Gpio51
ResetPcie2	4	0b	This bit is to be used with GEVENT4 mux select bits. If GEVENT4 IO mux select bits are set to 10b, GEVENT4# pin will become PCIE_RST2#
Bypass_pwr_good	5	0b	If asserted, FCH will not wait for deassertion of PWRGOOD to monitor wakeup events.
PwrGoodOut	6	0b	Output data for PwrGood pin
PwrGoodEnB	7	1b	Output enable for PwrGood pin (active low)

S5/Reset Status - RW – 16 bits - [PM_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
ThermalTrip	0	0b	Write 1 to clear.
4SecondPwrBtn	1	0b	Write 1 to clear.
Shutdown	2	0b	Write 1 to clear.
ThermalTripFromTemp	3	0b	Write 1 to clear.
RemotePowerDownFromASF	4	0b	Write 1 to clear.
ShutDownFan0	5	0b	Write 1 to clear.
ShutDownFan1	6	0b	Write 1 to clear.
ShutDownFan2	7	0b	Write 1 to clear.
ShutDownFan3	8	0b	Write 1 to clear.
ShutDownFan4	9	0b	Write 1 to clear.
PwrGdDwnBeforeSlpS3	10	0b	Set to 1 to delay SLP_S3_by 64us and also qualify the FCH PwrGood with SLP_S3.
SlpS3ToLdtPwrGdEn	11	1b	Set to 1 to de-assert LDT_PWRGD as long as SLP_S3#goes low.
DisableLdtPwrGood	12	0b	LdtPwrGood Control. Set this bit to 1 to disable the LdtPwrGood assertion along with NBPwrGood.
DisSbToNbPG	13	0b	Set to1 to disable NBPwrGood.
PmeTurnOffTime	15:14	00b	00: 1ms 01: 2ms 10: 4ms 11: 8ms
UserRst	16	0b	Write 1 to clear.
Soft_pcirst	17	0b	Write 1 to clear.
Do_k8_init	18	0b	Write 1 to clear.
Do_k8_reset	19	0b	Write 1 to clear.
Do_k8_full_reset	20	0b	Write 1 to clear.
SleepReset	21	0b	Write 1 to clear.
Kb_reset	22	0b	Write 1 to clear.
Lt_reset	23	0b	Write 1 to clear.
FailBootRst	24	0b	Write 1 to clear.
WatchDogIssueReset	25	0b	Write 1 to clear.
RemoteResetFromASF	26	0b	Write 1 to clear.
Sync_flood	27	0b	Write 1 to clear.
Hang_reset	28	0b	Write 1 to clear.
Ec_WatchDogRst	29	0b	Write 1 to clear.
Reserved	31:30		Reserved
This register shows the source of previous reset.			

ResetCommand - RW – 8 bits - [PM_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Reset	0	0b	Writing 1 to do a PCI reset
MemRstDisable	1	0b	When set, the memory reset function at DDR_RST# pin will be disabled.
SelectDebug	2	0b	0: Select the PM_Reg C0 to be S5/Reset Status register. 1: Select the PM_Reg C0 to be a debug status register.
UsrRst2Pll	3	1b	Set to 1 to stop Pll when reset button is pressed.
ResetPcie	4	0b	Set to 1 to reset Gpp port.
ResetButtonEn	5	1b	Set to 1 to enable user reset input.
ResetAllAcpi	6	0b	Writing 1 to emulate a Reset Button event.
ResetEn	7	0b	0: Not allow to write bit 0 1: Allow to write bit 0.

CF9Shadow – RW – 8 bits – [PM_Reg:C5h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0		Reserved
SysRst	1	0b	0: Send INIT HT message 1: Reset as specified by bit3
RstCmd	2	0b	Write with 1 to generate reset as specified by bit[3,1]. Write only. Always read as 0.
FullRst	3	0b	0: Assert reset signals only 1: Place system in S5 state for 3 to 5 seconds
Reserved	7:4		Reserved

HTControl - RW – 16 bits - [PM_Reg: C6h]			
Field Name	**Bits**	**Default**	**Description**
HtIdleInterval	2:0	00b	This register defines the idle time between the two LDTSTP# assertions.
Reserved	6		
HtTimeInterval	7	0b	This bit defines HTIdle Interval. 0: Microsecond 1: Millisecond
HtAssertInterval	10:8	0b	This field defines the assertion time.
HtDelayStartTime	13:12	00b	This field defines the delay start time associated with the function in C6[6]h. The values are in microseconds. This is to allow the write to C6h[6] to be complete before FCH execute the test function.

Misc - RW – 32 bits - [PM_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
CPU_IO_PullDownDrvStrength	0	0b	When set, the integrated pull-down drive strength of all CPU IOs are increased by 50%.
Reserved	1	0b	
TFATAL_EN	2	1b	This bit enables both the soft PCIRST and the THRMTRIP function.
TDeadEn	3	1b	When set, GEVENT2 takes up the THRMTRIP function. When THRMTRIP pin is low and TFATAL_EN(bit2 of the same register) is set, hardware will switch the system to S5 automatically.
oUseAcpiStraps	4	0b	When set, it will use the config bits from index D8h and D9h to override the EpromStraps.

Misc - RW – 32 bits - [PM_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
Eprom/EFuseIndex Select	5	0b	If this bit is 0, PMIO D8h and D9h are for accessing the EPROM strap bits. When this bit is set to 1, PMIO D8h and D9h is for accessing the Efuse bits.
TwarnEn	6	0b	If set, it enables TALERT# pin
DisablePciRom	7	0b	Set to 1 to disable PCI from strap.
Temp_polarity	9:8	00b	Temperature polarity control for THRMTRIP and TALERT respectively. 0: Active low 1: Active high
LLB_En	10	0b	If set, LLB function is enabled, and system won't wakeup from ACPI S state until LLB# is de-asserted.
WriteBackEnable	11	0b	HD audio/modem write back enable. If set, the WakeOnRing status bit will be written back to HD Audio controller upon system power up.
S5ResetOverride	12	0b	Set to 1 to mask off internet PCI reset used in ACPI.
Id_change_en	13	0b	Setting this bit will allow the software to change the DeviceID and RevisionID.
Reserved	14	1b	
HideSmbus	15	0b	Set to1 to hide SMBus PCI cfg space and Lpc bridge is promoted to function 0.
BypassRomSel	17:16	00b	These two bits will override the two ROM strap pins. 00: LPC ROM 10: FWH ROM 11: SPI ROM 01: Reserved
UseBypassRom	18	0b	When this bit is set, it will override the ROM straps and use bits 3:2 of this register to determine which type of ROM to use. This is for BIOS debugging purpose or for system having multiple BIOSes on board.
UseCpuRst	19	1b	If this bit is not set, system reset will cause INIT# instead of CPURST#.
ProcHotStsEn	20	0b	Set to enable PROCHOT# to generate TwarnStatus and thermal throttle.
SpiDrvStr	21	1b	Set to 1 to enhance SPIHoldB drive strength.
ClkIntrVectorOrdEn	22	0b	When set, the system timer interrupt in the IOAPIC will be tagged with a value defined by ClkIntrVectorOrd
ClkIntrVectorOrd	31:24	00000000b	Specify the value used to indentify the clock interrupt.

IoDrvSth - RW – 8/16/32 bits - [PM_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
IoDrvSth_AD	2:0	111b	I/O drive strength* for AD[31:0], CBE0#, CBE1#, CBE2#, CBE3# , PAR, FRAME#, IRDY#, DEVSEL#, TRDY#, LOCK#, STOP#, PERR#, SERR#, CLKRUN#, and PCIRST#.
IoDrvSth_GNT	5:3	111b	I/O drive strength* for GNT#[4:0] pads.
IoDrvSth_ClkGrpA	8:6	111b	I/O drive strength* for PCICLK0 pads. The recommended setting for single load is 000b.
IoDrvSth_ClkGrpB	11:9	111b	I/O drive strength* for PCICLK[4:1] pads. The recommended setting for single load is 000b.
IoDrvSth_LPC	14:12	111b	I/O drive strength* for LPC LAD, LFRAME# pads. The recommended setting for single load is 111b.
IoDrvSth_Int	17:15	111b	I/O drive strength* for INTA#, INTB#, INTC#, INTD#, INTE#, INTF#, INTG#, and INTH# pads.
IoDrvSth_Req	20:18	111b	I/O drive strength* for REQ[3:0]# when they are configured as GPIO.
IoDrvSth_GpioA	23:21	111b	I/O drive strength* for BMREQ#, GPIO[0, 2, 4, 5, 7, 8, 9, 13, 37, 38, 39, 40], GPOC[0, 1] pads.
IoDrvSth_GpioB	26:24	111b	I/O drive strength* for GPIO3, and GPIO[48:52] pads.

IoDrvSth - RW – 8/16/32 bits - [PM_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
IoDrvSth_Misc	29:27	111b	I/O drive strength* for GA20, KBRST#, SERIRQ, and SATA_ACT# pads.
IoDrvSth_IDE	31:30	11b	I/O drive strength* for IDE interface.
***Note:** IO Drive Strength: Each three bit field controls the number of P and N transistors enabled in the final stage of the output driver for the designated pads. By controlling the number of transistors enabled, the designer can optimize the drive characteristics of signals based on the topology of their specific design.			

RstCntrl - RW – 8 bits - [PM_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	-	
RstLengthSel	7:6	00b	These two bits select which register will be at PM_Reg:D1h.

RstLength - RW – 8 bits - [PM_Reg: D1h]			
Field Name	**Bits**	**Default**	**Description**
RstLength	7:0	F4	When RstLengthSel=00b, the register is RstLength and this is for defining the ARST# length. The amount of reset time is equal to RstLegnth * 4096 * 69.84ns
This is RstLength when RstLengthSel = 00b			

APURstLength - RW – 8 bits - [PM_Reg: D1h]			
Field Name	**Bits**	**Default**	**Description**
APURstLength	7:0	FB	When RstLengthSel=01b, the register is APURstLength and this is for defining the APU_RST# length. The amount of reset time is equal to APURstLegnth * 4096 * 69.84ns

APUPwrGdLength - RW – 8 bits - [PM_Reg: D1h]			
Field Name	**Bits**	**Default**	**Description**
APUPwrGdLength	7:0	EA	When RstLengthSel=11b, the register is APUPwrGdLength and this is for defining the LdtPwrGd latency. The amount of delay is equal to APUPwrGdLegnth * 4096 * 69.84ns

PmioDebug - RW – 8 bits - [PM_Reg: D2h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	-	
ZeroLpcClk0En	3	0	BIOS should aways set it to 1 to enable LPCCLK0 power-down (driven to 0) when the following are true: 1. IMC is not enabled 2. In S3 or S5 This will ensure that the LPCCLK0 is low when SLP_S3#/ SLP_S5# are asserted
LpcClkDrvSth	5:4	00b	Drive strength control for LpcClk[1:0] respectively. 0: Clock output will be 4mA 1: Clock output will be 8mA
Cf9RstDisable	6	0b	When set, write to CF9 will not generate a reset. The purpose of this bit is to allow BIOS to trap CF9
IsaPmEn	7	0b	Set to 1 to allow legacy method of IO CD6/CD7 to access Pm register block.

ManualReset - RW – 8 bits - [PM_Reg: D3h]			
Field Name	**Bits**	**Default**	**Description**
AssertAPURstB	0	1b	When set to 0, it asserts APU_RST# low
AssertARstB	1	1b	When set to 0, it asserts A_RST# low
AssertPciRstB	2	1b	When set to 0, it asserts PCIRST# low
AssertSataRstB	3	1b	When set to 0, it asserts the reset to SATA controller
AssertUsbRstB	4	1b	When set to 0, it asserts the reset to USB controllers
AssertAzRstB	5	1b	When set to 0, it asserts the reset to AZ controller
AssertSDRstB	6	1b	When set to 0, it asserts the reset to SDIO controller
AssertGecRstB	7	1b	When set to 0, it asserts the reset to BIF core

IMCGating - RW – 8/16 bits - [PM_Reg: D6h]			
Field Name	**Bits**	**Default**	**Description**
IMC_GA20_Enable	0	0b	Set to1 to enable IMC A20# request.
IMC_KBRST_Enable	1	0b	Set to1 to enable IMC KBRST# request.
IMC_IRQ1_Enable	2	0b	Set to1 to enable IMC IRQ1 request.
IMC_IRQ12_Enable	3	0b	Set to1 to enable IMC IRQ12 request.
IMCWatchDogRstEn	4	0b	Set to 1 to allow IMC watchdog Reset to reset the system.
IMCUserResetEn	5	1b	Set to 1 to allow SYS_RST# to reset the system when IMC is enabled.
ToggleRsmRst	6	0b	Set to 1 to force RsmRstB input to 0.
GenIMCClkEn	10	0b	Set to 1 to enable IMC clk

Eprom/EfuseIndex - RW – 8 bits - [PM_Reg: D8h]			
Field Name	**Bits**	**Default**	**Description**
Eprom/EfuseIndex	7:0	00h	Index register to access Eprom setting (PM_regxC8[5]=0) or Efuse bits (PM_regxC8[5]=1). Write to this port sets the initial value of the index. Writing to the EpromStrapData port will auto-increment this index. Programming through the index/data port will not take effect until the next reset. This register is used as the index register to read the value of efuse when PM_regxC8[5] is set to 1.

Eprom/EfuseData - RW – 8 bits - [PM_Reg: D9h]			
Field Name	**Bits**	**Default**	**Description**
Eprom/EfuseData	7:0	00h	Data register to access Eprom bits (PM_regxC8[5] =0) or Efuse bits (PM_regxC8[5]=1). Writing to the EpromStrapData port will auto-increment the index at PMIO_CCh. Programming through the index/data port will not take effect until the next reset. This register is used as the data register to read the value of efuse when PM_regxC8[5] is set to 1.

SataConfig - RW – 16 bits - [PM_Reg: DAh]			
Field Name	**Bits**	**Default**	**Description**
SataEnable	0	1b	0: SATA controller is disabled 1: SATA controller is enabled
Reserved	1		
SetMaxGen2	2	0b	0: SATA controller operates in maximum Gen3 (3.0Gbps) speed 1: SATA controller operates in maximum Gen2 (3.0Gbps) speed and saves more power on PLL.
HiddenIDE	3	0b	0: IDE controller is exposed and Combined Mode is enabled. SATA controller has control over Port0 through Port3, IDE controller has control over Port4 and Port7. 1: IDE controller is hidden and Combined Mode is disabled, SATA controller has full control of all 8 Ports when operating in non-IDE mode.
Ref_Clk_Sel	5:4	01b	This is CP_PLL_REFCLK_SEL, the reference clock source selection for SATA PLL. 00: Reference clock from crystal oscillator via PAD_XTALI and PAD_XTALO 01: Reference clock from internal clock through CP_PLL_REFCLK_P and CP_PLL_REFCLK_N via RDL 10: Differential reference clock from PAD_XTALI and PAD_XTALO 11: Same as 10
Ref_Div_Sel	7:6	10b	This is CP_PLL_CLKR, the reference clock divider setting. 00: Divide by 1 (25MHz reference clock) 01: Divide by 2 10: Divide by 4 (100MHz reference clock) 11: Same as 10
Reserved	15:8	-	

DacCntrl - RW – 16 bits - [PM_Reg: DCh]			
Field Name	**Bits**	**Default**	**Description**
DacEn	0	1	Set to 1 to enable Dac.
DacRst	1	0	0: Dac runs at normal state 1: Dac is in reset state
DacCntrl[7:2]	7:2	00	Placeholder

Reserved - RW – 8 bits - [PM_Reg: DEh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

BlinkControl - R - 8 bits - [PM_Reg: DFh]			
Field Name	**Bits**	**Default**	**Description**
BlinkControl	1:0	00b	Blinking interval select 00: Always off *see Note 01: 1sec on, 3 sec off, repeating 10: 2 sec on, 2 sec off, repeating 11: Always on Note: B-Link is multiplexed with Gevent18. If using Gevent 18 function, the B-Link needs to be disabled by programming '00'.
Reserved	7:2	-	

ABRegBar - RW – 32 bits - [PM_Reg: E0h]			
Field Name	**Bits**	**Default**	**Description**
ABRegBar	31:0	00000000h	IO Base address of UMI register.

Reserved - RW – 8bits - [PM_Reg: E6h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

SDFlashCntrl - RW – 8bits - [PM_Reg: E7h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	-	
SDFlashEnable	4	0	0: Disable SD Flash controller interface 1: Enable SD Flash controller interface If this bit is set, GPIO[73:80] will be configured as SD Flash interface. If it is cleared, the interface is configured to GPIO. Note: Setting this bit to '0' or '1' will only disable/enable the interface between the internal SD controller and the external SD pins. The SD controller, enabled through a different set of registers, will not be affected; it will remain enabled or disabled depending on how it was programmed.
Reserved	7:5	-	

PcibConfig - RW – 8 bits - [PM_Reg: EAh]			
Field Name	**Bits**	**Default**	**Description**
PCIDisable	0	0b	When this bit is set, it will disable the PCI bus interface so the pins can be configured as GPIO.
PciBridgeMIoOverride	1	0b	When set, PCIBridge (Device 20h, function 4) memory and I/O enable are always true, even if its PCI memory and IO configuration bits are set to 0.

AzEn - RW – 8 bits - [PM_Reg: EBh]			
Field Name	**Bits**	**Default**	**Description**
AzEnable	0	1b	0: Disable HD audio controller 1: Enable HD audio controller
AzNoSnoopEnable	1	0b	When set, HD AUDIO data transfer will not cause the BM_STS bit to be set and to wake up the CPU from C3 state. Under current C1e implementation, there is no need to set this bit.

LpcGating - RW – 8 bits - [PM_Reg: ECh]			
Field Name	**Bits**	**Default**	**Description**
Lpc_enable	0	1b	Set to 1 to enable LPC bridge
Lpc_a20en	1	0b	Set to1 to enable A20# input.

UsbGating - RW – 8 bits - [PM_Reg: EDh]			
Field Name	**Bits**	**Default**	**Description**
Usb_a20_en	0	0b	Set to enable A20Gate from USB OHCI controller in order to enable USB legacy support.
Usb_irq_en	1	0b	Set to enable IRQ1 and 12 from USB OHCI controller in order to enable USB legacy support.
PMIO_ohci_arb_req_q_vld_en	2	0b	Set to open OHCI arbiter req (open OHCI PCI 0x80 [8, 5:4]) and grant fix.
Usb_smi_en	4	0b	Set to enable SMI from OHCI controller in order to enable USB legacy support.
Note: The bits in the register are not used by USB directly; rather they are only used inside ACPI for USB related functions.			

Usb3Cntrl - RW – 8 bits - [PM_Reg: EEh]			
Field Name	**Bits**	**Default**	**Description**
Usb3PowerSel	1:0	00b	00: Usb3 is in S0 power rail. 01: Usb3 is in S3 power rail. 10: Usb3 is in S5 power rail. 11: Usb3 is in S5 power rail.
Usb3RstOnKbRstCf9Dis	2	0b	0: Usb3 can be reset by KbRst# and cf9 reset. 1: Usb3 can not be reset by KbRst# and cf9 reset.
Usb3HcRst	7	0b	Set to1 to put Usb3 host controller into reset state.

UsbEnable – RW – 8 bits – [PM_Reg:EFh]			
Field Name	**Bits**	**Default**	**Description**
USB1 OHCI Enable	0	1b	Enable bit for USB1 OHCI controller (device-18).
USB1 EHCI Enable	1	1b	Enable bit for USB1 EHCI controller (device-18).
USB2 OHCI Enable	2	1b	Enable bit for USB2 OHCI controller (device-19).
USB2 EHCI Enable	3	1b	Enable bit for USB2 EHCI controller (device-19).
USB3 OHCI Enable	4	1b	Enable bit for USB3 OHCI controller (device-22).
USB3 EHCI Enable	5	1b	Enable bit for USB3 EHCI controller (device-22).
USB4 OHCI Enable	6	1b	Enable bit for USB4 OHCI controller (device-20).
Port routing select	7	0b	Port 10 to Port 3 routing select bit 0: Port 10 to Port 3 are routed to USB3 1: Port 10 to Port 3 are routed to XHC
Notes: - Bits 0 and 1 are meaningless if USB3 is enabled. - xHCI Enable is in XHC ACPI MMIO space at ACPI_USB3_Reg: 00h			

UsbControl – RW – 24 bits – [PM_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
UsbPhyS5PwrDwnEnable	0	0b	Set to 1 to power down USB PHY in S4 and S5 state
Reserved	1	0b	
UsbKbResetEnable	2	1b	Set to 1 to enable resetting USB on KB reset.
UsbS5ResetEnable	3	1b	Set to 1 to enable USB reset on S4/S5 resume detection.
Usb11PdResistorEnable	4	1b	Set to 0 to turn off the integrated pull-down resistors on USB_FSD0P/N and USB_FSD1P/N (USB1.1 only ports).
Reserved	5		
Reserved	6	0b	
Reserved	7	1b	
UsbSleepCtrl	10:8	011b	These three bits control the behavior of USB2.0 async packets during CPU C states. Under normal condition, EHCI controller is to poll any new asynchronous activity every 10 microseconds. When these three bits are set, EHCI will alter its polling interval. 000b: standard 10us sleep 001b: wait for 2 microframes 010b: wait for 4 microframes 011b: wait for 6 microframes 100b: wait for next microframe 101b, 110b: reserved 111b: if CPU is in C state and the controller has already exhausted the link list, it can simply stop the asynchronous packets until CPU resumes back to C0 state. In this case, the controller will resume back to its standard mode.
Reserved	11	0b	
Usb2BlGlobalClkGateEn	12	0b	Set to 1 to enable USB 2.0 B-Link Global Clock Gating
Usb2ForceStopClk	13	0b	Set to 1 to enable EHCI/OHCI power saving for B-Link Global Clock Gating when corresponding EHCI/OHCI is disabled.
XHCPD20PhysuspendEn	14	0b	Set to 1 to suspend USB 2.0 PHY when XHC is powered down (if the ports are owned by XHC)
Reserved	15	0b	
Usb3VLoadIsoCtl	16	0b	Controls the value to which isolation cell forces vcontrol_load_n when USB3 is powered down. 0: vcontrol_load_n gated to 1'b0. 1: vcontrol_load_n gated to 1'b1.
UsbTapLatchCtl	17	0b	Controls the time at which the USB controller decodes the target controller id from the tap controller. 0: Command latched after decoding controller id. 1: Command latched before decoding controller id.

UsbControl – RW – 24 bits – [PM_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
Usb3IntPinCtl	18	0b	Controls default value of xhc1 Interrupt Pin register. 0: INTA 1: INTB
Reserved	23:19	00h	Reserved
UsbControl Register			

UsbReset - RW – 8 bits - [PM_Reg: F3h]			
Field Name	**Bits**	**Default**	**Description**
ForceReset2USB	2:0	00h	These are software control bits that can be used to force resetting of USB host controllers. Each bit corresponds to one USB major function.
ForcePHYPwrDown	3	0b	Forces USB PHY into power down mode.
ForcePHYPLLReset	4	0b	Forces USB PHY PLL reset.
ForcePHYDLLreset	5	0b	Forces USB PHY DLL reset.
ForcePHYEarlyReset	6	0b	Forces USB PHY early reset.
ForcePHYPortReset	7	0b	Forces USB PHY port reset.

UsbControl2 - RW – 8 bits - IPM Req: F4h1			
Field Name	**Bits**	**Default**	**Description**
USB_S3_DIS_CON_WO_WAKEEN	0	0	Set to open EHCI/OHCI S3 disconnect and connect fix.
Reserved	7:1	0h	Reserved

GecEn - RW – 8/16 bits - [PM_Reg: F6h]			
Field Name	**Bits**	**Default**	**Description**
GecDisable	0	0b	Set to 1 to disable Gec.
TstGecMiiMode	1	0b	Reserved for testing only.
GecSpiDebugEn	2	0b	If set, this will route the GEC's flash interface directly onto FCH's SPI interface. Note under this scenario, platform should use LPC flash for BIOS so there is no contention between BIOS and the integrated GEC MAC
GecSerialDebugEn	3	0b	If set, this will enable the serial debug port for the integrated GEC
Reserved	4	0b	Reserved
GecManualRst	5	0b	Setting this bit will force the integrated Ethernet MAC to be in reset state.
GecGpioDrvStr	6	0b	Drive strength control for MDCK, MDIO, PHY_RESET#, PHY_PD, and LED0 pins. 0: 4mA 1: 8 mA
GecDrvStrP	10:8	001b	Receiver termination value control in HSTL mode (GecRxRec18 = 1'b1) 000b: Lowest 001b: 011b: 111b: Highest
Reserved	15:13	001b	Reserved.

GecConfig – RW – 8/16/32 bits – [PM_Reg: F8h]			
Field Name	**Bits**	**Default**	**Description**
GecBypassClkSel	0	0b	Set to1 to enable Gec bypass clock.
Reserved	1	0b	
GecTxDrvMode	2	0b	SW should set this bit to 1 to configure the interface to CMOS mode.
GecRxRec33_25	3	1b	Set to 1 if the MAC-PHY is 3.3 or 2.5V. Note bit 3 and 4 must not be set to 1 at the same time. When both bits 3 and 4 are 0, the RX buffer is disabled.
Reserved	4	0b	
GecPwrPolicy	6:5	11b	BIOS should set these two bits according to the platform configuration. These configuration bits are used for internal power-domain-crossing logic. When GEC is powered down, signals from GEC power domain are gated off in the S5 power domain. 00b: GEC is powered down in S3 and S5. 01b: GEC is powered down only in S5. 10b: GEC is powered down only in S3. 11b: GEC is never powered down.
GecShadowRomIntrSel	7	0b	0: Generate SMI# when GEC shadow ROM is updated 1: Generate interrupt to IMC when GEC shadow ROM is updated
GecDrvStrP2	10:8	001b	RGMII output driver drive strength control 000b: Weakest 001b: 011b: 111b: Strongest
Reserved	13	1b	Reserved
GecDev15Func0	14	0b	0: Gec Device=20, Function=6 1: Gec Device=15, Function=0
Reserved	15	0b	Reserved
GecRef	18:16	100b	VREF setting for RX buffers in HSTL mode (GecRxRec18 = 1'b1)

TraceMemoryEn – RW – 8/16/32 bits – [PM_Reg: FCh]			
Field Name	**Bits**	**Default**	**Description**
TraceMemoryEn	0	0b	Set to 1 to enable trace memory decoding
TraceMemoryBaseAddr	31:20	000h	The base address of trace memory. It is 1M memory space.

3.4 Power Management Block 2 (PM2) Registers

PM2 registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from “AcpiMMioAddr” + 0x400 to “AcpiMMioAddr” + 0x4FF.

The base address “AcpiMMioAddr” is defined in PM_reg: 24h, with the default base address at “FED8_0000.”

This register block is used to control 5 Fan Outs and 5 Fan Ins, and to measure 8 voltage inputs and 5 temperarures.

Register Name	Offset Address
Fan0InputControl	00h
Fan0Control	01h
Fan0Freq	02h
LowDuty0	03h
MedDuty0	04h
Multiplier0	05h
LowTemp0Lo	06h
LowTemp0Hi	07h
MedTemp0Lo	08h
MedTemp0Hi	09h
HighTemp0Lo	0Ah
HighTemp0Hi	0Bh
LinearRange0	0Ch
LinearHoldCount0	0Dh
Fan1InputControl	10h
Fan1Control	11h
Fan1Freq	12h
LowDuty1	13h
MedDuty1	14h
Multiplier1	15h
LowTemp1Lo	16h
LowTemp1Hi	17h
MedTemp1Lo	18h
MedTemp1Hi	19h
HighTemp1Lo	1Ah
HighTemp1Hi	1Bh
LinearRange1	1Ch
LinearHoldCount1	1Dh
Fan2InputControl	20h
Fan2Control	21h
Fan2Freq	22h
LowDuty2	23h
MedDuty2	24h
Multiplier2	25h
LowTemp2Lo	26h
LowTemp2Hi	27h
MedTemp2Lo	28h
MedTemp2Hi	29h
HighTemp2Lo	2Ah
HighTemp2Hi	2Bh
LinearRange2	2Ch
LinearHoldCount2	2Dh
FanInputControl3	30h
Fan3Control	31h
Fan3Freq	32h
LowDuty3	33h
MedDuty3	34h
Multiplier3	35h
LowTemp3Lo	36h

Register Name	Offset Address
LowTemp3Hi	37h
MedTemp3Lo	38h
MedTemp3Hi	39h
HighTemp3Lo	3Ah
HighTemp3Hi	3Bh
LinearRange3	3Ch
LinearHoldCount3	3Dh
Fan4InputControl	40h
Fan4Control	41h
Fan4Freq	42h
LowDuty4	43h
MedDuty4	44h
Multiplier4	45h
LowTemp4Lo	46h
LowTemp4Hi	47h
MedTemp4Lo	48h
MedTemp4Hi	49h
HighTemp4Lo	4Ah
HighTemp4Hi	4Bh
LinearRange4	4Ch
LinearHoldCount4	4Dh
FanStatus	60h
FanINTRouteLo	61h
FanINTRouteHi	62h
SampleFreqDiv	63h
FanDebounceCounterLo	64h
FanDebounceCounterHi	65h
Fan0DetectorControl	66h
Fan0SpeedLimitLo	67h
Fan0SpeedLimitHi	68h
Fan0SpeedLo	69h
Fan0SpeedHi	6Ah
Fan1DetectorControl	6Bh
Fan1SpeedLimitLo	6Ch
Fan1SpeedLimitHi	6Dh
Fan1SpeedLo	6Eh
Fan1SpeedHi	6Fh
Fan2DetectorControl	70h
Fan2SpeedLimitLo	71h
Fan2SpeedLimitHi	72h
Fan2SpeedLo	73h
Fan2SpeedHi	74h
Fan3DetectorControl	75h
Fan3SpeedLimitLo	76h
Fan3SpeedLimitHi	77h
Fan3SpeedLo	78h
Fan3SpeedHi	79h
Fan4DetectorControl	7Ah
Fan4SpeedLimitLo	7Bh
Fan4SpeedLimitHi	7Ch
Fan4SpeedLo	7Dh
Fan4SpeedHi	7Eh
TempStatus	90h
TempControl0	91h
TempControl1	92h
TempINTRoute0	93h
TempINTRoute1	94h
IntTempLo	95h
IntTempHi	96h
IntTempLimitLo	97h
IntTempLimitHi	98h
Temp0Lo	99h
Temp0Hi	9Ah
Temp0LimitLo	9Bh
Temp0LimitHi	9Ch

Register Name	Offset Address
Temp1Lo	9Dh
Temp1Hi	9Eh
Temp1LimitLo	9Fh
Temp1LimitHi	A0h
Temp2Lo	A1h
Temp2Hi	A2h
Temp2LimitLo	A3h
Temp2LimitHi	A4h
Temp3Lo	A5h
Temp3Hi	A6h
Temp3LimitLo	A7h
Temp3LimitHi	A8h
IntTempChangeLimit	ABh
Temp0ChangeLimit	ACh
Temp1ChangeLimit	ADh
Temp2ChangeLimit	AEh
Temp3ChangeLimit	AFh
VoltageStatus	B0h
VoltageControl0	B2h
VoltageControl1	B3h
VoltageINTRout0	B5h
VoltageINTRout1	B6h
Voltage0Lo	B8h
Voltage0Hi	B9h
Voltage0LimitLo	BAh
Voltage0LimitHi	BBh
Voltage1Lo	BCh
Voltage1Hi	BDh
Voltage1LimitLo	BEh
Voltage1LimitHi	BFh
Voltage2Lo	C0h
Voltage2Hi	C1h
Voltage2LimitLo	C2h
Voltage2LimitHi	C3h
Voltage3Lo	C4h
Voltage3Hi	C5h
Voltage3LimitLo	C6h
Voltage3LimitHi	C7h
Voltage4Lo	C8h
Voltage4Hi	C9h
Voltage4LimitLo	CAh
Voltage4LimitHi	CBh
Voltage5Lo	CCh
Voltage5Hi	CDh
Voltage5LimitLo	CEh
Voltage5LimitHi	CFh
Voltage6Lo	D0h
Voltage6Hi	D1h
Voltage6LimitLo	D2h
Voltage6LimitHi	D3h
Voltage7Lo	D4h
Voltage7Hi	D5h
Voltage7LimitLo	D6h
Voltage7LimitHi	D7h
AnalogIoRstSel	DDh
TempRstSel	DFh
AlertThermaltripStatus	E0h
AlertLimitLo	E1h
AlertLimitHi	E2h
ThermalTripLimitLo	E3h
ThermalTripLimitHi	E4h
AlertThermaltripControl	E5h
HwmControl	E6h
VoltageReadFreq	E7h

Register Name	Offset Address
TempReadFreq	E8h
VoltageReadAverage	E9h
Hwm_VoltCalib	EAh
TempReadAverage	EBh
HwmStatus	ECh
VoltageReadStatus	EDh
TempReadStatus	EEh
HwmClkControl	EFh
ADC_PDBTime	F0h
ADC_StartUp	F1h
ADC_Delay	F2h
SAX_CTL_VTime	F3h
SAX_CTL_TTime	F4h
BGADJ	F5h
AFEcfg_Clkdiv	F6h
Hwm_DebugSel	F7h
VoltageSampleSel	F8h
TempSampleSel	F9h
HwmVoltage_div0	FAh
HwmVoltage_div1	FBh
Adc_Gain_Adj	FCh
Adc_cfg	FDh
Test_cntl	FEh
HwmMiscControl	FFh

Fan0InputControl - RW – 8 bits - [PM2_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut0 is enabled and temperature input is from internal diode. 001: FanOut0 is enabled and temperature input is from Temp0. 010: FanOut0 is enabled and temperature input is from Temp1. 011: FanOut0 is enabled and temperature input is from Temp2. 100: FanOut0 is enabled and temperature input is from Temp3. 101: FanOut0 is enabled and temperature input is from Temp0. Internal noise filtering algorithm is applied to Temp0. 110: FanOut0 is enabled and temperature input is 0. 111: FanOut0 is disabled.

Notes:

When the fan control is not in AutoMode, the active fan duty cycle is set by LowDuty register.

When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function.

(a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duly cycle.

(b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below:

When Actual Temperature < LowTemp,

DutyCycle = 0

When Actual Temperature > LowTemp and Actual Temperature < MedTemp;

DutyCycle = LowDuty

When Actual Temperature > MedTemp and Actual Temperature < HighTemp

DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty

When Actual Temperature > HighTemp

DutyCycle = max or 100%

In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.

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Fan0Control - RW – 8 bits - [PM2_Reg: 01h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut0 controlled by the temperature input; controlled by LowDuty0 otherwise.
LinearMode	1	0b	0: Use step function. 1: Use Linear function.
FanPolarity	2	0b	0: FanOut0 drives low. 1: FanOut0 drives high.
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under Linear mode.

Fan0Freq - RW – 8 bits - [PM2_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
FanFreq	7:0	00h	FanOut0 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7: Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally, 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz

LowDuty0 - RW – 8 bits - [PM2_Reg: 03h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	Fan0 Duty number when temperature is more than lowTemp0 and lower than MedTemp0. There are 256 time slots in one Fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

MedDuty0 - RW – 8 bits - [PM2_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	Fan0 Duty number when temperature is more than MedTemp0 and lower than HighTemp0. There are 256 time slots in one Fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot0 ~ slotN, and stops from slot(N+1) ~ slot255. 00: Always stop … FF: Full speed run

Multiplier0 - RW – 8 bits - [PM2_Reg: 05h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when Fan0 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp0Lo – RW – 8 bits - [PM2_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp0[7:0]. Lower bits of low temperature threshold.

LowTemp0Hi - RW – 8 bits - [PM2_Reg: 07h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp0[15:8]. Higher bits of low temperature threshold.

MedTemp0Lo - RW – 8 bits - [PM2_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp0[7:0]. Lower bits of medium temperature threshold.

MedTemp0Hi - RW – 8 bits - [PM2_Reg: 09h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp0[15:8]. Higher bits of medium temperature threshold.

HighTemp0Lo - RW – 8 bits - [PM2_Reg: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp0[7:0]. Lower bits of high temperature threshold.

HighTemp0Hi - RW – 8 bits - [PM2_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp0[15:8]. Higher bits of high temperature threshold.

LinearRange0 - RW – 8 bits - [PM2_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that Fan0 can tolerate. Fan0 will not be affected if temperature varies within this range.

LinearHoldCount0 - RW – 8 bits - [PM2_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan cycle to be waited before duty cycle can be changed.

Fan1InputControl - RW – 8 bits - [PM2_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut1 is enabled and temperature input is from Internal diode. 001: FanOut1 is enabled and temperature input is from Temp0. 010: FanOut1 is enabled and temperature input is from Temp1. 011: FanOut1 is enabled and temperature input is from Temp2. 100: FanOut1 is enabled and temperature input is from Temp3. 101: FanOut1 is disabled. 110: FanOut1 is enabled and temperature input is 0. 111: FanOut1 is disabled.

Notes:

When the fan control is not in AutoMode the active fan duty cycle is set by LowDuty register.

When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function.

(a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duty cycle.

(b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below:

When Actual Temperature < LowTemp,

DutyCycle = 0

When Actual Temperature > LowTemp and Actual Temperature < MedTemp;

DutyCycle = LowDuty

When Actual Temperature > MedTemp and Actual Temperature < HighTemp

DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty

When Actual Temperature > HighTemp

DutyCycle = max or 100%

In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.

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Fan1Control - RW – 8 bits - [PM2_Reg: 11h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut1 controlled by the temperature input; controlled by LowDuty1 otherwise.
LinearMode	1	0b	0: Use step function. 1: Use Linear function.
FanPolarity	2	0b	0: FanOut1 drives low. 1: FanOut1 drives high.
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under Linear mode.

Fan1Freq - RW – 8 bits - [PM2_Reg: 12h]			
Field Name	**Bits**	**Default**	**Description**
FanFreq	7:0	00h	FanOut1 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7 Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz.

LowDuty1 - RW – 8 bits - [PM2_Reg: 13h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	Fan0 Duty number when temperature is more than lowTemp1 and lower than MedTemp0. There are 256 time slots in one Fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop .. FF: Full speed run

MedDuty1 - RW – 8 bits - [PM2_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	Fan0 Duty number when temperature is more than MedTemp0 and lower than HighTemp1. There are 256 time slots in one Fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

Multiplier1 - RW – 8 bits - [PM2_Reg: 15h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when FanOut1 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp1Lo – RW – 8 bits - [PM2_Reg: 16h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp1[7:0]. Lower bits of low temperature threshold.

LowTemp1Hi - RW – 8 bits - [PM2_Reg: 17h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp1[15:8]. Higher bits of low temperature threshold.

MedTemp1Lo - RW – 8 bits - [PM2_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp1[7:0]. Lower bits of medium temperature threshold.

MedTemp1Hi - RW – 8 bits - [PM2_Reg: 19h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp1[15:8]. Higher bits of medium temperature threshold.

HighTemp1Lo - RW – 8 bits - [PM2_Reg: 1Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp1[7:0]. Lower bits of high temperature threshold.

HighTemp1Hi - RW – 8 bits - [PM2_Reg: 1Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp1[15:8]. Higher bits of high temperature threshold.

LinearRange1 - RW – 8 bits - [PM2_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that FanOut1 can tolerate. FanOut1 will not be affected if temperature varies within this range.

LinearHoldCount1 - RW – 8 bits - [PM2_Reg: 1Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan Cycle to be waited before duty cycle can be changed.

Fan2InputControl - RW – 8 bits - [PM2_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut2 is enabled and temperature input is from Internal diode 001: FanOut2 is enabled and temperature input is from Temp0. 010: FanOut2 is enabled and temperature input is from Temp1. 011: FanOut2 is enabled and temperature input is from Temp2. 100: FanOut2 is enabled and temperature input is from Temp3. 101: FanOut2 is disabled. 110: FanOut2 is enabled and temperature input is 0. 111: FanOut2 is disabled.

Notes:

When the fan control is not in AutoMode, the active fan duty cycle is set by LowDuty register.

When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function.

(a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duty cycle.

(b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below:

When Actual Temperature < LowTemp,

DutyCycle = 0

When Actual Temperature > LowTemp and Actual Temperature < MedTemp;

DutyCycle = LowDuty

When Actual Temperature > MedTemp and Actual Temperature < HighTemp

DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty

When Actual Temperature > HighTemp

DutyCycle = max or 100%

In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.

Fan2Control - RW – 8 bits - [PM2_Reg: 21h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut2 controlled by the temperature input; controlled by LowDuty2 otherwise.
LinearMode	1	0b	0: Use step function 1: Use Linear function
FanPolarity	2	0b	0: FanOut2 drives low 1: FanOut2 drives high
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under Linear mode.

Fan2Freq - RW – 8 bits - [PM2_Reg: 22h]			
Field Name	**Bits**	**Default**	**Description**
FanFreq	7:0	00h	FanOut2 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7: Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz

LowDuty2 - RW – 8 bits - [PM2_Reg: 23h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	Fan0 Duty number when temperature is more than lowTemp2 and lower than MedTemp2. There are 256 time slots in one fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

MedDuty2 - RW – 8 bits - [PM2_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	FanOut2 Duty number when temperature is more than MedTemp2 and lower than HighTemp2. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

Multiplier2 - RW – 8 bits - [PM2_Reg: 25h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when FanOut2 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp2Lo – RW – 8 bits - [PM2_Reg: 26h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp2[7:0]. Lower bits of low temperature threshold.

LowTemp2Hi - RW – 8 bits - [PM2_Reg: 27h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp2[15:8]. Higher bits of low temperature threshold.

MedTemp2Lo - RW – 8 bits - [PM2_Reg: 28h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp2[7:0]. Lower bits of medium temperature threshold.

MedTemp2Hi - RW – 8 bits - [PM2_Reg: 29h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp2[15:8]. Higher bits of medium temperature threshold.

HighTemp2Lo - RW – 8 bits - [PM2_Reg: 2Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp2[7:0]. Lower bits of high temperature threshold.

HighTemp2Hi - RW – 8 bits - [PM2_Reg: 2Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp2[15:8]. Higher bits of high temperature threshold.

LinearRange2 - RW – 8 bits - [PM2_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that FanOut2 can tolerate. FanOut2 will not be affected if temperature varies within this range.

LinearHoldCount2 - RW – 8 bits - [PM2_Reg: 2Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan Cycle to be waited before duty cycle can be changed.

Fan3InputControl - RW – 8 bits - [PM2_Reg: 30h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut3 is enabled and temperature input is from Internal diode. 001: FanOut3 is enabled and temperature input is from Temp0. 010: FanOut3 is enabled and temperature input is from Temp1. 011: FanOut3 is enabled and temperature input is from Temp2. 100: FanOut3 is enabled and temperature input is from Temp3. 101: FanOut3 is disabled. 110: FanOut3 is enabled and temperature input is 0. 111: FanOut3 is disabled.

Notes:

When the fan control is not in AutoMode, the active fan duty cycle is set by LowDuty register.

When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function.

(a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duty cycle.

(b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below:

When Actual Temperature < LowTemp,

DutyCycle = 0

When Actual Temperature > LowTemp and Actual Temperature < MedTemp;

DutyCycle = LowDuty

When Actual Temperature > MedTemp and Actual Temperature < HighTemp

DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty

When Actual Temperature > HighTemp

DutyCycle = max or 100%

In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.

Fan3Control - RW – 8 bits - [PM2_Reg: 31h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut3 controlled by the temperature input; controlled by LowDuty3 otherwise.
LinearMode	1	0b	0: Use step function 1: Use linear function
FanPolarity	2	0b	0: FanOut3 drives low 1: FanOut3 drives high
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under Linear mode.

Fan3Freq - RW – 8 bits - [PM2_Reg: 32h]			
Field Name	**Bits**	**Default**	Description
FanFreq	7:0	00h	FanOut3 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7: Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz

LowDuty3 - RW – 8 bits - [PM2_Reg: 33h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	FanOut3 Duty number when temperature is more than lowTemp2 and lower than MedTemp2. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop ... FF: Full speed run

MedDuty3 - RW – 8 bits - [PM2_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	FanOut3 Duty number when temperature is more than MedTemp3 and lower than HighTemp3. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

Multiplier3 - RW – 8 bits - [PM2_Reg: 35h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when FanOut3 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp3Lo – RW – 8 bits - [PM2_Reg: 36h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp3[7:0]. Lower bits of low temperature threshold.

LowTemp3Hi - RW – 8 bits - [PM2_Reg: 37h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp3[15:8]. Higher bits of low temperature threshold.

MedTemp3Lo - RW – 8 bits - [PM2_Reg: 38h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp3[7:0]. Lower bits of medium temperature threshold.

MedTemp3Hi - RW – 8 bits - [PM2_Reg: 39h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp3[15:8]. Higher bits of medium temperature threshold.

HighTemp3Lo - RW – 8 bits - [PM2_Reg: 3Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp3[7:0]. Lower bits of high temperature threshold.

HighTemp3Hi - RW – 8 bits - [PM2_Reg: 3Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp3[15:8]. Higher bits of high temperature threshold.

LinearRange3 - RW – 8 bits - [PM2_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that FanOut3 can tolerate. FanOut3 will not be affected if temperature varies within this range.

LinearHoldCount3 - RW – 8 bits - [PM2_Reg: 3Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan Cycle to be waited before duty cycle can be changed.

Fan4InputControl - RW – 8 bits - [PM2_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut4 is enabled and temperature input is from Internal diode. 001: FanOut4 is enabled and temperature input is from Temp0. 010: FanOut4 is enabled and temperature input is from Temp1. 011: FanOut4 is enabled and temperature input is from Temp2. 100: FanOut4 is enabled and temperature input is from Temp3. 101: FanOut4 is disabled. 110: FanOut4 is enabled and temperature input is 0. 111: FanOut4 is disabled.

Notes:

When the fan control in not in AutoMode, the active fan duty cycle is set by LowDuty register.

When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function.

(a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duty cycle.

(b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below:

When Actual Temperature < LowTemp,

DutyCycle = 0

When Actual Temperature > LowTemp and Actual Temperature < MedTemp;

DutyCycle = LowDuty

When Actual Temperature > MedTemp and Actual Temperature < HighTemp

DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty

When Actual Temperature > HighTemp

DutyCycle = max or 100%

In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.

Fan4Control - RW – 8 bits - [PM2_Reg: 41h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut4 controlled by the temperature input; controlled by LowDuty4 otherwise.
LinearMode	1	0b	0: Use step function 1: Use linear function
FanPolarity	2	0b	0: FanOut4 drives low 1: FanOut4 drives high
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under linear mode.

Fan4Freq - RW – 8 bits - [PM2_Reg: 42h]			
Field Name	**Bits**	**Default**	**Description**
FanFreq	7:0	00h	FanOut4 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7 Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz.

LowDuty4 - RW – 8 bits - [PM2_Reg: 43h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	FanOut4 Duty number when temperature is more than lowTemp4 and lower than MedTemp4. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop. … FF: Full speed run.

MedDuty4 - RW – 8 bits - [PM2_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	FanOut4 Duty number when temperature is more than MedTemp4 and lower than HighTemp4. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

Multiplier4 - RW – 8 bits - [PM2_Reg: 45h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when FanOut4 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp4Lo – RW – 8 bits - [PM2_Reg: 46h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp4[7:0]. Lower bits of low temperature threshold.

LowTemp4Hi - RW – 8 bits - [PM2_Reg: 47h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp4[15:8]. Higher bits of low temperature threshold.

MedTemp4Lo – RW – 8 bits - [PM2_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp4[7:0]. Lower bits of medium temperature threshold.

MedTemp4Hi - RW – 8 bits - [PM2_Reg: 49h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp4[15:8]. Higher bits of medium temperature threshold.

HighTemp4Lo - RW – 8 bits - [PM2_Reg: 4Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp4[7:0]. Lower bits of high temperature threshold.

HighTemp4Hi - RW – 8 bits - [PM2_Reg: 4Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp4[15:8]. Higher bits of high temperature threshold.

LinearRange4 - RW – 8 bits - [PM2_Reg: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that FanOut4 can tolerate. FanOut4 will not be affected if temperature varies within this range.

LinearHoldCount4 - RW – 8 bits - [PM2_Reg: 4Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan Cycle to be waited before duty cycle can be changed.

FanStatus – RW - [PM2_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
Fan0SpeedTooSlow	0	0b	Indicates whether Fan0 runs slower than the value in the Fan0SpeedLimit. Write to 1 to clear.
Fan1SpeedTooSlow	1	0b	Indicates whether Fan1 runs slower than the value in the Fan1SpeedLimit. Write to 1 to clear.
Fan2SpeedTooSlow	2	0b	Indicates whether Fan2 runs slower than the value in the Fan2SpeedLimit.Write to 1 to clear.
Fan3SpeedTooSlow	3	0b	Indicates whether Fan3 runs slower than the value in the Fan3SpeedLimit. Write to 1 to clear.
Fan4SpeedTooSlow	4	0b	Indicates whether Fan4 runs slower than the value in the Fan4SpeedLimit. Write to 1 to clear.
Reserved	7:5	000b	Reserved

FanINTRouteLo - RW – 8 bits - [PM2_Reg: 61h]			
Field Name	**Bits**	**Default**	**Description**
Fan0INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: No SCI/SMI generated
Fan1INTRoute	3:2	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: No SCI/SMI generated
Fan2INTRoute	5:4	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: No SCI/SMI generated
Fan3INTRoute	7:6	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: No SCI/SMI generated

FanINTRouteHi - RW – 8 bits - [PM2_Reg: 62h]			
Field Name	**Bits**	**Default**	**Description**
Fan4INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: No SCI/SMI generated
Reserved	7:2	000000b	

SampleFreqDiv – RW – 8 bits - [PM2_Reg: 63h]			
Field Name	**Bits**	**Default**	**Description**
SampleFreqDiv	1:0	00b	These bits determine the sampling rate of Fan Speed. 00: Base(22.5KHz) 01: Base(22.5KHz)/2 10: Base(22.5KHz)/4 11: Base(22.5KHz)/8
Reserved	7:2	000000b	Reserved

FanDebounceCounterLo - RW – 8 bits - [PM2_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
FanDebounceCounterLo	7:0	00h	Specify low 8 bits of the debounced counter when measuring Fan Speed

FanDebounceCounterHi - RW – 8 bits - [PM2_Reg: 65h]			
Field Name	**Bits**	**Default**	**Description**
FanDebounceCounterHi	7:0	00h	Specify high 8 bits of the debounced counter when measuring Fan Speed

Fan0DetectorControl- RW – 8 bits - [PM2_Reg: 66h]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan0 speed measurement 1: Enable Fan0 speed measurement
UseAverage	1	0b	0: Not to average Fan0 speed 1: Average Fan0 speed
Reserved	3:2	00b	Reserved
ShutDownEnable	4	00b	If set to, the machine can be shutdown if the Fan0 Status remains for more than 4 seconds.
Reserved	7:5		Reserved

Fan0SpeedLimitLo- RW – 8 bits - [PM2_Reg: 67h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan0SpeedLimit to set threshold when Fan0 speed is below it.

Fan0SpeedLimitHi- RW – 8 bits - [PM2_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan0SpeedLimit to set threshold when Fan0 speed is below it.

Fan0SpeedLo- R – 8 bits - [PM2_Reg: 69h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:1	00h	Fan0Speed [7:0]

Fan0SpeedHi- R – 8 bits - [PM2_Reg: 6Ah]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:0	00h	Fan0Speed[15:8]

Fan1DetectorControl- RW – 8 bits - [PM2_Reg: 6Bh]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan1 speed measurement 1: Enable Fan1 speed measurement
UseAverage	1	0b	0: Not to average Fan1 speed 1: Average Fan1 speed
Reserved	3:2	00b	Reserved
ShutDownEnable	4	00b	If set to 1, the machine can be shutdown if the Fan1 Status remains for more than 4 seconds.
Reserved	7:5		Reserved

Fan1SpeedLimitLo- RW – 8 bits - [PM2_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan1SpeedLimit to set threshold when Fan1 speed is below it.

Fan1SpeedLimitHi- RW – 8 bits - [PM2_Reg: 6Dh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan1SpeedLimit to set threshold when Fan1 speed is below it.

Fan1SpeedLo- R – 8 bits - [PM2_Reg: 6Eh]			
Field Name	**Bits**	**Default**	**Description**
Fan1Speed	7:1	00h	Fan1Speed[7:0]

Fan1SpeedHi- R – 8 bits - [PM2_Reg: 6Fh]			
Field Name	**Bits**	**Default**	**Description**
Fan1Speed	7:0	00h	Fan1Speed[15:8]

Fan1Speed register contains the actual Fan1 speed reading. The Fan1 speed is read from two 8-bit registers (High byte and Low byte). To read the correct value of the Fan1 speed, the following algorithm should be used:

[Note: Similar algorithm applies to Fan2Speed (PM_Reg:73h/74h), Fan3Speed (PM_Reg:78h/79h) and Fan4Speed (PM_Reg:7Dh/7Eh) registers further down]

FAN1Speed1 = 1st reading, FAN1Speed2 = 2nd reading, FAN1Speed3 = 3rd reading

If (FAN1Speed1 == FAN1Speed2) || If (FAN1Speed2 == FAN1Speed3)

FAN1Speed = FAN1Speed2

Else

FAN1Speed = FAN1Speed1

Where FAN1Speed1, FAN1Speed2. FAN1Speed3 = 16 bit Fan1 speed reading (Fan1SpeedHi, Fan1SpeedLo)

FAN1Speed = final 16-bit Fan1 speed reading

Fan2DetectorControl- RW – 8 bits - [PM2_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan2 speed measurement 1: Enable Fan2 speed measurement
UseAverage	1	0b	0: Not to average Fan2 speed 1: Average Fan2 speed
Reserved	3:2	00b	
ShutDownEnable	4	00b	If set to, the machine can be shutdown if the Fan2 Status remains for more than 4 seconds.
Reserved	7:5		Reserved

Fan2SpeedLimitLo- RW – 8 bits - [PM2_Reg: 71h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan2SpeedLimit to set threshold when Fan2 speed is below it.

Fan2SpeedLimitHi- RW – 8 bits - [PM2_Reg: 72h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan2SpeedLimit to set threshold when Fan2 speed is below it.

Fan2SpeedLo- R – 8 bits - [PM2_Reg: 73h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:1	00h	Fan2Speed[7:0]

Fan2SpeedHi- R – 8 bits - [PM2_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:0	00h	Fan2Speed[15:8]

Fan3DetectorControl- RW – 8 bits - [PM2_Reg: 75h]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan3 speed measurement 1: Enable Fan3 speed measurement
UseAverage	1	0b	0: Not to average Fan3 speed 1: Average Fan3 speed
Reserved	3:2	00b	
ShutDownEnable	4	00b	If set to, the machine can be shutdown if the Fan3 Status remains for more than 4 seconds.
Reserved	7:5	-	

Fan3SpeedLimitLo- RW – 8 bits - [PM2_Reg: 76h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan3SpeedLimit to set threshold when Fan3 speed is below it.

Fan3SpeedLimitHi- RW – 8 bits - [PM2_Reg: 77h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan3SpeedLimit to set threshold when Fan3 speed is below it.

Fan3SpeedLo- R – 8 bits - [PM2_Reg: 78h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:1	00h	Fan3Speed[7:0]

Fan3SpeedHi- R – 8 bits - [PM2_Reg: 79h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:0	00h	Fan3Speed[15:8]

Fan4DetectorControl- RW – 8 bits - [PM2_Reg: 7Ah]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan4 speed measurement 1: Enable Fan4 speed measurement
UseAverage	1	0b	0: Not to average Fan4 speed 1: Average Fan4 speed
Reserved	3:2	00b	Reserved
ShutDownEnable	4	00b	If set to, the machine can be shutdown if the Fan4 Status remains for more than 4 seconds.
Reserved	7:5	-	Reserved

Fan4SpeedLimitLo- RW – 8 bits - [PM2_Reg: 7Bh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan4SpeedLimit to set threshold when Fan4 speed is below it.

Fan4SpeedLimitHi- RW – 8 bits - [PM2_Reg: 7Ch]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan4SpeedLimit to set threshold when Fan4 speed is below it.

Fan4SpeedLo- R – 8 bits - [PM2_Reg: 7Dh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:1	00h	Fan4Speed[7:0]

Fan4SpeedHi- R – 8 bits - [PM2_Reg: 7Eh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:0	00h	Fan4Speed[15:8]

TempStatus – RW - [PM2_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
IntTempStatus	0	0b	Indicate whether internal Temp is out of the limit. Write to 1 to clear.
Temp0Status	1	0b	Indicate whether Temp0 is out of the limit. Write to 1 to clear.
Temp1Status	2	0b	Indicate whether Temp1 is out of the limit. Write to 1 to clear.
Temp2Status	3	0b	Indicate whether Temp2 is out of the limit. Write to 1 to clear.
Temp3Status	4	0b	Indicate whether Temp3 is out of the limit. Write to 1 to clear.
Reserved	7:5	000b	Reserved

TempControl0- RW – 8 bits - [PM2_Reg: 91h]			
Field Name	**Bits**	**Default**	**Description**
IntTempControl	1:0	00b	Values other than 00 indicate that IntTemp sensor is enabled. 00: Disable 01: Set IntTempStatus to 1 if IntTemp is higher than IntTempLimit. 10: Set IntTempStatus to 1 if IntTemp is lower than IntTempLimit. 11: Set IntTempStatus to 1 if IntTempHi is higher than IntTempLimitLo or lower than IntTempLimitHi.
Temp0Control	3:2	00b	TEMPIN0 sensor is enabled if Temp0Source is 0 and Temp0Control is not 00b. 00: TEMPIN0 sensor disabled if Temp0Source is 0. 01: Set Temp0Status to 1 if Temp0 is higher than Temp0Limit 10: Set Temp0Status to 1 if Temp0 is lower than Temp0Limit. 11: Set Temp0Status to 1 if Temp0Hi is higher than Temp0LimitLo or lower than Temp0LimitHi.
Temp1Control	5:4	00b	Values other than 00 indicate that Temp1 sensor is enabled. 00: Disable 01: Set Temp1Status to 1 if Temp1 is higher than Temp1Limit 10: Set Temp1Status to 1 if Temp1 is lower than Temp1Limit. 11: Set Temp1Status to 1 if Temp1Hi is higher than Temp1LimitLo or lower than Temp1LimitHi.
Temp2Control	7:6	00b	Values other than 00 indicate that Temp2 sensor is enabled. 00: Disable 01: Set Temp2Status to 1 if Temp2 is higher than Temp2Limit 10: Set Temp2Status to 1 if Temp2 is lower than Temp2Limit. 11: Set Temp2Status to 1 if Temp2Hi is higher than Temp2LimitLo or lower than Temp2LimitHi.

TempControl1- RW – 8 bits - [PM2_Reg: 92h]			
Field Name	**Bits**	**Default**	Description
Temp3Control	1:0	00b	Values other than 00 indicate that Temp3 sensor is enabled. 00: Disable 01: Monitor current temperature more than Temp3Limit 10: Monitor current temperature Lower than Temp3Limit 11: Monitor current temperature more than Temp3Limit[7:0] or Lower than Temp3Limit[15:8]
Reserved	2	0b	Reserved
Temp0Source	3	0b	Bit selects source for Temp0 reading. 0: TEMPIN0 temperature sensor input 1: SMBUS auto-polling value
Reserved	7:4	0000b	Reserved

TempINTRoute0 - RW – 8 bits - [PM2_Reg: 93h]			
Field Name	**Bits**	**Default**	**Description**
IntTempINTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Temp0INTRoute	3:2	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Temp1INTRoute	5:4	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Temp2INTRoute	7:6	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated

TempINTRoute1 - RW – 8 bits - [PM2_Reg: 94h]			
Field Name	**Bits**	**Default**	**Description**
Temp3INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Reserved	7:2	000000b	Reserved

IntTempLo- R – 8 bits - [PM2_Reg: 95h]			
Field Name	**Bits**	**Default**	**Description**
IntTempLo	7:0	00h	IntTemp[7:0]

IntTempHi- R – 8 bits - [PM2_Reg: 96h]			
Field Name	**Bits**	**Default**	**Description**
IntTempHi	7:0	00h	IntTemp[15:8]

IntTempLimitLo- RW – 8 bits - [PM2_Reg: 97h]			
Field Name	**Bits**	**Default**	**Description**
IntTempLimitLo	7:0	00h	IntTempLimit[7:0]

IntTempLimitHi- RW – 8 bits - [PM2_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
IntTempLimitHi	7:0	00h	IntTempLimit[15:8]

Temp0Lo- R/W – 8 bits - [PM2_Reg: 99h]			
Field Name	**Bits**	**Default**	Description
TempLo	7:0	00h	Temp0[7:0]. Register is writeable when Fan0InputControl[Fan0] = 3'b101.

Temp0Hi- R/W – 8 bits - [PM2_Reg: 9Ah]			
Field Name	**Bits**	**Default**	Description
TempHi	7:0	00h	Temp0[15:8]. Register is writeable when Fan0InputControl[Fan0] = 3'b101.

Temp0LimitLo- RW – 8 bits - [PM2_Reg: 9Bh]			
Field Name	**Bits**	**Default**	**Description**
Temp0LimitLo	7:0	00h	Temp0Limit[7:0]

Temp0LimitHi- RW – 8 bits - [PM2_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
Temp0LimitHi	7:0	00h	Temp0Limit[15:8]

Temp1Lo- R – 8 bits - [PM2_Reg: 9Dh]			
Field Name	**Bits**	**Default**	**Description**
Temp1Lo	7:0	00h	Temp1[7:0]

Temp1Hi- R – 8 bits - [PM2_Reg: 9Eh]			
Field Name	**Bits**	**Default**	**Description**
Temp1Hi	7:0	00h	Temp1[15:8]

Temp1LimitLo- RW – 8 bits - [PM2_Reg: 9Fh]			
Field Name	**Bits**	**Default**	**Description**
Temp1LimitLo	7:0	00h	Temp1Limit[7:0]

Temp1LimitHi- RW – 8 bits - [PM2_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
Temp1LimitHi	7:0	00h	Temp1Limit[15:8]

Temp2Lo- R – 8 bits - [PM2_Reg: A1h]			
Field Name	**Bits**	**Default**	**Description**
Temp2Lo	7:0	00h	Temp2[7:0]

Temp2Hi- R – 8 bits - [PM2_Reg: A2h]			
Field Name	**Bits**	**Default**	**Description**
Temp2Hi	7:0	00h	Temp2[15:8]

Temp2LimitLo- RW – 8 bits - [PM2_Reg: A3h]			
Field Name	**Bits**	**Default**	**Description**
Temp2LimitLo	7:0	00h	Temp2Limit[7:0]

Temp2LimitHi- RW – 8 bits - [PM2_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
Temp2LimitHi	7:0	00h	Temp2Limit[15:8]

Temp3Lo- R – 8 bits - [PM2_Reg: A5h]			
Field Name	**Bits**	**Default**	**Description**
Temp3Lo	7:0	00h	Temp3[7:0]

Temp3Hi- R – 8 bits - [PM2_Reg: A6h]			
Field Name	**Bits**	**Default**	**Description**
Temp3Hi	7:0	00h	Temp3[15:8]

Temp3LimitLo- RW – 8 bits - [PM2_Reg: A7h]			
Field Name	**Bits**	**Default**	**Description**
Temp3LimitLo	7:0	00h	Temp3Limit[7:0]

Temp3LimitHi- RW – 8 bits - [PM2_Reg: A8h]			
Field Name	**Bits**	**Default**	**Description**
Temp3LimitHi	7:0	00h	Temp3Limit[15:8]

IntTempChangeLimit- R/W – 8 bits - [PM2_Reg: ABh]			
Field Name	**Bits**	**Default**	Description
TempChangeLimit	7:0	00h	Filtering is applied to {IntTempHi, IntTempLo} if TempChangeLimit is nonzero.

Notes:

When Temp(new) > Temp(old) + [TempChangeLimit << 6]

Temp = Temp(old) + [TempChangeLimit << 6]

When Temp(new) < Temp(old) – [TempChangeLimit << 6]

Temp = Temp(old) – [TempChangeLimit << 6]

When Temp(new) <= Temp(old) + [TempChangeLimit << 6] and >= Temp(old) – [TempChangeLimit << 6]

Temp = Temp(new)

Temp0ChangeLimit- R/W – 8 bits - [PM2_Reg: ACh]			
Field Name	**Bits**	**Default**	Description
Temp0ChangeLimit	7:0	00h	Filtering is applied to {Temp0Hi, Temp0Lo} if TempChangeLimit is nonzero.

Temp1ChangeLimit- R/W – 8 bits - [PM2_Reg: ADh]			
Field Name	**Bits**	**Default**	Description
Temp1ChangeLimit	7:0	00h	Filtering is applied to {Temp1Hi, Temp1Lo} if TempChangeLimit is nonzero.

Temp2ChangeLimit- R/W – 8 bits - [PM2_Reg: AEh]			
Field Name	**Bits**	**Default**	Description
Temp2ChangeLimit	7:0	00h	Filtering is applied to {Temp2Hi, Temp2Lo} if TempChangeLimit is nonzero.

Temp3ChangeLimit- R/W – 8 bits - [PM2_Reg: AFh]			
Field Name	**Bits**	**Default**	Description
Temp3ChangeLimit	7:0	00h	Filtering is applied to {Temp3Hi, Temp3Lo} if TempChangeLimit is nonzero.

VoltageStatus- R – 8 bits - [PM2_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0Status	0	0b	1 means that Vin0 is out of VoltageLimit0
Voltage1Status	1	0b	1 means that Vin1 is out of VoltageLimit1
Voltage2Status	2	0b	1 means that Vin2 is out of VoltageLimit2
Voltage3Status	3	0b	1 means that Vin3 is out of VoltageLimit3
Voltage4Status	4	0b	1 means that Vin4 is out of VoltageLimit4
Voltage5Status	5	0b	1 means that Vin5 is out of VoltageLimit5
Voltage6Status	6	0b	1 means that Vin6 is out of VoltageLimit6
Voltage7Status	7	0b	1 means that Vin7 is out of VoltageLimit7

VoltageControl0- RW – 8 bits - [PM2_Reg: B2h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0Control	1:0	00b	Values other than 00 indicate that Voltage0 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 5Ah and 59h) against Voltage0Limit (combined value from registers 5Ch and 5Bh); set Voltage0Status bit if is greater than Voltage0Limit 10: Monitor current value (combined value from registers 5Ah and 59h) against Voltage0Limit (combined value from registers 5Ch and 5Bh); set Voltage0Status bit if it is lower than Voltage0Limit 11: Monitor Voltage0Hi against the limits. Set Voltage0Status when it is more than Voltage0LimitLo [7:0] or Lower than Voltage0LimitHi [15:8]
Voltage1Control	3:2	00b	Values other than 00 indicate that Voltage1 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 5Eh and 5Dh) against Voltage1Limit (combined value from registers 60h and 5Fh); set Voltage1Status bit if is greater than Voltage1Limit 10: Monitor current value (combined value from registers 5Eh and 5Dh) against Voltage1Limit (combined value from registers 60h and 5Fh); set Voltage1Status bit if it is lower than Voltage1Limit 11: Monitor Voltage1Hi against the limits. Set Voltage1 Status when it is more than Voltage1LimitLo [7:0] or Lower than Voltage1LimitHi [15:8]
Voltage2Control	5:4	00b	Values other than 00 indicate that Voltage2 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 62h and 61h) against Voltage2Limit (combined value from registers 64h and 63h); set Voltage2Status bit if is greater than Voltage2Limit 10: Monitor current value (combined value from registers 62h and 61h) against Voltage2Limit (combined value from registers 64h and 63h); set Voltage2Status bit if it is lower than Voltage2Limit 11: Monitor Voltage2Hi against the limits. Set Voltage2Status when it is more than Voltage2LimitLo [7:0] or Lower than Voltage2LimitHi [15:8]

VoltageControl0- RW – 8 bits - [PM2_Reg: B2h]			
Field Name	**Bits**	**Default**	**Description**
Voltage3Control	7:6	00b	Values other than 00 indicate that Voltage3 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 66h and 65h) against Voltage3Limit (combined value from registers 68h and 67h); set Voltage3Status bit if is greater than Voltage3Limit 10: Monitor current value (combined value from registers 66h and 65h) against Voltage3Limit (combined value from registers 68h and 67h); set Voltage3Status bit if it is lower than Voltage3Limit 11: Monitor Voltage3Hi against the limits. Set Voltage3Status when it is more than Voltage3LimitLo [7:0] or lower than Voltage3LimitHi [15:8]

VoltageControl1- RW – 8 bits - [PM2_Reg: B3h]			
Field Name	**Bits**	**Default**	**Description**
Voltage4Control	1:0	00b	Values other than 00 indicate that Voltage4 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 6Ah and 69h) against Voltage4Limit (combined value from registers 6Ch and 6Bh); set Voltage4Status bit if is greater than Voltage4Limit 10: Monitor current value (combined value from registers 6Ah and 69h) against Voltage4Limit (combined value from registers 6Ch and 6Bh); set Voltage4Status bit if it is lower than Voltage4Limit 11: Monitor Voltage4Hi against the limits. Set Voltage4Status when it is more than Voltage4LimitLo [7:0] or lower than Voltage4LimitHi [15:8]
Voltage5Control	3:2	00b	Values other than 00 indicate that Voltage5 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 6Eh and 6Dh) against Voltage5Limit (combined value from registers 70h and 6Fh); set Voltage5Status bit if is greater than Voltage5Limit 10: Monitor current value (combined value from registers 6Eh and 6Dh) against Voltage5Limit (combined value from registers 70h and 6Fh); set Voltage5Status bit if it is lower than Voltage5Limit 11: Monitor Voltage5Hi against the limits. Set Voltage5Status when it is more than Voltage5LimitLo [7:0] or lower than Voltage5LimitHi [15:8]
Voltage6Control	5:4	00b	Values other than 00 indicate that Voltage6 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 72h and 71h) against Voltage6Limit (combined value from registers 74h and 73h); set Voltage6Status bit if is greater than Voltage6Limit 10: Monitor current value (combined value from registers 72h and 71h) against Voltage6Limit (combined value from registers 74h and 73h); set Voltage6Status bit if it is lower than Voltage6Limit 11: Monitor Voltage6Hi against the limits. Set Voltage6Status when it is more than Voltage6LimitLo [7:0] or lower than Voltage6LimitHi [15:8]

VoltageControl1- RW – 8 bits - [PM2_Reg: B3h]			
Field Name	**Bits**	**Default**	**Description**
Voltage7Control	7:6	00b	Values other than 00 indicate that Voltage7 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 76h and 75h) against Voltage7Limit (combined value from registers 78h and 77h); set Voltage7Status bit if is greater than Voltage7Limit 10: Monitor current value (combined value from registers 76h and 75h) against Voltage7Limit (combined value from registers 78h and 77h); set Voltage7Status bit if it is lower than Voltage7Limit 11: Monitor Voltage7Hi against the limits. Set Voltage7Status when it is more than Voltage7LimitLo [7:0] or lower than Voltage7LimitHi [15:8]

AnalogINTRoute0 - RW – 8 bits - [PM2_Reg: B5h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage1INTRoute	3:2	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage2INTRoute	5:4	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage3INTRoute	7:6	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated

AnalogINTRoute1 - RW – 8 bits - [PM2_Reg: B6h]			
Field Name	**Bits**	**Default**	**Description**
Voltage4INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage5INTRoute	3:2	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage6INTRoute	5:4	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage7INTRoute	7:6	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated

Voltage0Lo- R – 8 bits - [PM2_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0Lo	7:0	00h	Voltage0 [7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage0Hi- R – 8 bits - [PM2_Reg: B9h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0Hi	7:0	00h	Voltage0 [15:8]

Voltage0LimitLo- RW – 8 bits - [PM2_Reg: BAh]			
Field Name	**Bits**	**Default**	**Description**
Voltage0LimitLo	7:0	00h	Voltage0Limit[7:0]

Voltage0LimitHi- RW – 8 bits - [PM2_Reg: BBh]			
Field Name	**Bits**	**Default**	**Description**
Voltage0LimitHi	7:0	00h	Voltage0Limit[15:8]

Voltage1Lo- R – 8 bits - [PM2_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**
Voltage1Lo	7:0	00h	Voltage1 [7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage1Hi- R – 8 bits - [PM2_Reg: BDh]			
Field Name	**Bits**	**Default**	**Description**
Voltage1Hi	7:0	00h	Voltage1 [15:8]

Voltage1LimitLo- RW – 8 bits - [PM2_Reg: BEh]			
Field Name	**Bits**	**Default**	**Description**
Voltage1LimitLo	7:0	00h	Voltage1Limit[7:0]

Voltage1LimitHi- RW – 8 bits - [PM2_Reg: BFh]			
Field Name	**Bits**	**Default**	**Description**
VoltageLimit1Hi	7:0	00h	Voltage1Limit[15:8]

Voltage2Lo- R – 8 bits - [PM2_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
Voltage2Lo	7:0	00h	Voltage2[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage2Hi- R – 8 bits - [PM2_Reg: C1h]			
Field Name	**Bits**	**Default**	**Description**
Voltage2Hi	7:0	00h	Voltage2[15:8]

Voltage2LimitLo- RW – 8 bits - [PM2_Reg: C2]			
Field Name	**Bits**	**Default**	**Description**
Voltage2LimitLo	7:0	00h	Voltage2Limit[7:0]

Voltage2LimitHi- RW – 8 bits - [PM2_Reg: C3h]			
Field Name	**Bits**	**Default**	**Description**
Voltage2LimitHi	7:0	00h	Voltage2Limit[15:8]

Voltage3Lo- R – 8 bits - [PM2_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Voltage3Lo	7:0	00h	Voltage3[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage3Hi- R – 8 bits - [PM2_Reg: C5h]			
Field Name	**Bits**	**Default**	**Description**
Voltage3Hi	7:0	00h	Voltage3[15:8]

Voltage3LimitLo- RW – 8 bits - [PM2_Reg: C6]			
Field Name	**Bits**	**Default**	**Description**
Voltage3LimitLo	7:0	00h	Voltage3Limit[7:0]

Voltage3LimitHi- RW – 8 bits - [PM2_Reg: C7h]			
Field Name	**Bits**	**Default**	**Description**
Voltage3LimitHi	7:0	00h	Voltage3Limit[15:8]

Voltage4Lo- R – 8 bits - [PM2_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
Voltage4Lo	7:0	00h	Voltage4[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage4Hi- R – 8 bits - [PM2_Reg: C9h]			
Field Name	**Bits**	**Default**	**Description**
Voltage4Hi	7:0	00h	Voltage4[15:8]

Voltage4LimitLo- RW – 8 bits - [PM2_Reg: CA]			
Field Name	**Bits**	**Default**	**Description**
Voltage4LimitLo	7:0	00h	Voltage4Limit[7:0]

Voltage4LimitHi- RW – 8 bits - [PM2_Reg: CBh]			
Field Name	**Bits**	**Default**	**Description**
Voltage4LimitHi	7:0	00h	Voltage4Limit[15:8]

Voltage5Lo- R – 8 bits - [PM2_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
Voltage5Lo	7:0	00h	Voltage5[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage5Hi- R – 8 bits - [PM2_Reg: CDh]			
Field Name	**Bits**	**Default**	**Description**
Voltage5Hi	7:0	00h	Voltage5[15:8]

Voltage5LimitLo- RW – 8 bits - [PM2_Reg: CE]			
Field Name	**Bits**	**Default**	**Description**
Voltage5LimitLo	7:0	00h	Voltage5Limit[7:0]

Voltage5LimitHi- RW – 8 bits - [PM2_Reg: CFh]			
Field Name	**Bits**	**Default**	**Description**
Voltage5LimitHi	7:0	00h	Voltage5Limit[15:8]

Voltage6Lo- R – 8 bits - [PM2_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Voltage6Lo	7:0	00h	Voltage6[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage6Hi- R – 8 bits - [PM2_Reg: D1h]			
Field Name	**Bits**	**Default**	**Description**
Voltage6Hi	7:0	00h	Voltage6[15:8]

Voltage6LimitLo- RW – 8 bits - [PM2_Reg: D2]			
Field Name	**Bits**	**Default**	**Description**
Voltage6LimitLo	7:0	00h	Voltage6Limit[7:0]

Voltage6LimitHi- RW – 8 bits - [PM2_Reg: D3h]			
Field Name	**Bits**	**Default**	**Description**
Voltage6LimitHi	7:0	00h	Voltage6Limit[15:8]

Voltage7Lo- R – 8 bits - [PM2_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
Voltage7Lo	7:0	00h	Voltage7[7:0]

Note: Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage7Hi- R – 8 bits - [PM2_Reg: D5h]			
Field Name	**Bits**	**Default**	**Description**
Voltage7Hi	7:0	00h	Voltage7[15:8]

Voltage7LimitLo- RW – 8 bits - [PM2_Reg: D6]			
Field Name	**Bits**	**Default**	**Description**
Voltage7LimitLo	7:0	00h	Voltage7Limit[7:0]

Voltage7LimitHi- RW – 8 bits - [PM2_Reg: D7h]			
Field Name	**Bits**	**Default**	**Description**
Voltage7LimitHi	7:0	00h	Voltage7Limit[15:8]

AnologloRstSel- RW – 8 bits - [PM2_Reg: DDh]			
Field Name	**Bits**	**Default**	**Description**
Voltage0RstSel	0	0	If set, VIN0 (voltage monitoring) function will not be stopped by reset. 0: disbale 1: enable
Voltage1RstSel	1	0	If set, VIN1 (voltage monitoring) function will not be stopped by reset. 0: disbale 1: enable
Voltage2RstSel	2	0	If set, VIN2 (voltage monitoring) function will not be stopped by reset. 0: disbale 1: enable
Voltage3RstSel	3	0	If set, VIN3 (voltage monitoring) function will not be stopped by reset. 0: disbale 1: enable
Voltage4RstSel	4	0	If set, VIN4 (voltage monitoring) function will not be stopped by reset. 0: disbale 1: enable

AnologloRstSel- RW – 8 bits - [PM2_Reg: DDh]			
Field Name	**Bits**	**Default**	**Description**
Voltage5RstSel	5	0	If set, VIN5 (voltage monitoring) function will not be stopped by reset. 0: disbale 1: enable
Voltage6RstSel	6	0	If set, VIN6 (voltage monitoring) function will not be stopped by reset. 0: disbale 1: enable
Voltage7RstSel	7	0	If set, VIN7 (voltage monitoring) function will not be stopped by reset. 0: disbale 1: enable

TempRstSel- RW – 8 bits - [PM2_Reg: DFh]			
Field Name	**Bits**	**Default**	**Description**
Temp0RstSel	0	0	If set, TEMPIN0 (thermal diode monitoring) function will not be stopped by reset. 0: disbale 1: enable
Temp1RstSel	1	0	If set, TEMPIN1 (thermal diode monitoring) function will not be stopped by reset. 0: disbale 1: enable
Temp2RstSel	2	0	If set, TEMPIN2 (thermal diode monitoring) function will not be stopped by reset. 0: disbale 1: enable
Temp3RstSel	3	0	If set, TEMPIN3 (thermal diode monitoring) function will not be stopped by reset. 0: disbale 1: enable
Temp4RstSel	4	0	If set, TEMPIN4 (thermal diode monitoring) function will not be stopped by reset. 0: disbale 1: enable

AlertThermaltripStatus- R – 8 bits - [PM2_Reg: E0h]			
Field Name	**Bits**	**Default**	**Description**
AlertStatus	0	0b	Read only. 0: Current temperature is not above AlertLimit 1: Current temperature is above AlertLimit
ThermalTripStatus	1	0b	Read only. 0: Current temperature is not above ThermalTripLimit 1: Current temperature is above ThermalTripLimit
Reserved	7:2		Reserved

AlertLimitLo- RW – 8 bits - [PM2_Reg: E1h]			
Field Name	**Bits**	**Default**	**Description**
AlertLimit	7:0	00h	AlertLimit[7:0]

AlertLimitHi- RW – 8 bits - [PM2_Reg: E2h]			
Field Name	**Bits**	**Default**	**Description**
AlertLimit	7:0	00h	AlertLimit[15:8]

ThermalTripLimitLo- RW – 8 bits - [PM2_Reg: E3h]			
Field Name	**Bits**	**Default**	**Description**
ThermalTripLimit	7:0	00h	ThermalTripLimit [7:0]

ThermalTripLimitHi- RW – 8 bits - [PM2_Reg: E4h]			
Field Name	**Bits**	**Default**	Description
ThermalTripLimit	7:0	00h	ThermalTripLimit [15:8]

AlertThermaltripControl- RW – 8 bits - [PM2_Reg: E5h]			
Field Name	**Bits**	**Default**	**Description**
AlertControl	1:0	00b	Bit 0: Enable TAlert on the selected Temp input Bit 1: Enable ThermalTrip on the selected Temp input
TempSelAlert	7:5	000b	Select temperature sensor as event source 000: Temp0 001: Temp1 010: Temp2 011: Temp3 100: Temp4 Others: Temp0 This register converts the Temp* pin into either TAlert or ThermalTrip function.

HwmControl- R/W – 8 bits - [PM2_Reg: E6h]			
Field Name	**Bits**	**Default**	**Description**
HostReadSensor	0	0b	Writing to1 forces HWM to do a read.
AutoReadSensor	1	0b	Set to 1 to enable periodical reading of voltage/temperature sensors
FastReadEnable	2	0	Set to1 to keep HWM reading sensors repeatedly.
PDAlways	3	0	0: Power on the HWM only when doing a sensor reading. 1: Power on the HWM all the time.
Reserved	6:4	000	.
ResetSensor	7	0	0: Running state 1: Put the HWM into reset state.

VoltageReadFreq - R/W – 8 bits - [PM2_Reg: E7h]			
Field Name	**Bits**	**Default**	**Description**
VoltSensorReadFreq	1:0	00b	00: 100 Hz 01: 200 Hz 10: 300 Hz 11: 500 Hz
Reserved	6:2	00000b	
VoltReadus	7	0b	1: Voltage read period in µs 0: Voltage read period in ms

TempReadFreq - R/W – 8 bits - [PM2_Reg: E8h]			
Field Name	**Bits**	**Default**	**Description**
TempSensorReadFreq	1:0	00b	00: 100ms 01: 200ms 10: 300ms 11: 500ms
Reserved	7:2	000000b	Reserved

VoltageReadAverage – R/W – 8 bits - [PM2_Reg: E9h]			
Field Name	**Bits**	**Default**	**Description**
Volateg0_Average	0	0b	Set to 1 to enable cumulative averaging of Vin0.
Volateg1_Average	1	0b	Set to 1 to enable cumulative averaging of Vin1.
Volateg2_Average	2	0b	Set to 1 to enable cumulative averaging of Vin2.
Volateg3_Average	3	0b	Set to 1 to enable cumulative averaging of Vin3.
Volateg4_Average	4	0b	Set to 1 to enable cumulative averaging of Vin4.
Volateg5_Average	5	0b	Set to 1 to enable cumulative averaging of Vin5.
Volateg6_Average	6	0b	Set to 1 to enable cumulative averaging of Vin6.
Volateg7_Average	7	0b	Set to 1 to enable cumulative averaging of Vin7.

Hwm_VoltCalib – R – 8 bits - [PM2_Reg: EAh]			
Field Name	**Bits**	**Default**	**Description**
Voltage_calibration	6:0	0000000b	Hwm calibration value
Voltage_calibrationValid	7	0b	1: Voltage_calibration in this register is valid. 0: Voltage_calibration in this register is invalid.

TempReadAverage – R/W – 8 bits - [PM2_Reg: EBh]			
Field Name	**Bits**	**Default**	**Description**
IntTemp_Average	0	1b	Set to 1 to enable cumulative averaging of Internal Temp.
Temp0_Average	1	0b	Set to 1 to enable cumulative averaging of Temp0.
Temp1_Average	2	0b	Set to 1 to enable cumulative averaging of Temp1.
Temp2_Average	3	1b	Set to 1 to enable cumulative averaging of Temp2.
Temp3_Average	4	1b	Set to 1 to enable cumulative averaging of Temp3.
Reserved	7:5	000b	Reserved

HwmStatus – R – 8 bits - [PM2_Reg: ECh]			
Field Name	**Bits**	**Default**	**Description**
SensorIdle	0	0b	0: HWM is idle. 1: HWM is doing the sensor reading.
Reserved	6:1	000000b	Reserved
HostReadSts	7	0b	0: No host read is pending. 1: Host read is pending.

VoltageReadStatus – R – 8 bits - [PM2_Reg: EDh]			
Field Name	**Bits**	**Default**	**Description**
Voltage0ReadStatus	0	0b	0: No Voltage0 reading is pending. 1: Voltage0 reading is pending.
Voltage1ReadStatus	1	0b	0: No Voltage1 reading is pending. 1: Voltage1 reading is pending.
Voltage2ReadStatus	2	0b	0: No Voltage2 reading is pending. 1: Voltage2 reading is pending.
Voltage3ReadStatus	3	0b	0: No Voltage3 reading is pending. 1: Voltage3 reading is pending.
Voltage4ReadStatus	4	0b	0: No Voltage4 reading is pending. 1: Voltage4 reading is pending.
Voltage5ReadStatus	5	0b	0: No Voltage5 reading is pending. 1: Voltage5 reading is pending.
Voltage6ReadStatus	6	0b	0: No Voltage6 reading is pending. 1: Voltage6 reading is pending.
Voltage7ReadStatus	7	0b	0: No Voltage7 reading is pending. 1: Voltage7 reading is pending.

TempReadStatus – R – 8 bits - [PM2_Reg: EEh]			
Field Name	**Bits**	**Default**	**Description**
IntTempReadStatus	0	0b	0: No Internal Temp reading is pending. 1: Internal Temp reading is pending.
Temp0ReadStatus	1	0b	0: No Temp0 reading is pending. 1: Temp0 reading is pending.
Temp1ReadStatus	2	0b	0: No Temp1 reading is pending. 1: Temp1 reading is pending.
Temp2ReadStatus	3	0b	0: No Temp2 reading is pending. 1: Temp2 reading is pending.
Temp3ReadStatus	4	0b	0: No Temp3 reading is pending. 1: Temp3 reading is pending.
Reserved	7:5	000b	Reserved

HwmClkControl – R/W – 8 bits - [PM2_Reg: EFh]			
Field Name	**Bits**	**Default**	**Description**
SensorClkDiv	3:0	0000b	Used to set the Hwm_Clk (sampling clock rate) frequency based on the formula below: Hwm_Clk = 66.67MHz / (2 * (SensorClkDiv+2)) For example: Hwm_Clk = 16.67MHz when the SensorClkDiv is set to value of 0000b Hwm_Clk = 11.11MHz when the SensorClkDiv is set to value of 0001b Note: The recommended value is 1010 (i.e. A)
Reserved	7:4	0000b	Reserved

ADC_PDBTime – R/W – 8 bits - [PM2_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
ADC_PDBTime	4:0	11001b	Control the time between HWM_PDB and ADC_PDB. Its unit is µs. Default is 25 µs.
Reserved	7:5	000b	Reserved

ADC_StartUp – R/W – 8 bits - [PM2_Reg: F1h]			
Field Name	**Bits**	**Default**	**Description**
ADC_StartUp	3:0	1010b	Control the time between ADC_RESET and sensor reading. Its unit is µs. Default is 10 µs.
Reserved	7:4	0000b	Reserved

ADC_Delay – R/W – 8 bits - [PM2_Reg: F2h]			
Field Name	**Bits**	**Default**	**Description**
ADC_StartUp	3:0	0010b	Control the delay time between two back to back reading. Its unit is us. Default is 2 µs.
Reserved	7:4	0000b	Reserved

SAX_CTL_VTime – R/W – 8 bits - [PM2_Reg: F3h]			
Field Name	**Bits**	**Default**	**Description**
SAX_CTL_VTime	3:0	0101b	Control the assertion time of SAX_CTL_V. Default is 5 µs.
Reserved	7:4	0000b	Reserved

SAX_CTL_TTime – R/W – 8 bits - [PM2_Reg: F4h]			
Field Name	**Bits**	**Default**	**Description**
SAX_CTL_TTime	7:0	11001000b	Control the assertion time of SAX_CTL_T. Default is 200 µs.

BGADJ – R/W – 8 bits - [PM2_Reg: F5h]			
Field Name	**Bits**	**Default**	**Description**
BGADJ	5:0	100000b	HWM tuning parameter
Reserved	7:6	00b	Reserved

AFEcfg_Clkdiv – R/W – 8 bits - [PM2_Reg: F6h]			
Field Name	**Bits**	**Default**	**Description**
AFE_cfg	1:0	00b	HWM tuning parameter
Reserved	5:2	0000b	Reserved
Clk_div	7:6	10b	HWM tuning parameter

Hwm_DebugSel – R/W – 8 bits - [PM2_Reg: F7h]			
Field Name	**Bits**	**Default**	**Description**
Hwm_Macro_DebugSel	3:0	0000b	HWM tuning parameter
Reserved	7:4	0000b	Reserved

VoltageSampleSel – R/W – 8 bits - [PM2_Reg: F8h]			
Field Name	**Bits**	**Default**	**Description**
Num_Samples_ForVolt	2:0	100b	Specify number of samples per voltage reading. Default value is 1 sample per reading. 000 : 1 sample 001 : 2 samples 010 : 4 samples 011 : 8 samples 100 : 16 samples (default) 101 : 32 samples 110 : 64 samples
HiRatioEnableForIntTemp	3	0b	Set to 1 to enable hi current ratio on Internal Temp.
HiRatioEnableForTemp0	4	0b	Set to 1 to enable hi current ratio on Temp0.
HiRatioEnableForTemp1	5	0b	Set to 1 to enable hi current ratio on Temp1.
HiRatioEnableForTemp2	6	0b	Set to 1 to enable hi current ratio on Temp2.
HiRatioEnableForTemp3	7	0b	Set to 1 to enable hi current ratio on Temp3.

TempSampleSel – R/W – 8 bits - [PM2_Reg: F9h]			
Field Name	**Bits**	**Default**	**Description**
Num_Samples_ForTemp	2:0	110b	Specify number of samples per Temp reading. Default value is 16 samples per reading 000 : 1 sample 001 : 2 samples 010 : 4 samples 011 : 8 samples 100 : 16 samples 101 : 32 samples 110 : 64 samples (default)
HiCurEnableForIntTemp	3	0b	Set to 1 to enable hi current on internal temp.
HiCurEnableForTemp0	4	0b	Set to 1 to enable hi current on temp0.
HiCurEnableForTemp1	5	0b	Set to 1 to enable hi current on temp1.
HiCurEnableForTemp2	6	0b	Set to 1 to enable hi current on temp2.
HiCurEnableForTemp3	7	0b	Set to 1 to enable hi current on temp3.

HwmVoltage_div0 – R/W – 8 bits - [PM2_Reg: FAh]			
Field Name	**Bits**	**Default**	**Description**
Volt0_div	1:0	00b	Specify voltage0 read range.
Volt1_div	3:2	00b	Specify voltage1 read range.
Volt2_div	5:4	00b	Specify voltage2 read range.
Volt3_div	7:6	00b	Specify voltage3 read range.

HwmVoltage_div1 – R/W – 8 bits - [PM2_Reg: FBh]			
Field Name	**Bits**	**Default**	**Description**
Volt4_div	1:0	00b	Specify voltage4 read range.
Volt5_div	3:2	00b	Specify voltage5 read range.
Volt6_div	5:4	00b	Specify voltage6 read range.
Volt7_div	7:6	00b	Specify voltage7 read range.

Adc_Gain_Adj – R/W – 8 bits - [PM2_Reg: FCh]			
Field Name	**Bits**	**Default**	**Description**
Adc_Gain_Adj	3:0	1000b	HWM tuning parameter.
Reserved	7:4	0000b	Reserved

Adc_cfg – R/W – 8 bits - [PM2_Reg: FDh]			
Field Name	**Bits**	**Default**	**Description**
Adc_cfg	3:0	1000b	HWM tuning parameter
Reserved	7:4	0000b	Reserved

Test_cntl – R/W – 8 bits - [PM2_Reg: FEh]			
Field Name	**Bits**	**Default**	**Description**
Test_cntl	3:0	000b	HWM tuning parameter
Reserved	7:4	0000b	Reserved

HwmMiscControl – R/W – 8 bits - [PM2_Reg: FFh]			
Field Name	**Bits**	**Default**	**Description**
Aport_mode	1:0	10b	HWM tuning parameter
Reserved	2	0b	Reserved
Gpio_A_Cntrl	3	0b	HWM tuning parameter
Offset_Can_En	4	0b	HWM tuning parameter
Cycle_en	5	0b	HWM tuning parameter

3.5 SMI Registers

SMI registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from “AcpiMMioAddr” + 0x200 to “AcpiMMioAddr” + 0x2FF.

The base address “AcpiMMioAddr” is defined in PM_reg x24, with the default base address at “FED8_0000”.

Register Name	Offset Address
EventStatus	00h
EventEnable	04h
SciTrig	08h
SciLevl	0Ch
SmiSciStatus	10h
SmiSciEn	14h
SwSciEn	18h
SwSciData	1Ch
SciSleepDisable	20h
Reserved	24-2Fh
CapturedData	30h
CapturedValid	34h
EPBIF_AER_Straps	38h
DataErrorStatus	3Ch
SciMap0	40h
SciMap1	44h
SciMap2	48h
SciMap3	4Ch
SciMap4	50h
SciMap5	54h
SciMap6	58h
SciMap7	5Ch
SciMap8	60h
SciMap9	64h
SciMap10	68h
SciMap11	6Ch
SciMap12	70h
SciMap13	74h
SciMap14	78h
Reserved	7Ch
SmiStatus0	80h
SmiStatus1	84h
SmiStatus2	88h
SmiPointer	94h
SmiShortTimer/SmiLongTimer	96h
GeventTrig	98h
IrqTrig	9Ch
SmiControl0	A0h
SmiControl1	A4h
SmiControl2	A8h
SmiControl3	ACh
SmiControl4	B0h
SmiControl5	B4h
SmiControl6	B8h
SmiControl7	BCh
SmiControl8	C0h
SmiControl9	C4h
IoTrapping0	C8h
IoTrapping1	CAh
IoTrapping2	CCh
IoTrapping3	CEh
MemTrappingAdr0	D0h
MemRdOvrData0	D4h
MemTrappingAdr1	D8h
MemRdOvrData1	DCh
MemTrappingAdr2	E0h

Register Name	Offset Address
MemRdOvrData2	E4h
MemTrappingAdr3	E8h
MemRdOvrData3	ECh
CfgTrappingAdr0	F0h
CfgTrappingAdr1	F4h
CfgTrappingAdr2	F8h
CfgTrappingAdr3	FCh

Event_Status -R/W – 8/16/32 bits - [SMI_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
EventStatus	31:0		This is a mirror register of the standard ACPI EVENT_STATUS register. Writing 1 to each bit clears the corresponding status bit. Each Event status is set when the selected event input equals to the corresponding value in SciTrig.

Event_Enable -RW – 32 bits - [SMI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
EventEnable	31:0	32'h0	This is the mirror register of the standard ACPI EVENT_ENABLE register. Each bit controls whether ACP should generate wakeup and SCi interrupt.

SciTrig -RW – 32 bits - [SMI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
SciTrig0	0	1b	The bit controls the way to set Event_Status bit 0 0: Active low 1: Active high
SciTrig1	1	1b	The bit controls the way to set Event_Status bit 1 0: Active low 1: Active high
SciTrig2	2	1b	The bit controls the way to set Event_Status bit 2 0: Active low 1: Active high
SciTrig3	3	1b	The bit controls the way to set Event_Status bit 3 0: Active low 1: Active high
SciTrig4	4	1b	The bit controls the way to set Event_Status bit 4 0: Active low 1: Active high
SciTrig5	5	1b	The bit controls the way to set Event_Status bit 5 0: Active low 1: Active high
SciTrig6	6	1b	The bit controls the way to set Event_Status bit 6 0: Active low 1: Active high
SciTrig7	7	1b	The bit controls the way to set Event_Status bit 7 0: Active low 1: Active high
SciTrig8	8	1b	The bit controls the way to set Event_Status bit 8 0: Active low 1: Active high

SciTrig -RW – 32 bits - [SMI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
SciTrig9	9	1b	The bit controls the way to set Event_Status bit 9 0: Active low 1: Active high
SciTrig10	10	1b	The bit controls the way to set Event_Status bit 10 0: Active low 1: Active high
SciTrig11	11	1b	The bit controls the way to set Event_Status bit 11 0: Falling edge 1: Active high
SciTrig12	12	1b	The bit controls the way to set Event_Status bit 12 0: Active low 1: Active high
SciTrig13	13	1b	The bit controls the way to set Event_Status bit 13 0: Active low 1: Active high
SciTrig14	14	1b	The bit controls the way to set Event_Status bit 14 0: Active low 1: Active high
SciTrig15	15	1b	The bit controls the way to set Event_Status bit 15 0: Active low 1: Active high
SciTrig16	16	1b	The bit controls the way to set Event_Status bit 16 0: Active low 1: Active high
SciTrig17	17	1b	The bit controls the way to set Event_Status bit 17 0: Active low 1: Active high
SciTrig18	18	1b	The bit controls the way to set Event_Status bit 18 0: Active low 1: Active high
SciTrig19	19	1b	The bit controls the way to set Event_Status bit 19 0: Active low 1: Active high
SciTrig20	20	1b	The bit controls the way to set Event_Status bit 20 0: Active low 1: Active high
SciTrig21	21	1b	The bit controls the way to set Event_Status bit 21 0: Active low 1: Active high
SciTrig22	22	1b	The bit controls the way to set Event_Status bit 22 0: Active low 1: Active high
SciTrig23	23	1b	The bit controls the way to set Event_Status bit 23 0: Active low 1: Active high
SciTrig24	24	1b	The bit controls the way to set Event_Status bit 24 0: Active low 1: Active high
SciTrig25	25	1b	The bit controls the way to set Event_Status bit 25 0: Active low 1: Active high
SciTrig26	26	1b	The bit controls the way to set Event_Status bit 26 0: Active low 1: Active high
SciTrig27	27	1b	The bit controls the way to set Event_Status bit 27 0: Active low 1: Active high

SciTrig -RW – 32 bits - [SMI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
SciTrig28	28	1b	The bit controls the way to set Event_Status bit 28 0: Active low 1: Active high
ScTrig29	29	1b	The bit controls the way to set Event_Status bit 29 0: Active low 1: Active high
SciTrig30	30	1b	The bit controls the way to set Event_Status bit 30 0: Active low 1: Active high
SciTrig31	31	1b	The bit controls the way to set Event_Status bit 31 0: Active low 1: Active high

SciLevl -RW –32 bits - [SMI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
SciLevl0	0	0	This register defines the trigger mode for each of the Event_Status: 0: Edge trigger 1: Level trigger
SciLevl1	1	0	0: Edge trigger 1: Level trigger
SciLevl2	2	0	0: Edge trigger 1: Level trigger
SciLevl3	3	0	0: Edge trigger 1: Level trigger
SciLevl4	4	0	0: Edge trigger 1: Level trigger
SciLevl5	5	0	0: Edge trigger 1: Level trigger
SciLevl6	6	0	0: Edge trigger 1: Level trigger
SciLevl7	7	0	0: Edge trigger 1: Level trigger
SciLevl8	8	0	0: Edge trigger 1: Level trigger
SciLevl9	9	0	0: Edge trigger 1: Level trigger
SciLevl10	10	0	0: Edge trigger 1: Level trigger
SciLevl11	11	0	0: Edge trigger 1: Level trigger
SciLevl12	12	0	0: Edge trigger 1: Level trigger
SciLevl13	13	0	0: Edge trigger 1: Level trigger
SciLevl14	14	0	0: Edge trigger 1: Level trigger
SciLevl15	15	0	0: Edge trigger 1: Level trigger
SciLevl16	16	0	0: Edge trigger 1: Level trigger
SciLevl17	17	0	0: Edge trigger 1: Level trigger
SciLevl18	18	0	0: Edge trigger 1: Level trigger
SciLevl19	19	0	0: Edge trigger 1: Level trigger

SciLevl -RW –32 bits - [SMI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
SciLevl20	20	0	0: Edge trigger 1: Level trigger
SciLevl21	21	0	0: Edge trigger 1: Level trigger
SciLevl22	22	0	0: Edge trigger 1: Level trigger
SciLevl23	23	0	0: Edge trigger 1: Level trigger
SciLevl24	24	0	0: Edge trigger 1: Level trigger
SciLevl25	25	0	0: Edge trigger 1: Level trigger
SciLevl26	26	0	0: Edge trigger 1: Level trigger
SciLevl27	27	0	0: Edge trigger 1: Level trigger
SciLevl28	28	0	0: Edge trigger 1: Level trigger
SciLevl29	29	0	0: Edge trigger 1: Level trigger
SciLevl30	30	0	0: Edge trigger 1: Level trigger
SciLevl31	31	0	0: Edge trigger 1: Level trigger

SmiSciStatus - RW – 32 bits - [SMI_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
SmiSciStatus	31:0	32'h0	Each bit indicates the corresponding SmiSci status. The input of each bit is controlled by the corresponding SciTrig bit. Each status bit can be cleared to 0 by writing 1. Note this function can be considered as a superset of Event_Status. When one of this bit is set (and its SmiSciEn is also set), it will trigger a SMI to call the BIOS. After the BIOS has serviced the SMM and clears its status, the internal logic will automatically set the corresponding Event_Status bit and thereby triggering a SCI.

SmiSciEn – RW – 32 bits - [SMI_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
SmiSciEn	31:0	32'h0	Each bit controls if SMI message will be generated when the corresponding SmiSciStatus bit is set to 1. 0: Not to send SMI message when the corresponding SmiSciStatus bit is set 1: Send SMI message when the corresponding SmiSciStatus bit is set

SwSciEn - RW – 32 bits - [SMI_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
SwSciEn	31:0	32'h0	When set, software can write to SwSciData and set the corresponding Event_Status bit (note the setting of this bit will need to match with SciTrig and SciLevl in order to set the status bit). This register is meant as a software mechanism to trigger SCI.

SwSciData - RW – 32 bits - [SMI_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
SwSciData	31:0	32'h0	This is the software data path to set the corresponding Event_Status when SwSciEn is set

SciSleepDisable - RW – 32 bits - [SMI_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
SciSleepDisable	31:0	32'h0	When set, the corresponding Event_Status bit will be masked off whenever the system goes to S3 or higher sleep state. This is meant for ignoring EVENT pins that are powered in the main power domain (instead of aux. power domain).

CapturedData - RO – 32 bits - [SMI_Reg: 30h]			
Field Name	**Bits**	**Default**	**Description**
CapturedData	31:0	--	This is the buffer to capture write data for the last transaction that caused an SMI#. **Note:** this buffer has no meaning for a read trap

CapturedValid - RO – 8 bits - [SMI_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
CapturedValid	3:0	--	This is the byte valid buffer to signal which byte is captured for the last transaction that caused the SMI. Bit 0 for byte 0, 1 for byte 1, 2 for byte 2, 3 for byte 3

EPBIF_AER_Straps - RW – 32 bits - [SMI_Reg: 38h]			
Field Name	**Bits**	**Default**	**Description**
STRAP_UMI_STICKY_OVERRIDE_S5	0	0b	When set to 1, values in this register would override straps loaded from EEPROM.
STRAP_UMI_AER_EN_SB	1	1b	AER enable.
STRAP_UMI_ERR_REPORTING_DIS_SB	2	1b	Error reporting disable.
STRAP_UMI_RX_IGNORE_BE_ERR_SB	3	1b	Ignore byte enable error.
STRAP_UMI_RX_IGNORE_CFG_ERR_SB	4	1b	Ignore configuration error.
STRAP_UMI_RX_IGNORE_CFG_UR_SB	5	1b	Ignore config. UR error.

EPBIF_AER_Straps - RW – 32 bits - [SMI_Reg: 38h]			
Field Name	**Bits**	**Default**	**Description**
STRAP_UMI_RX_IGNORE_CPL_ERR_SB	6	1b	Ignore completion error.
STRAP_UMI_RX_IGNORE_EP_ERR_SB	7	1b	Ignore poisoned TLP error.
STRAP_UMI_RX_IGNORE_IO_ERR_SB	8	1b	Ignore IO error.
STRAP_UMI_RX_IGNORE_IO_UR_ERR_SB	9	1b	Ignore IO UR error.
STRAP_UMI_RX_IGNORE_LEN_MISMATCH_ERR_SB	10	1b	Ignore length mismatch error.
STRAP_UMI_RX_IGNORE_MAX_PAYLOAD_ERR_SB	11	1b	Ignore maximum payload error.
STRAP_UMI_RX_IGNORE_MSG_ERR_SB	12	1b	Ignore message error.
STRAP_UMI_RX_IGNORE_TC_ERR_SB	13	1b	Ignore traffic class error.
STRAP_UMI_RX_IGNORE_VEND0_UR_SB	14	1b	Ignore Vendor 0 error.
STRAP_UMI_CPL_ABORT_ERR_EN_SB	15	1b	Completer abort error enable.
STRAP_UMI_ECRC_GEN_EN_SB	16	1b	ECRC generate enable.
STRAP_UMI_ECRC_CHECK_EN_SB	17	1b	ECRC check enable.
STRAP_UMI_FIRST_RCVD_ERR_LOG_SB	18	1b	First received error log.
STRAP_UMI_ACS_EN_SB	19	1b	ACS enable.
STRAP_UMI_ACS_SOURCE_VALIDATION_SB	20	1b	ACS source validation enable.
STRAP_UMI_ACS_TRANSLATION_BLOCKING_SB	21	1b	ACS translation blocking enable.
STRAP_UMI_ACS_P2P_REQUEST_REDIRECT_SB	22	1b	ACS P2P request redirect enable.
STRAP_UMI_ACS_P2P_COMPLETION_REDIRECT_SB	23	1b	ACS P2P completion redirect enable.
STRAP_UMI_ACS_UPSTREAM_FORWARDING_SB	24	1b	ACS upstream forwarding enable.
STRAP_UMI_ACS_DIRECT_TRANSLATED_P2P_SB	25	1b	ACS direct translated P2P enable.
STRAP_UMI_POISONED_ADVISORY_NONFATAL_A_SB	26	1b	Poisoned TLP as advisory nonfatal.
STRAP_UMI_INTERNAL_ERR_EN_SB	27	0b	Internal error enable.
Reserved	31:28	0000b	Reserved

DataErrorStatus- RW – 32 bits - [SMI_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
InternalSerr	0	0b	Internal devices serr error status; write 1 to clear it to 0.
InternalPerr	1	0b	Internal devices Perr error status; write 1 to clear it to 0.

DataErrorStatus- RW – 32 bits - [SMI_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
FusionGPPSerr	2	0b	Fusion/GPP devices serr error status; write 1 to clear it to 0.
AbUMIGPPPerr	3	0b	AB/UMI/GPP parity error status; write 1 to clear it to 0.
UMI_correctable_Err	4	0b	UMIcorrectable error status; write 1 to clear it to 0.
UMI_uncorrectable_Err	5	0b	UMI uncorrectable error status; write 1 to clear it to 0.
SataPerr	6	0b	SATA controller internal parity error status; write 1 to clear it to 0.
Sirq_Iochk	7	0b	Serial Iochk error; write 1 to clear it to 0

SciMap0 - RW – 32 bits - [SMI_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_0	4:0	0000b	Mapping of GEVENT0 to one of 32 Event_Status. 0000: map event source 0 to the input of Event_Status bit 0 0001: map event source 0 to the input of Event_Status bit 1 … 1111: map input event0 to the input of Event_Status bit 31
SciMap_1	12:8	0000b	Mapping of GEVENT1 to one of 32 Event_Status. 0000: map event source 1 to the input of Event_Status bit 0 0001: map event source 1 to the input of Event_Status bit 1 … 1111: map event source 1 to the input of Event_Status bit 31
SciMap_2	20:16	0000b	Mapping of GEVENT2 to one of 32 Event_Status. 0000: map event source 2 to the input of Event_Status bit 0 0001: map event source 2 to the input of Event_Status bit 1 … 1111: map event source 2 to the input of Event_Status bit 31
SciMap_3	28:24	0000b	Mapping of GEVENT3 to one of 32 Event_Status. 0000: map event source 3 to the input of Event_Status bit 0 0001: map event source 3 to the input of Event_Status bit 1 … 1111: map event source 3 to the input of Event_Status bit 31

SciMap1 - RW – 32 bits - [SMI_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_4	4:0	0000b	Mapping of GEVENT4 to one of 32 Event_Status. 0000: map event source 4 to the input of Event_Status bit 0 0001: map event source 4 to the input of Event_Status bit 1 … 1111: map event source 4 to the input of Event_Status bit 31
SciMap_5	12:8	0000b	Mapping of GEVENT5 to one of 32 Event_Status. 0000: map event source 5 to the input of Event_Status bit 0 0001: map event source 5 to the input of Event_Status bit 1 … 1111: map event source 5 to the input of Event_Status bit 31
SciMap_6	20:16	0000b	Mapping of GEVENT6 to one of 32 Event_Status. 0000: map event source 6 to the input of Event_Status bit 0 0001: map event source 6 to the input of Event_Status bit 1 … 1111: map event source 6 to the input of Event_Status bit 31
SciMap_7	28:24	0000b	Mapping of GEVENT7 to one of 32 Event_Status. 0000: map event source 7 to the input of Event_Status bit 0 0001: map event source 7 to the input of Event_Status bit 1 … 1111: map event source 7 to the input of Event_Status bit 31

SciMap2 - RW – 32 bits - [SMI_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_8	4:0	0000b	Mapping of GEVENT8 to one of 32 Event_Status. 0000: map event source 8 to the input of Event_Status bit 0 0001: map event source 8 to the input of Event_Status bit 1 … 1111: map event source 8 to the input of Event_Status bit 31
SciMap_9	12:8	0000b	Mapping of GEVENT9 to one of 32 Event_Status. 0000: map event source 9 to the input of Event_Status bit 0 0001: map event source 9 to the input of Event_Status bit 1 … 1111: map event source 9 to the input of Event_Status bit 31
SciMap_10	20:16	0000b	Mapping of GEVENT10 to one of 32 Event_Status. 0000: map event source 10 to the input of Event_Status bit 0 0001: map event source 10 to the input of Event_Status bit 1 … 1111: map event source 10 to the input of Event_Status bit 31
SciMap_11	28:24	0000b	Mapping of GEVENT11 to one of 32 Event_Status. 0000: map event source 11 to the input of Event_Status bit 0 0001: map event source 11 to the input of Event_Status bit 1 … 1111: map event source 11 to the input of Event_Status bit 31

SciMap3 - RW – 32 bits - [SMI_Reg: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
SciMap_12	4:0	0000b	Mapping of GEVENT12 to one of 32 Event_Status. 0000: map event source 12 to the input of Event_Status bit 0 0001: map event source 12 to the input of Event_Status bit 1 … 1111: map event source 12 to the input of Event_Status bit 31
SciMap_13	12:8	0000b	Mapping of GEVENT13 to one of 32 Event_Status. 0000: map event source 13 to the input of Event_Status bit 0 0001: map event source 13 to the input of Event_Status bit 1 … 1111: map event source 13 to the input of Event_Status bit 31
SciMap_14	20:16	0000b	Mapping of GEVENT14 to one of 32 Event_Status. 0000: map event source 14 to the input of Event_Status bit 0 0001: map event source 14 to the input of Event_Status bit 1 … 1111: map event source 14 to the input of Event_Status bit 31
SciMap_15	28:24	0000b	Mapping of GEVENT15 to one of 32 Event_Status. 0000: map event source 15 to the input of Event_Status bit 0 0001: map event source 15 to the input of Event_Status bit 1 … 1111: map event source 15 to the input of Event_Status bit 31

SciMap4 - RW – 32 bits - [SMI_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_16	4:0	0000b	Mapping of GEVENT16 to one of 32 Event_Status. 0000: map event source 16 to the input of Event_Status bit 0 0001: map event source 16 to the input of Event_Status bit 1 … 1111: map event source 16 to the input of Event_Status bit 31
SciMap_17	12:8	0000b	Mapping of GEVENT17 to one of 32 Event_Status. 0000: map event source 17 to the input of Event_Status bit 0 0001: map event source 17 to the input of Event_Status bit 1 … 1111: map event source 17 to the input of Event_Status bit 31
SciMap_18	20:16	0000b	Mapping of GEVENT18 to one of 32 Event_Status. 0000: map event source 18 to the input of Event_Status bit 0 0001: map event source 18 to the input of Event_Status bit 1 … 1111: map event source 18 to the input of Event_Status bit 31
SciMap_19	28:24	0000b	Mapping of GEVENT19 to one of 32 Event_Status. 0000: map event source 19 to the input of Event_Status bit 0 0001: map event source 19 to the input of Event_Status bit 1 … 1111: map event source 19 to the input of Event_Status bit 31

SciMap5 - RW – 32 bits - [SMI_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_20	4:0	0000b	Mapping of GEVENT20 to one of 32 Event_Status. 0000: map event source 20 to the input of Event_Status bit 0 0001: map event source 20 to the input of Event_Status bit 1 … 1111: map event source 20 to the input of Event_Status bit 31
SciMap_21	12:8	0000b	Mapping of GEVENT21 to one of 32 Event_Status. 0000: map event source 21 to the input of Event_Status bit 0 0001: map event source 21 to the input of Event_Status bit 1 … 1111: map event source 21 to the input of Event_Status bit 31
SciMap_22	20:16	0000b	Mapping of GEVENT22 to one of 32 Event_Status. 0000: map event source 22 to the input of Event_Status bit 0 0001: map event source 22 to the input of Event_Status bit 1 … 1111: map event source 22 to the input of Event_Status bit 31
SciMap_23	28:24	0000b	Mapping of GEVENT23 to one of 32 Event_Status. 0000: map event source 23 to the input of Event_Status bit 0 0001: map event source 23 to the input of Event_Status bit 1 … 1111: map event source 23 to the input of Event_Status bit 31

SciMap6 - RW – 32 bits - [SMI_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_24	4:0	0000b	Mapping of USB_PME (device 18) to one of 32 Event_Status. 0000: map event source 24 to the input of Event_Status bit 0 0001: map event source 24 to the input of Event_Status bit 1 … 1111: map event source 24 to the input of Event_Status bit 31
SciMap_25	12:8	0000b	Mapping of USB_PME (device 19) to one of 32 Event_Status. 0000: map event source 25 to the input of Event_Status bit 0 0001: map event source 25 to the input of Event_Status bit 1 … 1111: map event source 25 to the input of Event_Status bit 31
SciMap_26	20:16	0000b	Mapping of USB_PME (device 22) to one of 32 Event_Status. 0000: map event source 26 to the input of Event_Status bit 0 0001: map event source 26 to the input of Event_Status bit 1 … 1111: map event source 26 to the input of Event_Status bit 31
SciMap_27	28:24	0000b	Mapping of USB_PME (device 20) to one of 32 Event_Status. 0000: map event source 27 to the input of Event_Status bit 0 0001: map event source 27 to the input of Event_Status bit 1 … 1111: map event source 27 to the input of Event_Status bit 31

SciMap7 - RW – 32 bits - [SMI_Reg: 5Ch]			
Field Name	**Bits**	**Default**	**Description**
SciMap_28	4:0	0000b	Mapping of GPP_PME (device 21, function 0) to one of 32 Event_Status. 0000: map event source 28 to the input of Event_Status bit 0 0001: map event source 28 to the input of Event_Status bit 1 … 1111: map event source 28 to the input of Event_Status bit 31
SciMap_29	12:8	0000b	Mapping of GPP_PME (device 21, function 1) to one of 32 Event_Status. 0000: map event source 29 to the input of Event_Status bit 0 0001: map event source 29 to the input of Event_Status bit 1 … 1111: map event source 29 to the input of Event_Status bit 31
SciMap_30	20:16	0000b	Mapping of GPP_PME (device 21, function 2) to one of 32 Event_Status. 0000: map event source 30 to the input of Event_Status bit 0 0001: map event source 30 to the input of Event_Status bit 1 … 1111: map event source 30 to the input of Event_Status bit 31
SciMap_31	28:24	0000b	Mapping of GPP_PME (device 21, function 3) to one of 32 Event_Status. 0000: map event source 7 to the input of Event_Status bit 0 0001: map event source 7 to the input of Event_Status bit 1 … 1111: map event source 7 to the input of Event_Status bit 31

SciMap8 - RW – 32 bits - [SMI_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_32	4:0	0000b	Mapping of GPP_HotPlug (device 21, function 0) to one of 32 Event_Status. 0000: map event source 32 to the input of Event_Status bit 0 0001: map event source 32 to the input of Event_Status bit 1 … 1111: map event source 32 to the input of Event_Status bit 31
SciMap_33	12:8	0000b	Mapping of GPP_HotPlug (device 21, function 1) to one of 32 Event_Status. 0000: map event source 33 to the input of Event_Status bit 0 0001: map event source 33 to the input of Event_Status bit 1 … 1111: map event source 33 to the input of Event_Status bit 31
SciMap_34	20:16	0000b	Mapping of GPP_HotPlug (device 21, function 2) to one of 32 Event_Status. 0000: map event source 34 to the input of Event_Status bit 0 0001: map event source 34 to the input of Event_Status bit 1 … 1111: map event source 34 to the input of Event_Status bit 31
SciMap_35	28:24	0000b	Mapping of GPP_HotPlug (device 21, function 3) to one of 32 Event_Status. 0000: map event source 35 to the input of Event_Status bit 0 0001: map event source 35 to the input of Event_Status bit 1 … 1111: map event source 35 to the input of Event_Status bit 31

SciMap9 - RW – 32 bits - [SMI_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_36	4:0	0000b	Mapping of HD_Audio_PME to one of 32 Event_Status. 0000: map event source 36 to the input of Event_Status bit 0 0001: map event source 36 to the input of Event_Status bit 1 … 1111: map event source 36 to the input of Event_Status bit 31
SciMap_37	12:8	0000b	Mapping of SATA0_PME to one of 32 Event_Status. 0000: map event source 37 to the input of Event_Status bit 0 0001: map event source 37 to the input of Event_Status bit 1 … 1111: map event source 37 to the input of Event_Status bit 31
SciMap_38	20:16	0000b	Mapping of SATA1_PME to one of 32 Event_Status. 0000: map event source 38 to the input of Event_Status bit 0 0001: map event source 38 to the input of Event_Status bit 1 … 1111: map event source 38 to the input of Event_Status bit 31

SciMap9 - RW – 32 bits - [SMI_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_39	28:24	0000b	Mapping of GEC_PME to one of 32 Event_Status. 0000: map event source 39 to the input of Event_Status bit 0 0001: map event source 39 to the input of Event_Status bit 1 … 1111: map event source 39 to the input of Event_Status bit 31

SciMap10 - RW – 32 bits - [SMI_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_40	4:0	0000b	Mapping of EC0_PME to one of 32 Event_Status. 0000: map event source 40 to the input of Event_Status bit 0 0001: map event source 40 to the input of Event_Status bit 1 … 1111: map event source 40 to the input of Event_Status bit 31
SciMap_41	12:8	0000b	Mapping of EC1_PME to one of 32 Event_Status. 0000: map event source 41 to the input of Event_Status bit 0 0001: map event source 41 to the input of Event_Status bit 1 … 1111: map event source 41 to the input of Event_Status bit 31
SciMap_42	20:16	0000b	Mapping of CIR_PME to one of 32 Event_Status. 0000: map event source 42 to the input of Event_Status bit 0 0001: map event source 42 to the input of Event_Status bit 1 … 1111: map event source 42 to the input of Event_Status bit 31
SciMap_43	28:24	0000b	Mapping of WAKE# pin to one of 32 Event_Status. 0000: map event source 43 to the input of Event_Status bit 0 0001: map event source 43 to the input of Event_Status bit 1 … 1111: map event source 43 to the input of Event_Status bit 31

SciMap11 - RW – 32 bits - [SMI_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
SciMap_44	4:0	0000b	Mapping of internal FAN/THERMAL event to one of 32 Event_Status. 0000: map event source 44 to the input of Event_Status bit 0 0001: map event source 44 to the input of Event_Status bit 1 … 1111: map event source 44 to the input of Event_Status bit 31
SciMap_45	12:8	0000b	Mapping of ASF Master Interrupt event to one of 32 Event_Status. 0000: map event source 45 to the input of Event_Status bit 0 0001: map event source 45 to the input of Event_Status bit 1 … 1111: map event source 45 to the input of Event_Status bit 31

SciMap11 - RW – 32 bits - [SMI_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
SciMap_46	20:16	0000b	Mapping of ASF slave Interrupt event to one of 32 Event_Status. 0000: map event source 46 to the input of Event_Status bit 0 0001: map event source 46 to the input of Event_Status bit 1 … 1111: map event source 46 to the input of Event_Status bit 31
SciMap_47	28:24	0000b	Mapping of SMBUS0 Interrupt event to one of 32 Event_Status. 0000: map event source 47 to the input of Event_Status bit 0 0001: map event source 47 to the input of Event_Status bit 1 … 1111: map event source 47 to the input of Event_Status bit 31

SciMap12 - RW – 32 bits - [SMI_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_48	4:0	0000b	Mapping of TWARN pin to one of 32 Event_Status. 0000: map event source 48 to the input of Event_Status bit 0 0001: map event source 48 to the input of Event_Status bit 1 … 1111: map event source 48 to the input of Event_Status bit 31
SciMap_49	12:8	0000b	Mapping of internal traffic monitor to one of 32 Event_Status. 0000: map event source 49 to the input of Event_Status bit 0 0001: map event source 49 to the input of Event_Status bit 1 … 1111: map event source 49 to the input of Event_Status bit 31
SciMap_50	20:16	0000b	Mapping of LLB# to one of the 32 Event_Status bits. 0000: map event source 50 to the input of Event_Status bit 0 0001: map event source 50 to the input of Event_Status bit 1 … 1111: map event source 50 to the input of Event_Status bit 31
SciMap_51	28:24	0000b	Mapping of PWRBTN status to one of the 32 Event_Status bits. 0000: map event source 50 to the input of Event_Status bit 0 0001: map event source 50 to the input of Event_Status bit 1 … 1111: map event source 50 to the input of Event_Status bit 31

SciMap13 - RW – 32 bits - [SMI_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_52	4:0	0000b	Mapping of PROHOT# pin to one of the 32 Event_Status bits. 0000: map event source 52 to the input of Event_Status bit 0 0001: map event source 52 to the input of Event_Status bit 1 … 1111: map event source 52 to the input of Event_Status bit 31

SciMap13 - RW – 32 bits - [SMI_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_53	12:8	0000b	Mapping of “HW assertion message from APU” to one of the 32 Event_Status bits. 0000: map event source 53 to the input of Event_Status bit 0 0001: map event source 53 to the input of Event_Status bit 1 … 1111: map event source 53 to the input of Event_Status bit 31
SciMap_54	20:16	0000b	Mapping of “SCI assertion message from APU” to one of the 32 Event_Status bits. 0000: map event source 54 to the input of Event_Status bit 0 0001: map event source 54 to the input of Event_Status bit 1 … 1111: map event source 54 to the input of Event_Status bit 31
SciMap_55	28:24	0000b	Mapping of RAS_event status to one of the 32 Event_Status bits. 0000: map event source 55 to the input of Event_Status bit 0 0001: map event source 55 to the input of Event_Status bit 1 … 1111: map event source 55 to the input of Event_Status bit 31

SciMap14 - RW – 32 bits - [SMI_Reg: 78h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_56	4:0	0000b	Mapping of XHC0 (USB3 controller 0) pin to one of the 32 Event_Status bits. 0000: map event source 56 to the input of Event_Status bit 0 0001: map event source 56 to the input of Event_Status bit 1 … 1111: map event source 56 to the input of Event_Status bit 31
SciMap_57	12:8	0000b	Mapping of XHC1 (USB3 controller 1) to one of the 32 Event_Status bits. 0000: map event source 57 to the input of Event_Status bit 0 0001: map event source 57 to the input of Event_Status bit 1 … 1111: map event source 57 to the input of Event_Status bit 31

SmiStatus0 - RW – 32 bits - [SMI_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Gevent0Status_event0	0	0b	Status of Gevent0; write 1 to clear it to 0.
Gevent1Status_event1	0	0b	Status of Gevent1; write 1 to clear it to 0.
Gevent2Status_event2	0	0b	Status of Gevent2; write 1 to clear it to 0.
Gevent3Status_event3	0	0b	Status of Gevent3; write 1 to clear it to 0.
Gevent4Status_event4	0	0b	Status of Gevent4; write 1 to clear it to 0.
Gevent5Status_event5	0	0b	Status of Gevent5; write 1 to clear it to 0.
Gevent6Status_event6	0	0b	Status of Gevent6; write 1 to clear it to 0.
Gevent7Status_event7	0	0b	Status of Gevent7; write 1 to clear it to 0.
Gevent8Status_event8	0	0b	Status of Gevent8; write 1 to clear it to 0.
Gevent9Status_event9	0	0b	Status of Gevent9; write 1 to clear it to 0.
Gevent10Status_event10	0	0b	Status of Gevent10; write 1 to clear it to 0.
Gevent11Status_event11	0	0b	Status of Gevent11; write 1 to clear it to 0.
Gevent12Status_event12	0	0b	Status of Gevent12; write 1 to clear it to 0.
Gevent13Status_event13	0	0b	Status of Gevent13; write 1 to clear it to 0.

SmiStatus0 - RW – 32 bits - [SMI_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Gevent14Status_event14	0	0b	Status of Gevent14; write 1 to clear it to 0.
Gevent15Status_event15	0	0b	Status of Gevent15; write 1 to clear it to 0.
Gevent16Status_event16	0	0b	Status of Gevent16; write 1 to clear it to 0.
Gevent17Status_event17	0	0b	Status of Gevent17; write 1 to clear it to 0.
Gevent18Status_event18	0	0b	Status of Gevent18; write 1 to clear it to 0.
Gevent19Status_event19	0	0b	Status of Gevent19; write 1 to clear it to 0.
Gevent20Status_event20	0	0b	Status of Gevent20; write 1 to clear it to 0.
Gevent21Status_event21	0	0b	Status of Gevent21; write 1 to clear it to 0.
Gevent22Status_event22	0	0b	Status of Gevent22; write 1 to clear it to 0.
Gevent23Status_event23	0	0b	Status of Gevent23; write 1 to clear it to 0.
Usbwakup0_event24	24	0b	Status of USB device 18 Pme; write 1 to clear it to 0.
Usbwakup1_event25	25	0b	Status of USB device 19 Pme; write 1 to clear it to 0.
Usbwakup2_event26	26	0b	Status of USB device 22 Pme; write 1 to clear it to 0.
Usbwakup3_event27	27	0b	Status of USB device 20 Pme; write 1 to clear it to 0.
FCHGppPme0_event28	28	0b	Status of FCH GPP(dev21, function0) PME; write 1 to clear it to 0.
FCHGppPme1_event29	29	0b	Status of FCH GPP(dev21, function1) PME; write 1 to clear it to 0.
FCHGppPme2_event30	30	0b	Status of FCH GPP(dev21, function2) PME; write 1 to clear it to 0.
FCHGppPme3_event31	31	0b	Status of FCH GPP(dev21, function3) PME; write 1 to clear it to 0.

SmiStatus1 - RW – 32 bits - [SMI_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
FCHGppHp_event32	0	0b	Status of FCH GPP(dev21, function0/1/2/3) HP; write 1 to clear it to 0.
Reserved	1	0b	
Reserved	2	0b	
Reserved	3	0b	
AzaliaPme_event36	4	0b	Status of FCH HD Audio PME; write 1 to clear it to 0.
SataGevent0_event37	5	0b	Status of FCH SataGevent0; write 1 to clear it to 0.
SataGevent1_event38	6	0b	Status of FCH SataGevent1; write 1 to clear it to 0.
GecPme_event39	7	0b	Status of FCH Gec Pme; write 1 to clear it to 0.
ECGevent0_event40	8	0b	Status of FCH ECGevent0; write 1 to clear it to 0.
ECGevent1_event41	9	0b	Status of FCH ECGevent1; write 1 to clear it to 0.
CIRPme_event42	10	0b	Status of FCH CIR Pme; write 1 to clear it to 0.
reserved	11	0b	
FanThermalGevent_event 44	12	0b	Status of FCH FanThermal; write 1 to clear it to 0.
ASFMasterIntr_event45	13	0b	Status of FCH ASF Master interrupt; write 1 to clear it to 0.
ASFSlaveIntr_event46	14	0b	Status of FCH ASF Slave interrupt; write 1 to clear it to 0.
SMBUS0_event47	15	0b	Status of FCH SMBUS0 Master interrupt; write 1 to clear it to 0.
TWARN_event48	16	0b	Status of FCH TWARN; write 1 to clear it to 0.
TrafficMonitorIntr_event49	17	0b	Status of FCH Traffic Monitor Interrupt; write 1 to clear it to 0.
iLLB_event50	18	0b	Status of iLLB# assertion; write 1 to clear it to 0.
PwrButton_event51	19	0b	Status of PwrButton (rising edge) writing 1 to clear it to 0.
ProcHot_event52	20	0b	Status of ProcHot event; write 1 to clear it to 0.
APUHwAssertion_event53	21	0b	Status of APU Hw assertion; write 1 to clear it to 0.
APUSciAssrtion_event54	22	0b	Status of NB SCI request; write 1 to clear it to 0.
Ras_event55	23	0b	Internal devices SERR error status; write 1 to clear it to 0.
Xhc0Pme_event56	24	0b	Status of XHC0 (dev 16, func 0) PME; write 1 to clear it to 0.
Xhc1Pme_event57	25	0b	Status of XHC1 (dev 16, func 1) PME; write 1 to clear it to 0.

SmiStatus2 - RW – 32 bits - [SMI_Reg:88h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved
Slp_Type_event65	1	0b	Status of writing Slp_Typ; write 1 to clear it to 0.
GecRomSmi_event66	2	0b	Status of Gec Shadow ram Smi request; write 1 to clear it to 0
iSata_Ahci_smi_event67	3	0b	Status of Sata AHCI Smi request; write 1 to clear it to 0
APUGppPme_event68	4	0b	Status of APU Gpp Pme message; write 1 to clear it to 0
APUGppHp_event69	5	0b	Status of APU HP message; write 1 to clear it to 0
Rtc_Irq_event70	6	0b	Status of Rtc IRQ; write 1 to clear it to 0
ACPITimer_event71	7	0b	Status of Acpi Pm timer rollover interrupt; write 1 to clear it to 0
GBL_RLS_event72	8	0b	Status of GBL event; write 1 to clear it to 0
BIOS_RLS_event73	9	0b	Status of BIOS_RLS; write 1 to clear it to 0
PWRBTN_event74	10	0b	Status of Power Button being pressed; write 1 to clear it to 0
SmiCmdPort_event75	11	0b	Status of Writing Smi Command Port; write 1 to clear it to 0
UsbSmi_event76	12	0b	Status of Usb Smi request; write 1 to clear it to 0
SerialIrqSMi_event77	13	0b	Status of Smi request from Serial IRQ; write 1 to clear it to 0
SMBUS0Intr_event78	14	0b	Status of SMBUS0 interrupt request; write 1 to clear it to 0
IMCSmi0_event79	15	0b	Status of IMC Smi request ; write 1 to clear it to 0
XhcErr_event80	16	0b	Status of XHC error; write 1 to clear it to 0
IntruderAlertSts_event81	17	0b	Status of Intruder Alert event; write 1 to clear it to 0
VBATLow_event82	18	0b	Status of VBAT low; write 1 to clear it to 0
ProtHot_event83	19	0b	Status of ProtHot event; write 1 to clear it to 0
PciSerr_event84	20	0b	Status of Serr assertion on Pci bus; write 1 to clear it to 0
FCHGppSerr0_event85	21	0b	SERR error from FCH GPP device 21, function 0; write 1 to clear it to 0
FCHGppSerr1_event86	22	0b	SERR error from FCH GPP device 21, function 1; write 1 to clear it to 0
FCHGppSerr2_event87	23	0b	SERR error from FCH GPP device 21, function 2; write 1 to clear it to 0
FCHGppSerr3_event88	24	0b	SERR error from FCH GPP device 21, function 3; write 1 to clear it to 0
ThermalTrip_event89	25	0b	Status of ThermalTrip event; write 1 to clear it to 0
Emulate64_event90	26	0b	Status of Emulation Io Port 60/64h; write 1 to clear it to 0
Usb_FLR_event91	27	0b	Status of Usb FLR event; write 1 to clear it to 0
Sata_FLR_event92	28	0b	Status of Sata FLR event; write 1 to clear it to 0
Az_FLR_event93	29	0b	Status of Azalia FLR event; write 1 to clear it to 0
Gec_FLR_event94	30	0b	Status of Gec FLR event; write 1 to clear it to 0
CmosEraseSts_event95	31	0b	Status of Cmos Erase event; write 1 to clear it to 0

SmiStatus3- RW – 32 bits - [SMI_Reg: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
IRQ0Trapping_event96	0	0b	Status of IRQ0 request; write 1 to clear it to 0
IRQ1Trapping_event97	1	0b	Status of IRQ1 request; write 1 to clear it to 0
IRQ2Trapping_event98	2	0b	Status of IRQ2 request; write 1 to clear it to 0
IRQ3Trapping_event99	3	0b	Status of IRQ3 request; write 1 to clear it to 0
IRQ4Trapping_event100	4	0b	Status of IRQ4 request; write 1 to clear it to 0
IRQ5Trapping_event101	5	0b	Status of IRQ5 request; write 1 to clear it to 0
IRQ6Trapping_event102	6	0b	Status of IRQ6 request; write 1 to clear it to 0
IRQ7Trapping_event103	7	0b	Status of IRQ7 request; write 1 to clear it to 0
IRQ8Trapping_event104	8	0b	Status of IRQ8 request; write 1 to clear it to 0
IRQ9Trapping_event105	9	0b	Status of IRQ9 request; write 1 to clear it to 0
IRQ10Trapping_event106	10	0b	Status of IRQ10 request; write 1 to clear it to 0
IRQ11Trapping_event107	11	0b	Status of IRQ11 request; write 1 to clear it to 0
IRQ12Trapping_event108	12	0b	Status of IRQ12 request; write 1 to clear it to 0
IRQ13Trapping_event109	13	0b	Status of IRQ13 request; write 1 to clear it to 0
IRQ14Trapping_event110	14	0b	Status of IRQ14 request; write 1 to clear it to 0
IRQ15Trapping_event111	15	0b	Status of IRQ15 request; write 1 to clear it to 0
IRQ16Trapping_event112	16	0b	Status of IRQ16 request; write 1 to clear it to 0
IRQ17Trapping_event113	17	0b	Status of IRQ17 request; write 1 to clear it to 0

SmiStatus3- RW – 32 bits - [SMI_Reg: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
IRQ18Trapping_event114	18	0b	Status of IRQ18 request; write 1 to clear it to 0
IRQ19Trapping_event115	19	0b	Status of IRQ19 request; write 1 to clear it to 0
IRQ20Trapping_event116	20	0b	Status of IRQ20 request; write 1 to clear it to 0
IRQ21Trapping_event117	21	0b	Status of IRQ21 request; write 1 to clear it to 0
IRQ22Trapping_event118	22	0b	Status of IRQ22 request; write 1 to clear it to 0
IRQ23Trapping_event119	23	0b	Status of IRQ23 request; write 1 to clear it to 0
VIn0Sts_event120	24	0b	Status of Vin0 event; write 1 to clear it to 0
VIn1Sts_event121	25	0b	Status of Vin1 event; write 1 to clear it to 0
VIn2Sts_event122	26	0b	Status of Vin2 event; write 1 to clear it to 0
VIn3Sts_event123	27	0b	Status of Vin3 event; write 1 to clear it to 0
VIn4Sts_event124	28	0b	Status of Vin4 event; write 1 to clear it to 0
VIn5Sts_event125	29	0b	Status of Vin5 event; write 1 to clear it to 0
VIn6Sts_event126	30	0b	Status of Vin6 event; write 1 to clear it to 0
VIn7Sts_event127	31	0b	Status of Vin7 event; write 1 to clear it to 0

SmiStatus4- RW – 32 bits - [SMI_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
Temp0Sts_event128	0	0b	Status of Temp0 event; write 1 to clear it to 0
Temp1Sts_event129	1	0b	Status of Temp1 event; write 1 to clear it to 0
Temp2Sts_event130	2	0b	Status of Temp2 event; write 1 to clear it to 0
Temp3Sts_event131	3	0b	Status of Temp3 event; write 1 to clear it to 0
Temp4Sts_event132	4	0b	Status of Temp4 event; write 1 to clear it to 0
FanIn0Sts_event133	5	0b	Status of FanIn0 event; write 1 to clear it to 0
FanIn1Sts_event134	6	0b	Status of FanIn1 event; write 1 to clear it to 0
FanIn2Sts_event135	7	0b	Status of FanIn2 event; write 1 to clear it to 0
FanIn3Sts_event136	8	0b	Status of FanIn3 event; write 1 to clear it to 0
FanIn4Sts_event137	9	0b	Status of FanIn4 event; write 1 to clear it to 0
Fake0Sts_event138	10	0b	Status of Fake0; write 1 to clear it to 0
Fake1Sts_event139	11	0b	Status of Fake1; write 1 to clear it to 0
Fake2Sts_event140	12	0b	Status of Fake2; write 1 to clear it to 0
CStateMsg_event141	13	0b	Status of C State Change message request; write 1 to clear it to 0
ShortTimer_event142	14	0b	Status of Short Timer Smi request; write 1 to clear it to 0
LongTimer_event143	15	0b	Status of Long Timer Smi request; write 1 to clear it to 0
AbSmiTrap_event144	16	0b	Status of AB Smi trapping request; write 1 to clear it to 0
SoftReset_event145	17	0b	Status of Soft reset request; write 1 to clear it to 0. The soft request can be: 1. cf9 pci reset 2. asf remote reset 3. sync_flood reset 4. Kbrst 5. watchdigtimer reset
PStateChange_event146	18	0b	Status of P State request; write 1 to clear it to 0
PStateChange_event147	19	0b	Status of P State request; write 1 to clear it to 0
IoTrapping0_event148	20	0b	Status of Io Trapping0 Smi request; write 1 to clear it to 0
IoTrapping1_event149	21	0b	Status of Io Trapping1 Smi request; write 1 to clear it to 0
IoTrapping2_event150	22	0b	Status of Io Trapping2 Smi request; write 1 to clear it to 0
IoTrapping3_event151	23	0b	Status of Io Trapping3 Smi request; write 1 to clear it to 0
MemTrapping0_event152	24	0b	Status of memory Trapping0 Smi request; write 1 to clear it to 0
MemTrapping1_event153	25	0b	Status of memory Trapping1 Smi request; write 1 to clear it to 0
MemTrapping2_event154	26	0b	Status of memory Trapping2 Smi request; write 1 to clear it to 0
MemTrapping3_event155	27	0b	Status of memory Trapping3 Smi request; write 1 to clear it to 0
CfgTrapping0_event156	28	0b	Status of Pci configuration cycle Trapping0 Smi request ; write 1 to clear it to 0

SmiStatus4- RW – 32 bits - [SMI_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
CfgTrapping1_event157	29	0b	Status of Pci configuration cycle Trapping1 Smi request; write 1 to clear it to 0
CfgTrapping2_event158	30	0b	Status of Pci configuration cycle Trapping2 Smi request; write 1 to clear it to 0
CfgTrapping3_event159	31	0b	Status of Pci configuration cycle Trapping3 Smi request; write 1 to clear it to 0

SmiPointer - R – 8 bits - [SMI_Reg: 94h]			
Field Name	**Bits**	**Default**	**Description**
SmiSciSource	0	0b	Indicates whether the SMI source is from SMISCI.
SmiStatusSource0	1	0b	Indicates whether the SMI source is from SmiStatus0[31:0] if the corresponding SMI enable is selected.
SmiStatusSource1	2	0b	Indicates whether the SMI source is from SmiStatus1[31:0] if the corresponding SMI enable is selected.
SmiStatusSource2	3	0b	Indicates whether the SMI source is from SmiStatus2[31:0] if the corresponding SMI enable is selected.
SmiStatusSource3	4	0b	Indicate whether the SMI source is from SmiStatus3[31:0] if the corresponding SMI enable is selected.
SmiStatusSource4	5	0b	Indicate whether the SMI source is from SmiStatus4[31:0] if the corresponding SMI enable is selected.
Reserved	15:6	0	Reserved.

Note: This register is meant as a faster mechanism to locate the SMI source. BIOS can examine this register to find out the SMI source instead of reading SmiStatus0 through SmiStatus4 individually

There are two SMI timers: the short timer runs at 1us unit time and the long timer is 1ms unit time. SMI_Reg:96h is actually made up of two sets of registers depending on the setting of PMIO_98[29]. When PMIO_98[29]=0, it is selecting the control registers for the short timer. When PMIO_98[29]=1, it is selecting the control registers for the long timer.

SmiShortTimer – R/W – 16 bits - [SMI_Reg: 96h]			
Field Name	**Bits**	**Default**	**Description**
SmiTimerCount	14:0	0000h	Actual timer duration = (SmiTimerCount + 1) * 2 us
TimerEn	15	0b	Enable the SMI short Timer or long timer, which is selected by SmiTimerEn (PMIO_98[29]). 0 = Disable 1 = Enable
***Note:** This register 96h can be either “SmiShortTimer” or “SmiLongTimer,” depending on the select bit “SmiTimerSel” in SMI_Reg 98[29]. The default setting (SmiTimerSel=0) selects this register as “SmiShortTimer”; software needs to set the “SmiTimerSel=1” to select this register as “SmiLongTimer”.			

SmiLongTimer – R/W – 16 bits - [SMI_Reg: 96h]			
Field Name	**Bits**	**Default**	**Description**
SmiTimerCount	14:0	0000h	Actual timer duration = SmiTimerCount + 1 unit (ms)
TimerEn	15	0b	Enable the SMI short Timer or long timer, which is selected by SmiTimerEn (PMIO_98[29]). 0 = Disable 1 = Enable
***Note:** This register 96h can be either “SmiShortTimer” or “SmiLongTimer,” depending on the select bit “SmiTimerSel” in SMI_Reg 98[29]. The default setting (SmiTimerSel=0) selects this register as “SmiShortTimer”; software needs to set the “SmiTimerSel=1” to select this register as “SmiLongTimer”.			

There are 24 trigger bits for 24 Gevents.

SmiTrig0 - RW – 8/16/32 bits - [SMI_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
SmiTrig0	0	1b	This defines the trigger mode for SmiStatus0[23:0]. Note these are different from SciTrig 0: Active low 1: Active high
SmiTrig1	1	1b	0: Active low 1: Active high
SmiTrig2	2	1b	0: Active low 1: Active high
SmiTrig3	3	1b	0: Active low 1: Active high
SmiTrig4	4	1b	0: Active low 1: Active high
SmiTrig5	5	1b	0: Active low 1: Active high
SmiTrig6	6	1b	0: Active low 1: Active high
SmiTrig7	7	1b	0: Active low 1: Active high
SmiTrig8	8	1b	0: Active low 1: Active high
SmiTrig9	9	1b	0: Active low 1: Active high
SmiTrig10	10	1b	0: Active low 1: Active high
SmiTrig11	11	1b	0: Active low 1: Active high
SmiTrig12	12	1b	0: Active low 1: Active high
SmiTrig13	13	1b	0: Active low 1: Active high
SmiTrig14	14	1b	1: Active high 0: Active low
SmiTrig15	15	1b	0: Active low 1: Active high
SmiTrig16	16	1b	0: Active low 1: Active high
SmiTrig17	17	1b	0: Active low 1: Active high
SmiTrig18	18	1b	0: Active low 1: Active high
SmiTrig19	19	1b	0: Active low 1: Active high
SmiTrig20	20	1b	0: Active low 1: Active high
SmiTrig21	21	1b	0: Active low 1: Active high
SmiTrig22	22	1b	0: Active low 1: Active high
SmiTrig23	23	1b	0: Active low 1: Active high
TrappingIRQonPIC	24	1b	SMI will be generated when 0: Trapping Irq0 ~ 15 of IoApIC 1: Trapping Irq0 ~ 15 of PIC
FakeSts0	25	1b	Program the value to emulate an SMI input event.
FakeSts1	26	1b	Program the value to emulate an SMI input event.

SmiTrig0 - RW – 8/16/32 bits - [SMI_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
FakeSts2	27	1b	Program the value to emulate an SMI input event.
Eos	28	1b	Set to1 to allow SMI to be sent out to CPU; otherwise SMI is blocked.
SmiTimerSel	29	0b	0: Selects the SMI_Reg 96h to be SmiShortTimer register. 1: Selects the SMI_Reg 96h to be SmiLongTimer register.
SmiEnB	31	1b	Enable SMI function. 0: Enable 1: Disable

There are 24 trigger bits for the 24 IRQs

SmiTrig1 - RW – 8/16/32 bits - [SMI_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
SmiIrq0Trig	0	0b	0: Active low 1: Active high
SmiIrq1Trig	1	0b	0: Active low 1: Active high
SmiIrq2Trig	2	0b	0: Active low 1: Active high
SmiIrq3Trig	3	0b	0: Active low 1: Active high
SmiIrq4Trig	4	0b	0: Active low 1: Active high
SmiIrq5Trig	5	0b	0: Active low 1: Active high
SmiIrq6Trig	6	0b	0: Active low 1: Active high
SmiIrq7Trig	7	0b	0: Active low 1: Active high
SmiIrq8Trig	8	0b	0: Active low 1: Active high
SmiIrq9Trig	9	0b	0: Active low 1: Active high
SmiIrq10Trig	10	0b	0: Active low 1: Active high
SmiIrq11Trig	11	0b	0: Active low 1: Active high
SmiIrq12Trig	12	0b	0: Active low 1: Active high
SmiIrq13Trig	13	0b	0: Active low 1: Active high
SmiIrq14Trig	14	0b	0: Active low 1: Active high
SmiIrq15Trig	15	0b	0: Active low 1: Active high
SmiIrq16Trig	16	0b	0: Active low 1: Active high
SmiIrq17Trig	17	0b	0: Active low 1: Active high
SmiIrq18Trig	18	0b	0: Active low 1: Active high
SmiIrq19Trig	19	0b	0: Active low 1: Active high
SmiIrq20Trig	20	0b	0: Active low 1: Active high
SmiIrq21Trig	21	0b	0: Active low 1: Active high

SmiTrig1 - RW – 8/16/32 bits - [SMI_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
SmiIrq22Trig	22	0b	0: Active low 1: Active high
SmiIrq23Trig	23	0b	0: Active low 1: Active high

SMI_Reg 0xA0 through 0xA7 specify the control mechanism for SMI source 0 through 159 (please see SMI_Reg 0x80 through 0x90). Each control takes up 2 bits to control the behavior for each source.

SmiControl0 - RW – 8/16/32 bits - [SMI_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_0	1:0	00b	Control for GEVENT0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_1	3:2	00b	Control for GEVENT1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_2	5:4	00b	Control for GEVENT2 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_3	7:6	00b	Control for GEVENT3 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_4	9:8	00b	Control for GEVENT4 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_5	11:0	00b	Control for GEVENT5 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_6	13:12	00b	Control for GEVENT6 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_7	15:14	00b	Control for GEVENT7 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_8	17:16	00b	Control for GEVENT8 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl0 - RW – 8/16/32 bits - [SMI_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_9	19:18	00b	Control for GEVENT9 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_10	21:20	00b	Control for GEVENT10 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_11	23:22	00b	Control for GEVENT11 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_12	25:24	00b	Control for GEVENT12 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_13	27:26	00b	Control for GEVENT13 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_14	29:28	00b	Control for GEVENT14 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_15	31:30	00b	Control for GEVENT15 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl1 - RW – 8/16/32 bits - [SMI_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_16	1:0	00b	Control for GEVENT16 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_17	3:2	00b	Control for GEVENT17 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_18	5:4	00b	Control for GEVENT18 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl1 - RW – 8/16/32 bits - [SMI_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_19	7:6	00b	Control for GEVENT19 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_20	9:8	00b	Control for GEVENT20 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_21	11:0	00b	Control for GEVENT21 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_22	13:12	00b	Control for GEVENT22 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_23	15:14	00b	Control for GEVENT23 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_24	17:16	00b	Control for USB_PME (device 18) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_25	19:18	00b	Control for USB_PME (device 19) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_26	21:20	00b	Control for USB_PME (device 22) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_27	23:22	00b	Control for USB_PME (device 20) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_28	25:24	00b	Control for GPP_PME (device 21, function0) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_29	27:26	00b	Control for GPP_PME (device 21, function1) 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl1 - RW – 8/16/32 bits - [SMI_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_30	29:28	00b	Control for GPP_PME (device 21, function2) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_31	31:30	00b	Control for GPP_PME (device 21, function3) 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl2 - RW – 8/16/32 bits - [SMI_Reg: A8h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_32	1:0	00b	Control for GPP_HotPlug (device 21, function 0) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_33	3:2	00b	Control for GPP_HotPlug (device 21, function 1) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_34	5:4	00b	Control for GPP_HotPlug (device 21, function 2) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_35	7:6	00b	Control for GPP_HotPlug (device 21, function 3) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_36	9:8	00b	Control for PME frpm HD Audio 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_37	11:0	00b	Control for Sata Gevent0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_38	13:12	00b	Control for Sata Gevent1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_39	15:14	00b	Control for Gec Pme 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl2 - RW – 8/16/32 bits - [SMI_Reg: A8h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_40	17:16	00b	Control for IMC Gevent0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_41	19:18	00b	Control for IMC Gevent1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_42	21:20	00b	Control for CIR PME 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_43	23:22	00b	Control for Wak# pin 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_44	25:24	00b	Control for FanThermal Gevent 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_45	27:26	00b	Control for ASF Master interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_46	29:28	00b	Control for ASF Slave interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_47	31:30	00b	Control for SMBUS0 interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl3 - RW – 8/16/32 bits - [SMI_Reg: ACh]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_48	1:0	00b	Control for TWARN# 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_49	3:2	00b	Control for internal Traffic monitor interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl3 - RW – 8/16/32 bits - [SMI_Reg: ACh]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_50	5:4	00b	Control for iLLB# 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_51	7:6	00b	Control for Power button event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_52	9:8	00b	Control for ProcHot event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_53	11:10	00b	Control for APU hw assertion 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_54	13:12	00b	Control for APU SCI assertion 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_55	15:14	00b	Control for RAS event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_56	17:16	00b	Control for xhc0 event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_57	19:18	00b	Control for xhc1 event 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl4 - RW – 8/16/32 bits - [SMI_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_65	3:2	00b	Control for writting SLP_TYP to put the system in S state. 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_66	5:4	00b	Control for GEC shodows rom write 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl4 - RW – 8/16/32 bits - [SMI_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_67	7:6	00b	Control for Sata AHCI event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_68	9:8	00b	Control for APU Gpp PME 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_69	11:10	00b	Control for APU Gpp Hotplug 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_70	13:12	00b	Control for rtc IRQ 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_71	15:14	00b	Control for Pm timer rollerover 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_72	17:16	00b	Control for writing GBL_RLS 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_73	19:18	00b	Control for writing BIOS_RLS 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_74	21:20	00b	Control for power botton being pressed 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_75	23:22	00b	Control for writing Smi command port 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_76	25:24	00b	Control for Usb Smi request 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_77	27:26	00b	Control for Smi request form serial Irq 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl4 - RW – 8/16/32 bits - [SMI_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_78	29:28	00b	Control for SMBUS0 interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_79	31:30	00b	Control for IMC Smi request0 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl5 - RW – 8/16/32 bits - [SMI_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_80	1:0	00b	Control for IMC Smi request1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_81	3:2	00b	Control for Intruder event. 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_82	5:4	00b	Control for VBAT low 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_83	7:6	00b	Control for ProcHot 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_84	9:8	00b	Control for SERR# 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_85	11:10	00b	Control for FCH GPP Serr#(device 21, function 0) 01: SMI 10: NMI 11: IRQ13
SmiControl_86	13:12	00b	Control for FCH GPP Serr#(device 21, function 1) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_87	15:14	00b	Control for FCH GPP Serr#(device 21, function 2) 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl5 - RW – 8/16/32 bits - [SMI_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_88	17:16	00b	Control for FCH GPP Serr#(device 21, function 3) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_89	19:18	00b	Control for ThermalTrip# assertion 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_90	21:20	00b	Control for Emulation64 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_91	23:22	00b	Control for Usb FLR 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_92	25:24	00b	Control for Sata FLR 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_93	27:26	00b	Control for HD audio FLR 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_94	29:28	00b	Control for Gec FLR 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_95	31:30	00b	Control for Cmos Erase 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl6 - RW – 8/16/32 bits - [SMI_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_96	1:0	00b	Control for Irq0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_97	3:2	00b	Control for Irq1 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl6 - RW – 8/16/32 bits - [SMI_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_98	5:4	00b	Control for Irq2. 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_99	7:6	00b	Control for Irq3 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_100	9:8	00b	Control for Irq4 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_101	11:10	00b	Control for Irq5 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_102	13:12	00b	Control for Irq6 01: SMI 10: NMI 11: IRQ13
SmiControl_103	15:14	00b	Control for Irq7 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_104	17:16	00b	Control for Irq8 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_105	19:18	00b	Control for Irq9 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_106	21:20	00b	Control for Irq10 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_107	23:22	00b	Control for Irq11 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_108	25:24	00b	Control for Irq12 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_109	27:26	00b	Control for Irq13 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl6 - RW – 8/16/32 bits - [SMI_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_110	29:28	00b	Control for Irq14 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_111	31:30	00b	Control for Irq15 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl7 - RW – 8/16/32 bits - [SMI_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_112	1:0	00b	Control for Irq16 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_113	3:2	00b	Control for Irq17 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_114	5:4	00b	Control for Irq18 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_115	7:6	00b	Control for Irq19 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_116	9:8	00b	Control for Irq20 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_117	11:10	00b	Control for Irq21 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_118	13:12	00b	Control for Irq22 01: SMI 10: NMI 11: IRQ13
SmiControl_119	15:14	00b	Control for Irq23 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl7 - RW – 8/16/32 bits - [SMI_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_120	17:16	00b	Control for Vin0 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_121	19:18	00b	Control for Vin1 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_122	21:20	00b	Control for Vin2 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_123	23:22	00b	Control for Vin3 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_124	25:24	00b	Control for Vin4 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_125	27:26	00b	Control for Vin5 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_126	29:28	00b	Control for Vin6 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_127	31:30	00b	Control for Vin7 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl8 - RW – 8/16/32 bits - [SMI_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_128	1:0	00b	Control for Internal Temp out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_129	3:2	00b	Control for Temp0 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl8 - RW – 8/16/32 bits - [SMI_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_130	5:4	00b	Control for Temp1 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_131	7:6	00b	Control for Temp2 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_132	9:8	00b	Control for Temp3 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_133	11:10	00b	Control for Fan Tach 0 too slow event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_134	13:12	00b	Control for Fan1 Tach too slow event 01: SMI 10: NMI 11: IRQ13
SmiControl_135	15:14	00b	Control for Fan2 Tach too slow event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_136	17:16	00b	Control for Fan3 Tach too slow event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_137	19:18	00b	Control for Fan4 Tach too slow event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_138	21:20	00b	Control for FakeSts0 00: Disable 01: SMI 10: NMI 11: IRQ13 Note: FakeSts0 defined in PMIO can be programmed to generate SMI/NMI/IRQ13 specified in those two bits.
SmiControl_139	23:22	00b	Control for FakeSts1 00: Disable 01: SMI 10: NMI 11: IRQ13 Note: FakeSts1 defined in PMIO can be programmed to generate SMI/NMI/IRQ13 specified in those two bits.

SmiControl8 - RW – 8/16/32 bits - [SMI_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_140	25:24	00b	Control for FakeSts2 00: Disable 01: SMI 10: NMI 11: IRQ13 Note: FakeSts2 defined in PMIO can be programmed to generate SMI/NMI/IRQ13 specified in those two bits.
SmiControl_141	27:26	00b	Control for C state Message 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_142	29:28	00b	Control for Short timer 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_143	31:30	00b	Control for Long timer 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl9 - RW – 8/16/32 bits - [SMI_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_144	1:0	00b	Control for AB Smi trapping request 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_145	3:2	00b	Control for P state message 0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_146	5:4	00b	Control for P state message 1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_147	7:6	00b	Control for P state message 2 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_148	9:8	00b	Control for Io trapping 0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_149	11:10	00b	Control for Io trapping 1 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl9 - RW – 8/16/32 bits - [SMI_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_150	13:12	00b	Control for Io trapping 2 01: SMI 10: NMI 11: IRQ13
SmiControl_151	15:14	00b	Control for Io trapping 3 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_152	17:16	00b	Control for memory trapping 0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_153	19:18	00b	Control for memory trapping 1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_154	21:20	00b	Control for memory trapping 2 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_155	23:22	00b	Control for memory trapping 3 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_156	25:24	00b	Control for configuration cycle trapping 0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_157	27:26	00b	Control for configuration cycle trapping 1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_158	29:28	00b	Control for configuration cycle trapping 2 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_159	31:30	00b	Control for configuration cycle trapping 3 00: Disable 01: SMI 10: NMI 11: IRQ13

IoTrapping0 - RW – 8/16 bits - [SMI_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
IoTrapping0	15:0	00b	Specify the I/O address which causes SMI event.

IoTrapping1 - RW – 8/16 bits - [SMI_Reg: CAh]			
Field Name	**Bits**	**Default**	**Description**
IoTrapping1	15:0	00b	Specify the I/O address which causes SMI event.

IoTrapping2 - RW – 8/16 bits - [SMI_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
IoTrapping2	15:0	00b	Specify the I/O address which causes SMI event.

IoTrapping3 - RW – 8/16 bits - [SMI_Reg: CEh]			
Field Name	**Bits**	**Default**	**Description**
IoTrapping3	15:0	00b	Specify the I/O address which causes SMI event.

MemTrapping0 - RW – 8/16/32 bits - [SMI_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
MemTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
MemRdOvrEn	1	0b	Set to 1 to force read data to be replaced by MemRdOvrData0.
MemTrapping	31:2	00000000h	Specify the 30-bit memory address which causes SMI event; lowest 2 bits are ignored.

MemRdOvrData0 - RW – 8/16/32 bits - [SMI_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
MemRdOvrData	31:0	00h	The 32 bit data is used as the return data when the memory read trapping is enabled in MemTrapping0. with MemRdOvrEn = 1

MemTrapping1 - RW – 8/16/32 bits - [SMI_Reg: D8h]			
Field Name	**Bits**	**Default**	**Description**
MemTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
MemRdOvrEn	1	0b	Set to 1 to force read data to be replaced by MemRdOvrData1.
MemTrapping	31:2	00000000h	Specify the 30-bit memory address which causes SMI event; lowest 2 bits are ignored.

MemRdOvrData1 - RW – 8/16/32 bits - [SMI_Reg: DCh]			
Field Name	**Bits**	**Default**	**Description**
MemRdOvrData	31:0	00h	The 32 bit data is used as the return data when the memory read trapping is enabled in MemTrapping1. with MemRdOvrEn = 1.

MemTrapping2 - RW – 8/16/32 bits - [SMI_Reg: E0h]			
Field Name	**Bits**	**Default**	**Description**
MemTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
MemRdOvrEn	1	0b	Set to 1 to force read data to be replaced by MemRdOvrData2.
MemTrapping	31:2	00000000h	Specify the 30-bit memory address which causes SMI event; lowest 2 bits are ignored.

MemRdOvrData2 - RW – 8/16/32 bits - [SMI_Reg: E4h]			
Field Name	**Bits**	**Default**	**Description**
MemRdOvrData	31:0	00h	The 32 bit data is used as the return data when the memory read trapping is enabled in MemTrapping2. with MemRdOvrEn = 1

MemTrapping3 - RW – 8/16/32 bits - [SMI_Reg: E8h]			
Field Name	**Bits**	**Default**	**Description**
MemTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
MemRdOvrEn	1	0b	Set to 1 to force read data to be replaced by MemRdOvrData3.
MemTrapping	31:2	00000000h	Specify the 30-bit memory address which causes SMI event; lowest 2 bits are ignored.

MemRdOvrData3 - RW – 8/16/32 bits - [SMI_Reg: ECh]			
Field Name	**Bits**	**Default**	**Description**
MemRdOvrData	31:0	00h	The 32 bit data is used as the return data when the memory read trapping is enabled in MemTrapping3. with MemRdOvrEn = 1

CfgTrapping0 - RW – 8/16/32 bits - [SMI_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
CfgTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
IoTrappingRw0	1	0b	0: Trap on I/O read access on the address specified in IoTrappingAdr0 1: Trap on I/O write access on the address specified in IoTrappingAdr0
CfgTrapping	31:2	00000000h	Specify the I/O address which causes SMI event.

CfgTrapping1 - RW – 8/16/32 bits - [SMI_Reg: F4h]			
Field Name	**Bits**	**Default**	**Description**
CfgTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
IoTrappingRw1	1	0b	0: trap on I/O read access on the address specified in IoTrappingAdr1 1: trap on I/O write access on the address specified in IoTrappingAdr1
CfgTrapping	31:2	00000000h	Specify the I/O address which causes SMI event.

CfgTrapping2 - RW – 8/16/32 bits - [SMI_Reg: F8h]			
Field Name	**Bits**	**Default**	**Description**
CfgTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
IoTrappingRw2	1	0b	0: Trap on Io read access on the address specified in IoTrappingAdr2 1: Trap on Io write access on the address specified in IoTrappingAdr2
CfgTrapping	31:2	00000000h	Specify the I/O address which causes SMI event.

CfgTrapping3 - RW – 8/16/32 bits - [SMI_Reg: FCh]			
Field Name	**Bits**	**Default**	**Description**
CfgTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
IoTrappingRw3	1	0b	0: Trap on Io read access on the address specified in IoTrappingAdr3 1: Trap on Io write access on the address specified in IoTrappingAdr3
CfgTrapping	31:2	00000000h	Specify the I/O address which causes SMI event.

3.6 GPIO Registers

GPIO registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from “AcpiMMioAddr” + 0x100 to “AcpiMMioAddr” + 0x1FF.

The base address “AcpiMMioAddr” is defined in PM_Reg 0x24, with the default base address at “FED8_0000”.

The GPIO registers are used to control the GPIO pin statuses. Each GPIO pin has one register associated with it: the pin GPIO<N> (where the N is in the range from 0 ~ N, but not all numbers exist; consult related databook for the full numbers) maps to the register offset <NNh>, where “NNh” is the hexadecimal of number N.

The GPIO registers also control the GEvent pins. The GEvent<X> pins (where X is in the range of 0 ~ 23) map to the offset range 60h ~ 77h (or 96 ~ 119 in decimal). That means the register GPIO60 controls pin GEvent0, register GPIO61 controls GEvent1, and so on.

Gpio<N> – R/W 8 bits - [Gpio_Reg: NNh]			
Field Name	**Bits**	**Default**	**Description**
OwnedByIMC	0	0b	This bit can only be written by IMC. If this bit is set, only IMC can write to bits[6:2] and bit 1 can no longer be written by host. This bit is always sticky.
OwnedByHost	1	0b	This bit can only be written by host (BIOS). If this bit is set, only host can write to bits[6:2] and bit 0 can no longer be written by IMC. This bit is always sticky.
Sticky	2	0b	If set, bits[6:3]are sticky. If cleared, bits[6:3] are reset back to default values whenever a reset occurs. This will allow every GPIO to be sticky or non-sticky. 0: bits[6:3] can be reloaded to the default value on pci reset 1: bits[6:3] can be reloaded to the default value on RsmRst And SYS_RST#
PullUpB	3	0b	0: Pull-up enable 1: Pull-up disabled
PullDown	4	0b	0: Pull down disabled 1: Pull down enabled
GpioOutEnB	5	1b	0: Output enable 1: output disable
GpioOut	6	0b	Output state when GpioOutEnableB is enabled
GpioIn	7	0b	Read only – current pin state

3.7 IoMux Registers

IoMux registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from “AcpiMMioAddr” + 0xD00 to “AcpiMMioAddr” + 0xDFF.

The base address “AcpiMMioAddr” is defined in PM_reg x24, with the default base address at “FED8_0000.”

The IoMux register is used to select the function for multi-function IO pins. For example, the pin “AD0/GPIO0” is a multi-function pin that can perform either the “AD0” function or “GPIO0” function. The first part of the pin name indicates the default function, the second part indicates the second function, and so on.

Bolton has GPIO pins ranging from GPIO0 to GPIO228, mapped to IoMux registers IoMux00 to IoMuxE4 (“00” and “E4” are hexadecimal values). The IoMux registers also control the function selection for GEvent pins, with GEvent0~ GEvent23 mapped to GPIO96 ~ GPIO119.

IoMux<N>-Gpio<X> – R/W 8 bits - [IoMux_Reg: <N>h]			
Field Name	**Bits**	**Default**	**Description**
IOMux – GPIO<X>	1:0	00b	Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3
Reserved	7:2	000000b	Reserved
***Note:** <N> denotes number in hexadecimal: 00h ~ E4h. <X> denotes number in decimal: 0 ~ 228.			

3.7.1 IoMux Registers / Multifuction Pin Definitions

IoMux Register	Value	Function
IoMux00	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD0. When PCIBridge is disabled, then it is configured as GPIO00
IoMux01	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD1. When PCIBridge is disabled, then it is configured as GPIO01
IoMux02	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD2. When PCIBridge is disabled, then it is configured as GPIO02
IoMux03	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD3. When PCIBridge is disabled, then it is configured as GPIO03
IoMux04	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD4. When PCIBridge is disabled, then it is configured as GPIO04
IoMux05	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD5. When PCIBridge is disabled, then it is configured as GPIO05
IoMux06	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD6. When PCIBridge is disabled, then it is configured as GPIO06
IoMux07	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD7. When PCIBridge is disabled, then it is configured as GPIO07
IoMux08	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD8. When PCIBridge is disabled, then it is configured as GPIO08
IoMux09	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD9. When PCIBridge is disabled, then it is configured as GPIO09
IoMux0A	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD10. When PCIBridge is disabled, then it is configured as GPIO10
IoMux0B	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD11. When PCIBridge is disabled, then it is configured as GPIO11
IoMux0C	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD12. When PCIBridge is disabled, then it is configured as GPIO12

IoMux Register	Value	Function
IoMux0D	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD13. When PCIBridge is disabled, then it is configured as GPIO13
IoMux0E	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD14. When PCIBridge is disabled, then it is configured as GPIO14
IoMux0F	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD15. When PCIBridge is disabled, then it is configured as GPIO15
IoMux10	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD16. When PCIBridge is disabled, then it is configured as GPIO16
IoMux11	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD17. When PCIBridge is disabled, then it is configured as GPIO17
IoMux12	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD18. When PCIBridge is disabled, then it is configured as GPIO18
IoMux13	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD19. When PCIBridge is disabled, then it is configured as GPIO19
IoMux14	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD20. When PCIBridge is disabled, then it is configured as GPIO20
IoMux15	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD21. When PCIBridge is disabled, then it is configured as GPIO21
IoMux16	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD22. When PCIBridge is disabled, then it is configured as GPIO22
IoMux17	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD23. When PCIBridge is disabled, then it is configured as GPIO23
IoMux18	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD24. When PCIBridge is disabled, then it is configured as GPIO24
IoMux19	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD25. When PCIBridge is disabled, then it is configured as GPIO25
IoMux1A	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD26. When PCIBridge is disabled, then it is configured as GPIO26
IoMux1B	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD27. When PCIBridge is disabled, then it is configured as GPIO27
IoMux1C	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD28. When PCIBridge is disabled, then it is configured as GPIO28
IoMux1D	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD29. When PCIBridge is disabled, then it is configured as GPIO29
IoMux1E	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD30. When PCIBridge is disabled, then it is configured as GPIO30
IoMux1F	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always AD31. When PCIBridge is disabled, then it is configured as GPIO31
IoMux20	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always INTE#. When PCIBridge is disabled, then it is configured as GPIO32
IoMux21	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always INTF#. When PCIBridge is disabled, then it is configured as GPIO33
IoMux22	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always INTG#. When PCIBridge is disabled, then it is configured as GPIO34
IoMux23	-	When PCIBridge is enabled (PMIO_EA[0]=0), this pin is always INTH#. When PCIBridge is disabled, then it is configured as GPIO35
IoMux24	00 01 10 11	PCICLK1 GPIO36 GPIO36 GPIO36
IoMux25	00 01 10 11	PCICLK2 GPIO37 GPIO37 GPIO37

IoMux Register	Value	Function
IoMux26	00	PCICLK3
	01	GPIO38
	10	GPIO38
	11	GPIO38
IoMux27	00	PCICLK4
	01	OSC (14MHz output)
	10	GPIO39
	11	GPIO39
IoMux28	00	PCIREQ1#
	01	GPIO40
	10	GPIO40
	11	GPIO40
IoMux29	00	PCIREQ2#
	01	CLKREQ8#
	10	GPIO41
	11	GPIO41
IoMux2A	00	PCIREQ3#
	01	CLKREQ5#
	10	SATA_IS6
	11	GPIO42
IoMux2B	-	SCL0/GPIO43 is configured as SCL0 when (PMIO_2E) Smbus0Sel[1:0] are set to 00b; otherwise, it is configured as GPIO43
IoMux2C	00	PCIGNT1#
	01	GPIO44
	10	GPIO44
	11	GPIO44
IoMux2D	00	PCIGNT2#
	01	GPIO45
	10	GPIO45
	11	GPIO45
IoMux2E	00	PCIGNT3#
	01	CLKREQ7#
	10	SATA_IS7
	11	GPIO46
IoMux2F	-	SDA0/GPIO47 is configured as SDA0 when (PMIO_2E) Smbus0Sel[1:0] are set to 00b; otherwise, it is configured as GPIO47
IoMux30	00	SERIRQ#
	01	GPIO48
	10	GPIO48
	11	GPIO48
IoMux31	00	LDRQ1#
	01	CLKREQ6#
	10	GPIO49
	11	GPIO49
IoMux32		SMARTVOLT1/SATA_IS2#/GPIO50 becomes SMARTVOLT1 when SmartVolt1Enable (PMIO_3C[7]) is set. Otherwise, it is configured by IoMux32:
	00	GPIO50
	01	SATA_IS2
	10	GPIO50
	11	GPIO50
IoMux33		SMARTVOLT2/SHUTDOWN#/GPIO51 becomes SMARTVOLT2 when SmartVolt2Enable (PMIO_40[7]) is set. Otherwise, it is configured by IoMux33:
	00	GPIO51
	01	SHUTDOWN#
	10	GPIO51
	11	GPIO51

IoMux Register	Value	Function
IoMux34	00	FANOUT0
	01	GPIO52
	10	GPIO52
	11	GPIO52
IoMux35	00	FANOUT1
	01	GPIO53
	10	GPIO53
	11	GPIO53
IoMux36	00	FANOUT2
	01	GPIO54
	10	GPIO54
	11	GPIO54
IoMux37	00	Tristate
	01	FANOUT3
	10	SD Power Control
	11	GPIO55
IoMux38	00	FANIN0
	01	GPIO56
	10	GPIO56
	11	GPIO56
IoMux39	00	FANIN1
	01	GPIO57
	10	GPIO57
	11	GPIO57
IoMux3A	00	FANIN2
	01	GPIO58
	10	GPIO58
	11	GPIO58
IoMux3B	00	SATA_IS5
	01	FANIN3
	10	GPIO59
	11	GPIO59
IoMux3C	00	CLKREQ0#
	01	SATA_IS3
	10	GPIO60
	11	GPIO60
IoMux3D	00	CLKREQ1#
	01	FANOUT4
	10	GPIO61
	11	GPIO61
IoMux3E	00	CLKREQ2#
	01	FANIN4
	10	GPIO62
	11	GPIO62
IoMux3F	00	CLKREQ3#
	01	SATA_IS1
	10	GPIO63
	11	GPIO63
IoMux40	00	CLKREQ4#
	01	SATA_IS0
	10	GPIO64
	11	GPIO64

IoMux Register	Value	Function
IoMux41	00	CLKREQG#
	01	GPIO65
	10	GPIO65
	11	Ext_14M_OscIn
IoMux42	00	SPKR
	01	GPIO66
	10	GPIO66
	11	GPIO66
IoMux43	00	SATA_ACT#
	01	GPIO67
	10	GPIO67
	11	GPIO67
IoMux44	00	HSYNC
	01	GPIO68
	10	GPIO68
	11	GPIO68
IoMux45	00	VSYNC
	01	GPIO69
	10	GPIO69
	11	GPIO69
IoMux46	00	VGA_SDA
	01	GPIO70
	10	GPIO70
	11	GPIO70
IoMux47	00	VGA_SCL
	01	GPIO71
	10	GPIO71
	11	GPIO71
IoMux48	-	Not used
IoMux49	-	This pin is configured as SGPIO_CLK0 when SGPIO function is enabled in SATA. If it is not configured as SGPIO, then it is confuged as SDCLK when SD function is enabled. If neither function is enabled, then it is configured as GPIO73
IoMux4A	-	This pin is configured as SGPIO_LOAD0 when SGPIO function is enabled in SATA. If it is not configured as SGPIO, then it is confuged as SDCLK when SD function is enabled. If neither function is enabled, then it is configured as GPIO74
IoMux4B	-	This pin is confuged as SDCD when SD function is enabled. If SD function is not enabled, then it is configured as GPIO75
IoMux4C	-	This pin is confuged as SDWP# when SD function is enabled. If SD function is not enabled, then it is configured as GPIO76
IoMux4D	-	This pin is configured as SGPIO_DATAIN0 when SGPIO function is enabled in SATA. If it is not configured as SGPIO, then it is confuged as SDDAT0 when SD function is enabled. If neither function is enabled, then it is configured as GPIO77
IoMux4E	-	This pin is configured as SGPIO_DATAOUT0 when SGPIO function is enabled in SATA. If it is not configured as SGPIO, then it is confuged as SDDAT1 when SD function is enabled. If neither function is enabled, then it is configured as GPIO78
IoMux4F	-	This pin is confuged as SDDAT2 when SD function is enabled. If SD function is not enabled, then it is configured as GPIO79
IoMux50	-	This pin is confuged as SDDAT3 when SD function is enabled. If SD function is not enabled, then it is configured as GPIO80
IoMux51 through IoMux5F	-	Not used
IoMux60	00	GA20IN/GEVENT0
	01	GPIO96
	10	GPIO96
	11	GPIO96

IoMux Register	Value	Function
IoMux61	00	KBRST#/GEVENT1
	01	GPIO97
	10	GPIO97
	11	GPIO97
IoMux62	00	THERMTRIP#//SMBALERT#/ GEVENT2
	01	GPIO98
	10	GPIO98
	11	GPIO98
IoMux63	00	PME#/GEVENT3
	01	GPIO99
	10	GPIO99
	11	GPIO99
IoMux64	00	GEVENT4
	01	GPIO100
	10	PCIE_RST2#
	11	GEVENT4
IoMux65	00	GEVENT5/GPIO101
	01	LPC_PD#
	10	GEVEN5/GPIO101
	11	Reserved
IoMux66		If CIR is enabled, USB_OC6#/IR_TX1/GEVENT6 is configured as IR_TX1. Otherwise, it is configured as defined by IoMux66.
	00	USB_OC6#
	01	GEVENT6/GPIO102
	10	GEVENT6/GPIO102
	11	GEVENT6/GPIO102
IoMux67	00	DDR3_RST#/GEVENT7/VGA_PD is configured as DDR3_RST# when CPU strap is set to GH class and MISC_50[16]=0. If MISC_50[16]=1 or it is strapped to Fusion class APOU, then it becomes VGA_PD
	01	GEVENT7/GPIO103
	10	GEVENT7/GPIO103
	11	GEVENT7/GPIO103
IoMux68	00	GEVENT8
	01	GEVENT8/GPIO104
	10	GEVENT8/GPIO104
	11	GEVENT8/GPIO104
IoMux69		If BIOS flash is set to SPI ROM AND QDR mode is enabled, this pin is configured as SPI_HOLD
	00	GEVENT9
	01	GEVENT9/GPIO105
	10	GEVENT9/GPIO105
	11	GEVENT9/GPIO105
IoMux6A	00	GEVENT10
	01	GEVENT10/GPIO106
	10	GEVENT10/GPIO106
	11	GEVENT10/GPIO106
IoMux6B	00	GEVENT11
	01	GEVENT11/GPIO107
	10	GEVENT11/GPIO107
	11	GEVENT11/GPIO107
IoMux6C	00	USB_OC0#
	01	GEVENT12/GPIO108
	10	LPC_PD#
	11	Reserved

IoMux Register	Value	Function
IoMux6D	00	USB_OC1#
	01	GEVENT13/GPIO109
	10	GEVENT13/GPIO109
	11	GEVENT13/GPIO109
IoMux6E	00	USB_OC2#
	01	GEVENT14/GPIO110
	10	GEVENT14/GPIO110
	11	GEVENT14/GPIO110
IoMux6F	00	USB_OC3#
	01	GEVENT15/AC_PRES
	10	GEVENT15/GPIO111
	11	GEVENT15/GPIO111
IoMux70	00	USB_OC4#/GEVENT16/CIR_RX0
	01	GEVENT16
	10	GEVENT16/GPIO112
	11	GEVENT16/GPIO112
IoMux71		If CIR is enabled, USB_OC6#/IR_TX1/GEVENT6 is configured as IR_TX1. Otherwise, it is configured as defined by IoMux66.
	00	USB_OC5#
	01	GEVENT17/GPIO113
	10	GEVENT17/GPIO113
	11	GEVENT17/GPIO113
IoMux72	00	BLINK
	01	USB_OC8#/GEVENT18
	10	GEVENT18/GPIO114
	11	GEVENT18/GPIO114
IoMux73	00	GEVENT19
	01	GEVENT19/GPIO115
	10	GEVENT19/GPIO115
	11	GEVENT19/GPIO115
IoMux74	00	GEVENt20/CIR_RX1
	01	GEVENT20/GPIO116
	10	GEVENT20/GPIO116
	11	GEVENT20/GPIO116
IoMux75	00	SPI_CS3#
	01	GEVENT21
	10	GEVENT21/GPIO117
	11	GEVENT21/GPIO117
IoMux76	00	GEVENT22
	01	GEVENT22/GPIO118
	10	GEVENT22/GPIO118
	11	GEVENT22/GPIO118
IoMux77	00	GEVENT23
	01	GEVENT23/GPIO119
	10	GEVENT23/GPIO119
	11	GEVENT23/GPIO119
IoMux78 through IoMux A0		Not used
IoMuxA1		If BIOS flash is set to SPI ROM AND QDR mode is enabled, this pin is configured as SPI_WP#; otherwise, the pin is defined by IoMuxA1
	00	ROM_RST#
	01	GPIO161
	10	GPIO161
	11	GPIO161
IoMuxA2 through IoMuxA5		Not used

IoMux Register	Value	Function
IoMuxA6	00	SPI_CS2#
	01	Reserved
	10	GPIO166
	11	GPIO166
IoMuxA7	00	AzSDIN0
	01	GPIO167
	10	GPIO167
	11	GPIO167
IoMuxA8	00	AzSDIN1
	01	GPIO168
	10	GPIO168
	11	GPIO168
IoMuxA9	00	AzSDIN2
	01	GPIO169
	10	GPIO169
	11	GPIO169
IoMuxAA	00	AzSDIN3
	01	GPIO170
	10	GPIO170
	11	GPIO170
IoMuxAB	00	TEMPIN0 (this also requires the enable bit in PMIO2)
	01	GPIO171
	10	GPIO171
	11	GPIO171
IoMuxAC	00	TEMPIN1 (this also requires the enable bit in PMIO2)
	01	GPIO172
	10	GPIO172
	11	GPIO172
IoMuxAD	00	TEMPIN2 (this also requires the enable bit in PMIO2)
	01	GPIO173
	10	GPIO173
	11	GPIO173
IoMuxAE	00	TEMPIN3 (this also requires the enable bit in PMIO2)
	01	GPIO174
	10	GPIO174
	11	GPIO174
IoMuxAF	00	VIN0 (this also requires the enable bit in PMIO2)
	01	GPIO175
	10	GPIO175
	11	GPIO175
IoMuxB0	00	VIN1 (this also requires the enable bit in PMIO2)
	01	GPIO176
	10	GPIO176
	11	GPIO176
IoMuxB1		SGPIO_DATAIN (when it is enabled in SATA)
	00	VIN2 (this also requires the enable bit in PMIO2)
	01	GPIO177
	10	GPIO177
	11	GPIO177
IoMuxB2		SGPIO_DATAOUT (when it is enabled in SATA)
	00	VIN3 (this also requires the enable bit in PMIO2)
	01	GPIO178
	10	GPIO178
	11	GPIO178

IoMux Register	Value	Function
IoMuxB3		SGPIO_LOAD (when it is enabled in SATA)
	00	VIN4 (this also requires the enable bit in PMIO2)
	01	GPIO179
	10	GPIO179
	11	GPIO179
IoMuxB4		SGPIO_CLK (when it is enabled in SATA)
	00	VIN5 (this also requires the enable bit in PMIO2)
	01	GPIO180
	10	GPIO180
	11	GPIO180
IoMuxB5	00	VIN6 (this also requires the enable bit in PMIO2)
	01	GPIO181
	10	GPIO181
	11	GPIO181
IoMuxB6	00	VIN7 (this also requires the enable bit in PMIO2)
	01	GPIO182
	10	GPIO182
	11	GPIO182
IoMuxB7	00	Reserved
	01	GPIO183
	10	GPIO183
	11	GPIO183
IoMuxB8	00	IR_LED/LLB#
	01	GPIO184
	10	GPIO184
	11	GPIO184
IoMuxB9	-	If OHCI4 is enabled, this becomes USB_FSD0P; otherwise, it is GPIO185
IoMuxBA	-	If OHCI4 is enabled, this becomes USB_FSD1P; otherwise, it is GPIO186
IoMuxBB	-	If Smbus0Sel[4] is true, this becomes SDA4; otherwise, it is GPIO187
IoMuxBC	-	If Smbus0Sel[4] is true, this becomes SCL4; otherwise, it is GPIO188
IoMuxBD	-	GPIO189
IoMuxBE	-	GPIO190
IoMuxBF	-	GPIO191
IoMuxC0	-	GPIO192
IoMuxC1	-	If Smbus0Sel[2] is true, this becomes SCL2; otherwise, it is GPIO193
IoMuxC2	-	If Smbus0Sel[2] is true, this becomes SDA2; otherwise, it is GPIO194
IoMuxC3	-	If Smbus0Sel[3] is true, this becomes SCL3; otherwise, it is GPIO195
IoMuxC4	-	If Smbus0Sel[2] is true, this becomes SDA3; otherwise, it is GPIO196
IoMuxC5	-	If IMC is enabled, this pin can be configured as PWM0; otherwise, it can be configured as GPIO197
IoMuxC6	-	If IMC is enabled, this pin can be configured as PWM1; otherwise, it can be configured as GPIO198
IoMuxC7	-	If IMC is enabled, this pin can be configured as PWM2; otherwise, it can be configured as GPIO199
IoMuxC8	-	If IMC is enabled, this pin can be configured as PWM3; otherwise, it can be configured as GPIO200
IoMuxC9 through IoMuxE2	-	Correpsonding GPIO201 through 226 are controlled directly by the respective GPIO registers.
IoMuxE3	-	If ASF is enabled, this pin becomes SCL1; otherwise, it is GPIO227
IoMuxE4	-	If ASF is enabled, this pin becomes SDA1; otherwise, it is GPIO228
IoMuxE5	00	DPHPD
	01	GPIO229
	10	GPIO229
	11	GPIO229
IoMuxE6 through IoMuxFF	-	Not used

3.8 Miscellaneous Registers

Miscellaneous registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from “AcpiMMioAddr “ + 0xE00 to “AcpiMMioAddr” + 0xEFF.

The base address “AcpiMMioAddr” is defined in PM_reg x24, with the default base address at “FED8_0000.”

The Miscellaneous Registers block is used for e-fuse, strap, and clock control.

Register Name	Offset Address
GPPClkCntrol	00h
ClkOutputCntrl	04h
CGPllConfig1	08h
CGPllConfig2	0Ch
CGPllConfig3	10h
CGPllConfig4	14h
CGPllConfig5	18h
CGPllConfig6	1Ch
IMPCalibration	20h
ClkDrvSth1	24h
ClkDrvSth2	28h
ClkGatedCntl	2Ch
OscFreqCounter	30h
HpetClkPeriod	34h
MiscClkCntrl	40h
PostCode	44h
JtagCntrl	50h
MiscFix	51h
Reserved	51h
JdleCntrl	60h
StrapStatus	80h
StrapOverride	84h
AutoTransaction	90h
AllowEC	91h
AutoAdrLow	94h
AutoAdrHigh	98h
AutoData	9Ch
CPU_PState0	C0h
CPU_PState1	C4h
CPU_CState0	D0h
CPU_CState1	D4h
SataPortSts	F0h
ClkCntrlSts	F4h

GPPClkCntrol – R/W – 32 bits - [MISC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK0 Clock Request mapping	3:0	Fh	GPP0 PCIE clock pins (GPP_CLK0P/GPP_CLK0N) output control by CLKREQ# pin GPP_CLK0P/GPP_CLK0N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP0 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP0 PCIE clock output pins if it is asserted. GPP0_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)
GPP_CLK1 Clock Request mapping	7:4	Fh	GPP1 PCIE clock pins (GPP_CLK1P/GPP_CLK1N) output control by CLKREQ# pin GPP_CLK1P/GPP_CLK1N pins are powered off when FCH is strapped to use an external clock and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP1 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off GPP1 PCIE clock output pins if it is asserted. GPP1_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

GPPClkCntrol – R/W – 32 bits - [MISC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK2 Clock Request mapping	11:8	Fh	GPP2 PCIE clock pins (GPP_CLK2P/GPP_CLK2N) output control by CLKREQ# pin GPP_CLK2P/GPP_CLK2N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP2 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP2 PCIE clock output pins if it is asserted. GPP2_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)
GPP_CLK3 Clock Request mapping	15:12	Fh	GPP3 PCIE clock pins (GPP_CLK3P/GPP_CLK3N) output control by CLKREQ# pin GPP_CLK3P/GPP_CLK3N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP3 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP3 PCIE clock output pins if it is asserted. GPP3_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

GPPClkCntrol – R/W – 32 bits - [MISC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK4 Clock Request mapping	19:16	Fh	GPP4 PCIE clock pins (GPP_CLK4P/GPP_CLK4N) output control by CLKREQ# pin GPP_CLK4P/GPP_CLK4N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP4 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP4 PCIE clock output pins if it is asserted. GPP4_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)
GPP_CLK5 Clock Request mapping	23:20	Fh	GPP5 PCIE clock pins (GPP_CLK5P/GPP_CLK5N) output control by CLKREQ# pin GPP_CLK5P/GPP_CLK5N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP5 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP5 PCIE clock output pins if it is asserted. GPP5_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

GPPClkCntrol – R/W – 32 bits - [MISC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK6 Clock Request mapping	27:24	Fh	GPP6 PCIE clock pins (GPP_CLK6P/GPP_CLK6N) output control by CLKREQ# pin GPP_CLK6P/GPP_CLK6N pins are powered off when FCH is strapped to use an external clock, and powered on when strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP6 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off GPP6 PCIE clock output pins if it is asserted. GPP6_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)
GPP_CLK7 Clock Request mapping	31:28	Fh	GPP7 PCIE clock pins (GPP_CLK7P/GPP_CLK7N) output control by CLKREQ# pin GPP_CLK7P/GPP_CLK7N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP7 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off GPP7 PCIE clock output pins if it is asserted. GPP7_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

ClkOutputCntrl – R/W – 32 bits - [MISC_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK8 Clock Request mapping	3:0	Fh	GPP8 PCIE clock pins (GPP_CLK8P/GPP_CLK8N) output control by CLKREQ# pin GPP_CLK8P/GPP_CLK8N PCIE clock output pins are powered off when FCH is strapped to use an external clock, and powered on when strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP8 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off GPP8 PCIE clock output pins if it is asserted. GPP8_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)
SLT_GFX_CLK Clock Request Mapping	7:4	Fh	Gfx PCIE clock pins (SLT_GFX_CLKP/SLT_GFX_CLKN) output control SLT_GFX_CLKP/SLT_GFX_CLKN pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, Gfx PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off Gfx PCIE clock output pins if it is asserted. Gfx_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

ClkOutputCntrl – R/W – 32 bits - [MISC_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
APU/PCIE/Disp/Disp2Clk override enable	8	0b	Enable clock buffers override control for APU_CLK, PCIE_RCLK, DISP_CLK, and DISP2_CLK differential clock outputs. The state of the above 4 differential clock pairs are controlled by the strap (LPCCLK1). The states are: Strap (LPCCLK1) = 1 : clock output buffers enable Strap (LPCCLK1) = 0 : clock output buffers OFF This "override enable bit" allows the clock output buffers to be controlled through ClkCntrol1 register regardless of the strap value. 0: Disable override control over clock strap (LPCCLK1) 1: Enable override control clock strap (LPCCLK1)
APU_CLK Power Down Enable	9	0b	Power down APU_CLK output buffer for power saving. Set to 1 to power down the APU_CLK output buffer, this bit can only take effect when "APU/PCIE/Disp/Disp2Clk override enable" is set to 1.
DISP2_CLK Power Down Enable	10	0b	Power down DISP2_CLK output buffer for power saving. Set to 1 to power down the DISP2_CLK output buffer, this bit can only take effect when "APU/PCIE/Disp/Disp2Clk override enable" is set to 1.
PCIE_RCLK_Output Power Down Enable	11	0b	Power down PCIE_RCLK output buffer for power saving. Set to 1 to power down the PCIE_RCLK output buffer, this bit can only take effect when "APU/PCIE/Disp/Disp2Clk override enable" is set to 1.
DISP_CLK Power Down Enable	12	0b	Power down DISP_CLK output buffer for power saving. Set to 1 to power down the DISP_CLK output buffer, this bit can only take effect when "APU/PCIE/Disp/Disp2Clk override enable" is set to 1.
PCIE_RCLK Power Down Enable	13	0b	Power down PCIE_RCLK input buffer for power saving. Set to 1 to power down the PCIE_RCLK input buffer.
Reserved	15:14	00b	
Clock Buffer Bias Power Down Enable	16	1b	Set to 1 to power down the clock buffers bias current circuit for power saving.
Reserved	19:17		
APU_CLK voltage swing control	20	0b	Voltage swing control for APU_CLK output buffer. 0: High swing, 20% more than regular swing 1: Normal swing

CGPllConfig1 – R/W – 32 bits - [MISC_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
CG1 Spread Spectrum Enable	0	0b	CG1_PLL Spread Spectrum Enable 0: Disable Spread Spectrum (default) 1: Enable Spread Spectrum
Reserved	4:1		
SATA clock source select	5	0b	SATA clock source frequency select from CG2_PLL 0: PLL 100Mhz (default) 1: Buffered 25Mhz
Reserved	6		(6)
Cg1Pll_SS_AMOUNT_NFRAC_SLIP_0	7	0b	CG1 PLL spread magnitude (slip portion) when "Enhanced Spread Mode Enable" (MISC_Reg x08[8])" is set. This bit is not used when "Enhanced Spread Mode Enable" (MISC_Reg x08[8])" is not set.

CGPllConfig1 – R/W – 32 bits - [MISC_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Enhanced Spread Mode Enable	8	1b	To enable enhanced Spread Spectrum Mode. 0: Disable 1: Enable **Note:** When the bit is set to 1, the control of spread magnitude and spread range can be controlled separately. The spread range is controlled by Cg1Pll_Q_SS_DSFRAC, Cg1Pll_ FBDIV_FRACTION & Cg1Pll_ FBDIV. And the spread magnitude is controlled by Cg1Pll_SS_AMOUNT_DSFRAC, Cg1Pll_SS_AMOUNT_NFRAC_SLIP.
CgPll_overclocking_test	9	0b	Over-clocking test enable 0: Disable 1: Enable
CG2 Reset	10	0b	CG2 PLL Reset Set to 1 to reset the CG2 PLL. The bit will be clear to '1' by hardware after reset sequence is done.
Cg2Pll_ OCLKBYX_SEL	12:11	00b	Source of OCLKBYX: non-slip clock running at 400MHz 0x0 = non-slip clock divided by 3 0x1 = non-slip clock divided by 2 0x2 = non-slip clock divided by 4 0x3 = non-slip clock divided by 4
Cg2Pll_Q_IBIAS	14:13	01b	CG2 PLL current bias adjustment
Cg2Pll_Q_ICO_IBIAS	16:15	10b	ICO current bias adjustment
Cg2Pll_Q_SCL_IBIAS	18:17	10b	SCL Dividers' current bias adjustment
Cg2Pll_ MODE_S_FORCE	22:19	0101b	Force calibration results to known state (Strap) Must bypass calibration logic by setting Cg2Pll_CAL_BYPASS =1
Cg2Pll_ CAL_BYPASS	23	0b	CG2 PLL Calibration by-pass mode select 0: Calibrate 1: Bypass calibration and use Cg2Pll_MODE_S_FORCE[3:0] setting.
Cg1Pll_Q_CP[3:0]	27:24	1h	CG1 PLL charge pump current adjustment.
Cg1Pll_SS_AMOUNT_DSFRAC_12_9	31:28	9h	CG1 PLL spread magnitude (delta-sigma portion) when "Enhanced Spread Mode Enable" (MISC_Reg x08[8]) is set. These bits are not used when "Enhanced Spread Mode Enable" (MISC_Reg x08[8])" is not set.

CGPllConfig2 – R/W – 32 bits - [MISC_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cg1Pll_Q_ LF_MODE	8:0	0FDh	CG1 PLL Loop filter mode settings Controls the loop filter for CG1.
Cg2Pll_REFDIV_LOAD	9	0b	When setting this bit, different CG2 PLL reference divider values can be loaded into CG2 PLL thru Cg2Pll_REF_DIV registers. Depending on LPCCLK1 clock mode strap, either 5'b00001 (integrated clock mode) or 5'b00100 (external clock mode) is loaded.
Cg2Pll_REF_DIV	14:10	00001b	Reference divider value for CG2 PLL 5'b00001 = 25Mhz 5'b00100 = 100Mhz
Cg2Pll_FBDIV	25:15	18h	Feedback divider value for CG2 PLL
Cg2Pll_FBDIV_FRACTION	29:26	0h	CG2PLL Fractional Control of feedback divider
Cg2Pll_ VCO_GAIN	31:30	0h	CG2 PLL VCO gain setting adjustment.

CGPllConfig3 – R/W – 32 bits - [MISC_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Cg1Pll_SS_STEP_SIZE_ DSFRAC_7_0	7:0	BEh	Control spread step size (delta-sigma portion) bit-7 ~ bit-0. Use this to adjust modulation rate. Controls the SS_STEP_SIZE_DSFRAC for CG1, with default value = 83h. **Note:** There are 16-bits of register to control spread step size; these bits are defined in various CGPllConfig registers: "SS_STEP_SIZE_DSFRAC_15_13" , "SS_STEP_SIZE_DSFRAC_12_8" & "SS_STEP_SIZE_DSFRAC_7_0".
Cg1Pll_Q_SS_DSFRAC	23:8	9975h	Delta Sigma signal. Fraction parameter for DS modulator, expresses x/1024. Controls the SS_DSFRAC for CG1 with default value = 9975h.
Cg1Pll_Q_SS_DSMODE	25:24	10b	Delta Sigma signal. Selects the order of DS modulator: 0: DS modulator is disabled (Default) 1: 1st order 2: 2nd order 3: 3rd order Controls the SS_DSMODE for CG1.
Cg2Pll_CAL_FB	31:26	18h	PLL control bits for internal dividers for calibration

CGPllConfig4 – R/W – 32 bits - [MISC_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Cg2Pll_Q_HALFGM_EN	0	0b	Set second loop op-amp to ½ gm 0: Do not lower gm by 0.5 (Default). 1: Lower gm by 0.5
Cg2Pll_SEL_SPARE0	1	0b	Spare bit.
Cg2Pll_CNTL	11:2	000h	Bits for input control. IPPLL_CNTL[0] => Controls 100MHz bypass mux. 0: Send divider output to OPPLL_PCIe_CLK differential output path. 1: Send 100MHz PCIe Ref clock to OPCIe_CLK differential output. IPPLL_CNTL[4] => Enables Power Saving Mode in digital block. Tied to IPPLL_PWRSVG_EN on the digital block. 0: All blocks and dividers are enabled in the digital block (Default) 1: Some blocks and dividers are disabled in the digital block to save power and more importantly reduce noise. IPPLL_CNTL[5] => Enables Debug Bus output in digital block. Tied to IPPLL_DEBUG_EN on the digital block. 0: All 150MHz output from digital block are disabled (Default). 1: 150MHz outputs from digital block are enabled.
Cg2Pll_IVR_BIAS	15:12	0h	Adjust bias current for PLL regulator
Cg2Pll_ IVR_FILTER	17:16	0h	Bits for Regulator reference voltage Low Pass Filter

CGPllConfig4 – R/W – 32 bits - [MISC_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Cg2Pll_ IVR_LPF_C	21:18	0h	Voltage regulator bandwidth Capacitor adjustment Bit 0 if "1" remove 1X from total capacitance. Bit 1 if "1" remove 2X from total capacitance. Bit 2 if "1" remove 4X from total capacitance. Bit 3 removed programmability to improve PSRR. Default is 0000: Use all capacitors.
Cg2Pll_ IVR_LPF_R	25:22	0h	Voltage regulator bandwidth series Resistor adjustment Bit 0 if "1" short 140K from total resistance. Bit 1 if "1" short 281K from total resistance. Bit 2 if "1" short 562K from total resistance. Bit 3 if "1" short 1.124M from total resistance. Default is 0000: Use all resistors 2.1075M Ohms.
Cg2Pll_ IVR_PD	26	0b	Regulator Power Down.
Cg2Pll_ IVR_PG_BIT	31:27	00h	Voltage regulator Pass Gate control. Bit 0 if "1" disconnect 1/5th of the passgates. Bit 1 if "1" disconnect 1/5th of the passgates. Bit 2 if "1" disconnect 1/5th of the passgates. Bit 3 if "1" disconnect 1/5th of the passgates. Bit 4 if "1" disconnect 1/5th of the passgates. Default is 00000: Use all passgates (Maximum VCO current 30mA).

CGPllConfig5 – R/W – 32 bits - [MISC_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Cg2Pll_ IVR_RESET	0	0b	Regulator Reset
Cg2Pll_ IVR_TRIM	4:1	0h	Bit Setting Result Output Voltage 0000 1.222V (Nominal is 1.1V + 122mV) 0001 1.283V (+61mV) 0010 1.344V (+122mV) 0011 1.406V (+184mV) 0100 1.344V (+122mV) 0110 1.467V (+367mV) 0111 1.528V (+428mV) 1000 1.1V (-122mV) 1001 1.161V (-61mV) 1010 1.1V (-122mV) 1011 1.161V (-61mV) 1100 1.1V (-122mV) 1101 1.161V (-61mV) 1110 1.1V (-122mV) 1111 1.161V (-61mV)
Cg1Pll_FBDIV	12:5	18h	Feedback divider value for CG1 PLL

CGPllConfig5 – R/W – 32 bits - [MISC_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Cg1Pll's SS_STEP_SIZE_DSFRAC_15_14, SS_AMOUNT_FBDIV_0 / SS_AMOUNT_DSFRAC_15_13	15:13	100b	Controls spread step size (delta-sigma portion) bit-15 ~ bit-14. Use this to adjust modulation rate when "Enhanced Spread Mode Enable" (MISC_Reg x08[8]) is not set. Bit-13 is used to control spread magnitude (integer portion) when "Enhanced Spread Mode Enable" (MISC_Reg x08[8]) is not set. Controls the spread magnitude (delta-sigma portion) bit-15 ~ bit-13 when "Enhanced Spread Mode Enable" is set. This is only available in silicon revision A12 and above. **Note:** There are 16-bit of register to control spread step size; these bits are defined in various CGPllConfig registers: "SS_STEP_SIZE_DSFRAC_15_13" , "SS_STEP_SIZE_DSFRAC_12_8" & "SS_STEP_SIZE_DSFRAC_7_0".
Cg1Pll_ FBDIV_FRACTION	19:16	0h	CG1PLL Fractional Control of feedback divider
Cg2_FBMUX	20	0b	PLL feedback source
Cg1Pll_REFDIV	25:21	01h	CG1_PLL reference divider value. Only available for silicon revision A12 and above.
Cg1Pll_VCO800M_En	26	0b	Enable CG1_PLL VCO running at 800Mhz Requires a warm reset after setting this bit to enable/disable VCO running at 800Mhz. 0: Disable 1: Enable
Cg1Pll_ OCLKBYX_SEL	28:27	00b	Source of OCLKBYX: CG1 VCO clock running at 1200Mhz or 800MHz. 00: VCO clock divided by 3 01: VCO clock divided by 2 10: VCO clock divided by 4 11: VCO clock divided by 4
Cg2Pll_VCO800M_En	29	0b	Enable CG2_PLL VCO running at 800Mhz. Requires a warm reset after setting this bit to enable/disable VCO running at 800MHz. 0: disable 1: enable
Cg1Pll_REFDIV_LOAD	30	0b	Set 1 to load CG1_PLL REF_DIV value from MISC_Reg x18[25:21] when it is not SSC or Overclock test mode.
Reserved	31	0b	

CGPllConfig6 – R/W – 32 bits – [MISC_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
Cg1Pll_SS_STEP_SIZE_DSFRAC_12_8	5:0	00h	Controls spread step size(delta-sigma portion) bit-12 ~ bit-8. Use this to adjust modulation rate. Bit-5 is used to control the spread magnitude (slip portion) bit-1 (SS_AMOUNT_NFRAC_SLIP_1) when "Enhanced Spread Mode Enable" (MISC_Reg x08[8])" is set. **Note:** There are 16-bits of register to control spread step size; these bits are defined in various CGPllConfig registers: "SS_STEP_SIZE_DSFRAC_15_13" , "SS_STEP_SIZE_DSFRAC_12_8" & "SS_STEP_SIZE_DSFRAC_7_0".

CGPllConfig6 – R/W – 32 bits – [MISC_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
Cg2Pll_PWDN_Force	6	0h	Force Cg2Pll Power Down. Set this bit and Misc_Reg 08[6] to 1 to power down CG2_PLL
25MXtalPad_PWDN_Force	7	0h	Force 25M XTAL Pad Power Down. Set this bit and Misc_Reg 40[17] to 1 to power down 25Mhz XTAL Pad
Cg2Pll_Refclk_Sel	8	1h	Cg2Pll Reference Clock Select: 0: 100Mhz from external clock chip 1: 25Mhz from XTAL
Reserved	10:9	0h	
Cg1Pll_Spare	14:11	0h	
Cg2Pll_Spare	18:15	0h	
Cg2Pll_Core_PWDN_EN	19	0h	Power Off Cg2Pll Core. Setting this bit will power off Cg2Pll core, but output buffer will still be ON. This is used when Cg2Pll is power off, but needs to provide buf25Mhz clock for SATA in external clock mode.
SATA_buf25M_ClkSrc	20	0h	SATA Buf25Mhz Clock Source. SATA Buf25Mhz clock can be from either CG1_PLL or CG2_PLL. Both are non-spread. 0: from CG2_PLL 1: from CG1_PLL
CG1_ClkDriver_Type	24:21	4'b0000	CG1_PLL Clock Driver 1: CMOS type clock driver (consume less power) 0: CML type clock driver Bit21 is for USB Bit22 is for SATA Bit23 is for CPU Bit24 is for PCIE
CG2_ClkDriver_Type	28:25	4'b0000	CG2_PLL Clock Driver. 0: CML type clock driver 1: CMOS type clock driver (consume less power) Bit21 is for USB Bit22 is for SATA Bit23 is for CPU Bit24 is for PCIE
Reserved	31:29		Reserved

IMPCalibration – R/W – 32 bits – [MISC_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	8h	
Reserved	7:4	7h	
Reserved	11:8	6h	
RX_MANUAL_IMPEDANCE	15:12	6h	Manually overwrite IMP_RXIMP_CNTRL[15:0] and RXTERM_VAL[15:0]. Will be converted to thermometer code.
PAD_UPDATE_RATE	20:16	Eh	PAD's update interval Controls how fast the desired calibration value will be obtained. Also controls how frequently re-calibration will occur.
PAD_SAMPLE_DELAY	25:21	1h	Sampling window. Controls how many clock cycles statemachine will stay in NDELAY or PDELAY.
Reserved	26	0h	
Reserved	27	0h	

IMPCalibration – R/W – 32 bits – [MISC_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
PAD_MANUAL_OVERRIDE	28	0h	Enable the impedance overwrite.
Reserved	29	0h	
Reserved	30	1h	
RX_IMP_PDNB	31	1h	Disable the calibration for RX. 0: Power Down 1: Power On

ClkDrvSth1 – R/W – 32 bits – [MISC_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK1 Clock Buffer Driving Strength Control	1:0	01b	Drive Strength control for GPP_CLK_1 differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
GPP_CLK2 Clock Buffer Driving Strength Control	3:2	01b	Drive Strength control for GPP_CLK_2 differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
GPP_CLK3 Clock Buffer Driving Strength Control	5:4	01b	Drive Strength control for GPP_CLK_3 differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
GPP_CLK4 Clock Buffer Driving Strength Control	7:6	01b	Drive Strength control for GPP_CLK_4 differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
GPP_CLK5 Clock Buffer Driving Strength Control	9:8	01b	Drive Strength control for GPP_CLK_5 differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
GPP_CLK6 Clock Buffer Driving Strength Control	11:10	01b	Drive Strength control for GPP_CLK_6 differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
GPP_CLK7 Clock Buffer Driving Strength Control	13:12	01b	Drive Strength control for GPP_CLK_7 differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA

ClkDrvSth1 – R/W – 32 bits – [MISC_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK8 Clock Buffer Driving Strength Control	15:14	01b	Drive Strength control for GPP_CLK_8 differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
GPP_CLK9 Clock Buffer Driving Strength Control	17:16	01b	Drive Strength control for GPP_CLK_9 differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
SLT_GFX Clock Buffer Driving Strength Control	19:18	01b	Drive Strength control for SLT_GFX differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
APU_CLK Clock Buffer Driving Strength Control	21:20	01b	Drive Strength control for APU_CLK differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
DISP2_CLK Clock Buffer Driving Strength Control	23:22	01b	Drive Strength control for DISP2_CLK differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
NB_PCIe Clock Buffer Driving Strength Control	25:24	01b	Drive Strength control for NB_PCIe differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
NB_Disp Clock Buffer Driving Strength Control	27:26	01b	Drive Strength control for NB_Disp differential Clock Buffers 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
Reserved	31:28	00h	

ClkDrvSth2 – R/W – 32 bits – [MISC_Reg: 28h]			
Field Name	**Bits**	**Default**	**Description**
PAD_INC_THRESHOLD	4:0	18h	Establishes an upper limit for which TX/RX_COUNT is compared against. Larger than or smaller than this value will result in IMP_RX/TXIMP_CNTRL[15:0] and TX/RXTERM_VAL[15:0] to increase or descrease.
PAD_DEC_THRESHOLD	9:5	08h	Establishes a lower limit for which TX/RX_COUNT is compared against. Larger than or smaller than this value will result in IMP_RX/TXIMP_CNTRL[15:0] and TX/RXTERM_VAL[15:0] increasing or descreasing.
PERIODIC_CAL	10	0h	Periodic Calibration Enable 0: Disable 1: Enable
Reserved	11	0h	

ClkDrvSth2 – R/W – 32 bits – [MISC_Reg: 28h]			
Field Name	**Bits**	**Default**	**Description**
Clkbuf_IMP_Update	12	0h	Clkbuf Impedance Update. Clkgen_outpad Impedance value will be locked after initial calibration cycle. Setting this bit to 1 will update impedance value for clkgen_outpad when Periodic Calibration is enabled or Re-Calibration is enabled
IMP_CalHalt	13	0h	Halt Impedance Calibration cycle Setting this bit to 1 will halt impedance calibration cycle
Reserved	15:14	0h	
OSCOUT1_CLK_sel	18:16	3'b000	Defines auxiliary output clock frequency on OSCOUT1 pin. 000: 14MHz (default) 001: 25MHz 010: 48MHz 011: 50MHz 1xx: 24MHz
OSCOUT2_CLK_sel	21:19	3'b000	Defines auxiliary output clock frequency on USBCLK/OSCOUT2 pin. 000: 14MHz (default) 001: 25MHz 010: 48MHz 011: 50MHz 1xx: 24MHz

ClkGatedCntl – R/W – 32 bits – [MISC_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
AlinkClk_GateOff_Threshold	7:0	00h	A-Link Clock GatedOff Threshold. When all controllers agree to stop A-Link clock, clkgating logic will start a timer and deassert ALClk_Enable when the timer reaches a programmable threshold. If threshold is "0," gated clock will stop at 3 falling edge after ALClk_Enable is deasserted. If threshold is "N", gated clock will stop at (3+N) falling edge after Clk_Enable is deasserted. ALClk_Enable is an internal handshake signal indicating whether gated A-Link clock is running or not.
BlinkClk_GateOff_Threshold	15:8	00h	B-Link Clock GatedOff Threshold. When all controllers agree to stop B-Link clock, clkgating logic will start a timer and deassert BLClk_Enable when the timer reaches a programmable threshold. If threshold is "0," gated clock will stop at 3 falling edge after BLClk_Enable is deasserted. If threshold is "N", gated clock will stop at (3+N) falling edge after Clk_Enable is deasserted. BLClk_Enable is an internal handshake signal indicating whether gated B-Link clock is running or not.
AlinkClk_GateOffEn	16	0b	A-Link Clock Gate-Off Enable Internal A-Link clock has two clock trees: one is a free-running clock and the other is a gated clock. When all controllers agree to stop the gated A-Link clock and this bit got set, clkgating logic will gate off the clock tree from clock root. 0: Disable A-Link Clock Gate-Off function. Default 1: Enable A-Link Clock Gate-Off function

ClkGatedCntl – R/W – 32 bits – [MISC_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
BlinkClk_GateOffEn	17	0b	B-Link Clock Gate-Off Enable Internal B-Link clock has two clock trees: one is a free running clock and the other is a gated clock. When all controllers agree to stop the gated B-Link clock and this bit got set, clkgating logic will gate off the clock tree from clock root. 0: Disable BLink Clock Gate-Off function. Default 1: Enable BLink Clock Gate-Off function
Reserved	28:18	000h	
DebugBusSel_Clktop	31:29	000b	Debug Bus Select for clk_top signals

Note: The definition of the register below (MISC_Reg: 30h) depends on the setting of MISC_Reg: 40h (register AltHPET) bit 30. If this bit is 0, then MISC_Reg: 30h is defined as OscFreqCounter, if it is 1, then MISC_Reg: 30h is defined as AltHPET. In other words:

If MISC_Reg: 40h [30] = 0, MISC_Reg: 30h is:

OscFreqCounter – R/W – 32 bits - [MISC_Reg: 30h]			
Field Name	**Bits**	**Default**	**Description**
OscCountPerSec	15:0	0h	If Misc_reg:40h[30] is 0: This register shows part of OscCountPerSec (bit[15:0]). Number of OSC clocks per second. Whenever bit 31 (CountEnable) is set, an internal counter will start counting the number of OSC clocks per second and record the count value here. If Misc_reg:40h[30] is 1: This register shows AltHPET[15:0] counter. AltHPET[15:0] is the counting on 32KHz RTC clock. It will be reset or wrap around (depending on the setting of Sel_AltHPETrst) every second at the rising of Rtc1HzClk.
OscCountPerSec[27:16]	27:16	0h	Number of OSC clocks per second. Whenever bit 31 (CountEnable) is set, an internal counter will start counting the number of OSC clocks per second and record the count value here.
Reserved	29:28	00b	Reserved
CountIsValid	30	0b	When OscCountPerSec is valid, this bit is set. This bit is read only. SW should always wait for this bit to be set before it reads OscCountPerSec
CountEnable	31	0b	When set, it enables the internal counter to count the number of OSC clocks. When SW is not using this function, it should always set it back to 0 to conserve power.

And if MISC_Reg: 40h [30] = 1, MISC_Reg: 30h is:

AltHPET – R/W – 32 bits - [MISC_Reg: 30h]			
Field Name	**Bits**	**Default**	**Description**
AltHPETCount	15:0	0h	IAltHPETCount[15:0] is counting on the 32KHz RTC clock. It will be reset or wrap around (depending on the setting of Sel_AltHPETrst) every second at the rising edge of Rtc1HzClk.
Reserved	31:16	0h	Reserved

HpetClkPeriod - R/W 8/16/32 bits - [Misc_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
HpetClkPeriod	31:0	0429B17Eh	The register controls the value of clkperiod register in HPET MMIO register space.

MiscClkCntrl – R/W – 32 bits – [MISC_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
SDByPassClkEn	0	1'b0	SD Bypass clock Enable. When set this bit, SD clock will come from SPciGntB[2] pin.
CoreSpeedMode	1	1'b0	Slow down Internal Core Clock (B-Link clock) for power saving. 0: Full speed B-Link clock 1: Slow speed B-Link clock
OSCOUT1_Clk_OutputEnB	2	1'b1	Auxiliary Clock1, OSCOUT1 clock output enable. 0: Enable 1: Disable
OSCOUT1_Clk_Testmode	3	1'b0	When set, OSCOUT1 becomes a test port for clkgen_outpad. Debugging purpose only. This bit should not be set under normal operating condition Test port output will depend on the selection from Misc_Reg x04h[19:17]
USB3_RefClk_Sel	4	1'b1	USB3.0 reference clock source selection in internal clock mode. 0: 100MHz spread clock from internal CG1_PLL 1: 100MHz non-spread clock from internal CG2_PLL
Reserved	5	1'b0	
UsbClkCfg	6	1'b1	Defines whether USB uses the internal or external 48Mhz clock. If USB uses internal 48Mhz as clock source, USBCLK/OSCOUT2 pin can output 14/24/25/48/50Mhz clock depend on OSCOUT2_sel setting. If USB uses external 48Mhz clock as clock source, USBCLK/OSCOUT2 pin cannot be used as Auxiliary clock output. Output enable of OSCOUT2 pin control by UsbClkCfg and OSCOUT2_OutOff. When UsbClkCfg=1 & OSCOUT2_OutOff=0, pin output enable will be on. 0: External 48Mhz 1: Internal 48Mhz (default)
OSCOUT2_OutOff	7	1'b1	If USB uses internal 48Mhz as clock source, set this to "1" will turn off USBCLK/OSCOUT2 clock output. 0: OSCOUT2 pin output enable 1: OSCOUT2 pin output disable. (Turn off OSCOUT2 output)
Reserved	8	1'b0	
SD_Clk_Sel	11:9	3'b100	SD clock frequency 000: 100MHz 001: 80MHz 010: 66.6MHz 011: 57.14MHz 100: 50MHz (default) 101: 44.4MHz 110: 40MHz 111: 25MHz

MiscClkCntrl – R/W – 32 bits – [MISC_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Auxiliary_14Mclk_Sel	12	1'b0	14MHz clock selection for Auxiliary clock output 0: 14.285MHz clock from CG2_PLL 1: 14.318MHz clock from CLK_REQG#/14M_OSC/GPIO65 pin
InvertTermResistor	13	1'b0	Invert Normal REFCLK (NB_PCIE_CLK) termination. 0: Normal REFCLK termination, default 1: Invert Normal REFCLK termination Note: SAd25 has same function, but Inverted value from debug strap. SAd25 strap "1" : Normal REFCLK termination, default SAd25 strap "0" : Invert Normal REFCLK termination
OscClkSwitchEn	14	1'b0	When this bit is set, the Bolton will use the internal PLL to generate the 14Mhz.
BlinkClkSlowEnable	15	1'b0	When this bit is set, internal B-Link clock will run on 66Mhz. The normal internal B-Link clock is running on 133Mhz. See more detail on MISC_Reg: 40h[20]
SD_ClkStop	16	1'b0	Program this bit to "1" before changing SD clock frequency, then program this bit to "0" to re-start SD clock
25Mxtal_PWDN	17	1'b0	Power off 25M Xtal. Set this bit can power off 25Mhz Xtal pad when the following conditions is not true. (1) chip in integrated clock mode, or (2) GEC present, or (3) USB 48Mhz clock from CG2_PLL, or (4) SATA use CG2_PLL clock as ref clock source, or (5) 14.318Mhz clock generated from CG2_PLL (6) 25Mhz Auxiliary clock selected (7) 0: power on 1: power off
DrvSth_Auxiliary_Clk1	18	1'b1	Drive Strength Control for Auxiliary Clock1 (14M_25M_48M_50M_OSC) 0: 4 mA 1: 8 mA (Default)
DrvSth_Auxiliary_Clk2	19	1'b1	Drive Strength Control for Auxiliary Clock2 (USBCLK/14M_25M_48M_50M_OSC) 0: 4 mA 1: 8 mA (Default)
Enable BlinkClkSlow Mode	20	1'b0	Set to 1 to enable internal core clock (B-Link clock) running at slower speed (66Mhz) for power saving. This bit can only take effect when Misc Reg x40[1] is set to "1".
Cg2Pll_VCOREF_Cntrl	22:21	2'b00	CG2Pll VCOREF Control. Only available for silicon revision A12 and above.
Cg2Pll_CALREF_Cntrl	24:23	2'b00	CG2Pll CALREF Control. Only available for silicon revision A12 and above.
Reserved	25		

MiscClkCntrl – R/W – 32 bits – [MISC_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Cg1Pll_FBDIV_Test	26	1'b0	Enable to load CG1_PLL FBDIV value for testing. Requires a warm reset after setting this bit to enable/disable loading CG1_PLL FBDIV. CG1_PLL FBDIV value is in Misc_Reg18[12:5]. 0: Disable 1: Enable
Reserved	28:27	0h	Reserved
Sel_AltHPETrst	29	0	1: Reset AltHPET every second (whenever there is a rising edge of RTC 1Hz clock, AltHPET will be reset) 0: Reset AltHPET at the first rising of RTC 1Hz clock after Sel_AltHPET is set.
Sel_AltHpet	30	1'b0	0: Misc_Reg:30h[15:0] is OscCountPerSec[15:0] 1: Misc_Reg:30h[15:0] is AltHPET[15:0]
Reserved	31	0	Reserved

PostCode – R – 8 bits - [Misc_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
ValueOnPort80	7:0	0h	The 8 bits stores the current the value written to Port 80h

ChipDebugBusByte0 – R – 8 bits - [Misc_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
ChipDebugBus[7:0]	7:0	0h	This register returns the lower 8 bits of the internal Bolton S0 debug bus

ChipDebugBusByte1 – R – 8 bits - [Misc_Reg: 49h]			
Field Name	**Bits**	**Default**	**Description**
ChipDebugBus[15:8]	7:0	0h	This register returns the high 8 bits of the internal Bolton S0 debug bus

ChipDebugBusByte2 – R – 8 bits - [Misc_Reg: 4Ah]			
Field Name	**Bits**	**Default**	**Description**
ChipDebugBus[23:16]	7:0	0h	This register returns the lower 8 bits of the internal Bolton S5 debug bus

ChipDebugBusByte3 – R – 8 bits - [Misc_Reg: 4Bh]			
Field Name	**Bits**	**Default**	**Description**
ChipDebugBus[31:24]	7:0	0h	This register returns the high 8 bits of the internal Bolton S5 debug bus

JtagCntrl – R/W – 8 bits - [Misc_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
XHC jtag tap selection	0	0	XHC tap controller selection 0: Select tap controller of Xhci0 1: Select tap controller of Xhci 1
VGA jtag tap enable	1	0	Enable/disable tap controller inside VGA tile
XHC jtag tap enable	2	0	Enable tap controller in XHC tile. If XHC tap enabled, it has higher priority than rest other tap controllers in S5 or VGA tiles.
Reserved	7:3	5h00	

MiscFix – R/W – 24 bits - [Misc_Reg: 51h]			
Field Name	**Bits**	**Default**	**Description**
PmTimerFix	0	0	Set this bit to 1 to enable PM Timer fix (refer to erratum #39). This setting is applicable to revision A14 only.
Reserved	2:1	0	Reserved
FanLinearEnhanceEn	3	0	Set to 1 to let FanOut0 change along with the current Temp when Temp has been out of LinearRange0.
Reserved	4	0	Reserved
ServerCAtom	5	0	Set to 1 to protect the current Mt C1e from other pending Mt C1e or Fid/Vid.
RstCntlFix	6	0	Set to 1 to allow software to change CPU PwrGood time.
Reserved	9:7	0h	Reserved
ServerCGateBehaviorSel	10	0	0: ServerCGate will de-assert after C-state goes back to IDLE and StpClkDeassert message is sent. 1: ServerCGate will de-assert once C-State goes back to IDLE.
AbNoBypassEn	11	0	When this bit is 1, LPC cycle will not be bypassed when retry times out.
FanLinearHoldFix	12	0	Set to 1 to change unit of LinearHoldCount to 128ms
Reserved	15:13	0h	Reserved
VFidClrThrotEn	16	0	Set to 1 to protect Fid/Vid from throttling
FidReStart	17	0	0: Restart Fid/Vid if the FidVid comes with Mt C1e. 1: Do not restart Fid/Vid if the FidVid comes with Mt C1e
Reserved	19:18	0	Reserved
FidVidAtom	20	0	Set to 1 to protect Fid/Vid from other pending Mt C1e request.
SerIRQ_ClkRun_En	21	0	Set the bit to 1 to extend SerIrq request from device in order to participate in ClkRun# protocol.
Reserved	22	0	Reserved
TimerSyncFix	23	0	Set to 1 to add sync between timer clk and PCI clk

IdleCntrl – R/W – 32 bits - [MISC_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
IdleMonEn	0	0	Control the dynamic clock frequency logic. Set to 1 to enable. When the dynamic clock frequency logic is enabled, it will monitor the amount of idle-ness (defined by IdleThreshold) within a period (defined by IdlePeriodSel). Whenever the condition is met, it will down shift the internal clock (SPCI, A-link, and B-link clock frequency). DFSlowSpeedSel selects either clock run at 50% of full speed or 25% of full speed. 0: Disable 1: Enable
IdleMonCEn	1	0	If this bit is set, the dynamic clock frequency logic will only consider the chip to be in idle state when CPU is in C state
IdlePeriodSel	3:2	01	Select interval for monitoring: 00: 53.76us 01: 302us 10: 2.29ms 11: 18.3ms
ForceSlowFreq	4	0	Force core logic clock run at lower frequency. IdleMonEn will let dynamic clock frequency logic monitor amount of idle-ness and do frequency down shift accordingly. Setting ForceSlowFreq will force core logic to run at 50% or 25% of full speed frequency with IdleMonEn disabled. (Secondary PCI, internal A-link , and B-link clock frequency) DFSlowSpeedSel select either clock run at 50% of full speed or 25% of full speed 0: Disable 1: Enable
DFSlowSpeedSel	5	0	Dynamic frequency Slow Speed selection. DFSlowSpeedSel selects either clock run at 50% of full speed or 25% of full speed 0: 50% of full speed 1: 25% of full speed
Reserved	7:6	0h	
IdleThreshold	15:8	80h	This defines the “idle-ness” threshold when the dynamic clock logic would downshift the clock frequency. Each unit represents 1/256 of the interval.
Reserved	23:16	00h	
IdleCount	31:24	--	This returns the idle count from the latest monitored period.

StrapStatus – R – 8/16/32 bits - [MISC_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
UseLpcRomStrap	1	1b	Inverted version from EcPwm2 pad Note: Both EcPwm3 and EcPwm2 straps pins are used to select boot ROM type.
IMCEnableStrap	2	0b	Enable IMC
BootFailTmrEnStrap	3	0b	Enable Watchdog function
ClkGenStrap	4	0b	Select 25Mhz crystal clock or 100Mhz PCI-E clock
DefaultModeStrap	5	1b	Select default debug straps
Reserved	6	-	Reserved
I2CRomStrap	7	0b	Getting UMI core strap from I2C ROM or using default value
ILAAutorunEnBStrap	8	1b	Enable trace memory auto run feature
FcPllBypStrap	9	1b	Bypass FC clock
PciPllBypStrap	10	0b	Bypass PCI PLL (used in functional test at tester)
ShortResetStrap	11	1b	Genearate short reset

StrapStatus – R – 8/16/32 bits - [MISC_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	12	1b	PCI_ROM_BOOT strap
FastBif2cClkStrap	13	0b	Select fast BIF EPROM clocks
Reserved	14	-	Reserved
BlinkSlowModestrap	15	0b	B-Link slow mode (100Mhz B-Link clock) strap
BIF_GEN2_COMPLIANCE_ Strap	16	0b	BIF gen 2 compliance strap
Reserved	31:17	4'h0000	Reserved

StrapOverride – R/W – 8/16/32 bits - [MISC_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
Override FWHDisableStrap	0	0b	Override FWHDiableStrap value from external pin.
Override UseLpcRomStrap	1	0b	Override UseLpcRomStrap value from external pin.
Override EcEnableStrap	2	0b	Override EcEnableStrap value from external pin.
Override BootFailTmrEnStrap	3	0b	Override BootFailTmrEnStrap value from external pin.
Reserved	4	0b	Reserved
Override DefaultModeStrap	5	0b	Override DefaultModeStrap value from external pin.
Reserved	6	0b	Reserved
Override I2CRomStrap	7	0b	Override I2CRomStrap value from external pin.
Override ILAAutorunEnBStrap	8	0b	Override ILAAutorunEnBStrap value from external pin.
Override FcPllBypStrap	9	0b	Override FcPllBypStrap value from external pin.
Override PciPllBypStrap	10	0b	Override PciPllBypStrap value from external pin.
Override ShortResetStrap	11	0b	Override ShortResetStrap value from external pin.
Reserved	12	0b	Reserved
Override FastBif2ClkStrap	13	0b	Override FastBif2ClkStrap value from external pin'
Reserved	14	0b	Reserved
PciRomBoot Strap	15	0b	Override PCI Rom Boot Strap value from external pin'
BlinkSlowModestrap	16	0b	Override B-Link Slow mode (100Mhz) from external pin'
ClkGenStrap	17	0b	Override CLKGEN from external pin.
BIF_GEN2_COMPL_Strap	18	0b	Override BIF_ GEN2_COMPLIANCE strap from external pin.
Reserved	30:19	0000h	Reserved
StrapOverrideEn	31	0b	Enable override strapping feature.

AutoTransaction - RW - 8 bits - [MISC_Reg:90h]			
Field Name	**Bits**	**Default**	**Description**
AutoExecute	0	0b	Writing this bit will cause the HW to execute the transaction defined by the definition below. Once it is written, this bit stays as 1 until the transaction is completed, in which case it will return to 0
DualAddr	1	0b	0: Use single address cycle 1: Use dual address cycle
ByteCount	3:2	00b	00: 1 byte 01: 2 bytes 10: 4 bytes 11: 4 bytes
TransactionType	7:4	0h	PCI Command type used for this transaction. For example, if this is programmed with a value of 3h, the transaction issue will be an IO write.

AllowEC - RW - 8 bits - [MISC_Reg:91h]			
Field Name	**Bits**	**Default**	**Description**
AllowIMCToAutoTransactEn	0	0b	When this bit is 0, IMC cannot write to any of registers relating to any of the registers in the Auto Transaction Generation logic. When this bit is 1, then IMC can change any of these bits. Only BIOS can change this bit.
DisableAuto	1	0b	If this bit is set, the entire AutoTransaction logic is disabled. Once this bit is set, it cannot be cleared except by system reset
AutoTriggerFromCpuEn	2	0b	If this bit is set, a falling edge on KSO15/XDB[1] will trigger the autotransaction logic
Reserved	7:3	00h	

AutoAddrLow - RW - 32 bits - [MISC_Reg:94h]			
Field Name	**Bits**	**Default**	**Description**
AutoAddrLow	31:0	0000_0000h	Low address to be used by the AutoExecute operation

AutoAddrHigh - RW - 32 bits - [MISC_Reg:98h]			
Field Name	**Bits**	**Default**	**Description**
AutoAddrHigh	31:0	0000_0000h	High address to be used by the AutoExecute operation. This register is only applicable when DualAddr = 1.

AutoData - RW - 32 bits - [MISC_Reg:9Ch]			
Field Name	**Bits**	**Default**	**Description**
AutoData	31:0	0000_0000h	If the operation is read, this register will return the read data. If the TransactionType is a write command, this register will contain the write data. Note byte is aligned accordingly.

CPU_Pstate0 – R – 8/16/32 bits - [Misc_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
Core0_PState	2:0	000b	FCH will monitor the P state of each CPU core (up to 16 cores) 000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core1_PState	6:4	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7

CPU_Pstate0 – R – 8/16/32 bits - [Misc_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
Core2_PState	10:8	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core3_PState	14:12	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core4_PState	18:16	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core5_PState	22:20	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core6_PState	26:24	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core7_PState	30:28	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7

CPU_Pstate1 – R – 8/16/32 bits - [Misc_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Core8_PState	2:0	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core9_PState	6:4	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core10_PState	10:8	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core11_PState	14:12	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core12_PState	18:16	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core13_PState	22:20	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core14_PState	26:24	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7

CPU_Pstate1 – R – 8/16/32 bits - [Misc_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Core15_PState	30:28	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7

CPU_Cstate0 – R – 8/16/32 bits - [Misc_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Core0_CState	2:0	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core1_CState	6:4	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core2_CState	10:8	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core3_CState	14:12	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core4_CState	18:16	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7

CPU_Cstate0 – R – 8/16/32 bits - [Misc_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Core5_CState	22:20	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core6_CState	26:24	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core7_CState	30:28	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7

CPU_Cstate1 – R – 8/16/32 bits - [Misc_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
Core8_CState	2:0	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core9_CState	6:4	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core10_CState	10:8	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7

CPU_Cstate1 – R – 8/16/32 bits - [Misc_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
Core11_CState	14:12	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core12_CState	18:16	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core13_CState	22:20	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core14_CState	26:24	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core15_CState	30:28	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7

SataPortSts – RW – 8/16/32 bits - [Misc_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
Port0Sts	0	-	This status bit indicates the internal status of each of the SATA port. The selected status of Port 0.
Port1Sts	1	-	The selected status of Port 1
Port2Sts	2	-	The selected status of Port 2
Port3Sts	3	-	The selected status of Port 3
Port4Sts	4	-	The selected status of Port 4
Port5Sts	5	-	The selected status of Port 5
Reserved	23:8	0000h	
SataPortSel	25:24	00b	00: Select “led” for Port 0 to 5 01: Select “det” for Port 0 to 5 10: Select “err” for Port 0 to 5 11: Select “led” for Port 0 to 5

SataPortSts – RW – 8/16/32 bits - [Misc_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:26	00h	

ClkCntrlSts – R – 8/16/32 bits - [Misc_Reg: F4h]			
Field Name	**Bits**	**Default**	**Description**
ClkBuffer_ImpCntl_Value	3:0	-	Clk buffer Impedance Control Value The impedance calibration logic (impctr_clkbuf) provides a 13-bit thermometer-coded control signal (impedance value) to clkgen_outpad and DP_Link, use the feedback from clkgen_outpad/CALRN to determine whether to increase or decrease this 13-bit control signal and calibrate the termination value to 50 Ohm. These 4 bits represent the thermometer code decoder value for the 13-bit impedance value.
IMPComparator_Status	4	-	Rx impedance calibration comparator output status from clk_buffer.

3.9 SMBus Registers

Register Name	Offset Address
SMBusStatus	00h
SMBusSlaveStatus	01h
SMBusControl	02h
SMBusHostCmd	03h
SMBusAddress	04h
SMBusData0	05h
SMBusData1	06h
SMBusBlockData	07h
SMBusSlaveControl	08h
SMBusShadowCmd	09h
SMBusSlaveEvent	0A-0Bh
SlaveData	0C-0Dh
SMBusTiming	0Eh
I2CbusConfig	10h
I2CCommand	11h
I2CShadow1	12h
I2Cshadow2	13h
SMBusAutoPoll	14h
SMBusCounter	15h
SMBusStop	16h
SMBusHostCmd2	17h

Note: The SMBus registers are located at the IO address space defined by PMIO register 0x2C, bits[15:5].

SMBusStatus - RW - 8 bits - [SMBUS:00h]			
Field Name	**Bits**	**Default**	Description
HostBusy	0	0b	This bit indicates the SMBus controller is in the process of completing a command. When this bit is set, software should not access any other SMBus registers. [Read-only]
SMBusInterrupt	1	0b	This bit is set by hardware to indicate the completion of the last host command. This bit can be cleared by writing a 1 to it.
DeviceErr	2	0b	This bit is set by hardware to indicate an error of one of the following: 1) illegal command field, 2) unclaimed cycle, 3) host device time-out. This bit can be cleared by writing a 1 to it.
BusCollision	3	0b	This bit is set by hardware to indicate an SMBus transaction collision; this bit can be cleared by writing a 1 to it.
Failed	4	0b	This bit is set by hardware to indicate a failed bus transaction, set when SMBusControl. Kill bit is set. This bit is cleared by writing a 1 to it.
Reserved	7:5	000b	Reserved

SMBusSlaveStatus - RW - 8 bits - [SMBUS:01h]			
Field Name	**Bits**	**Default**	Description
SlaveBusy	0	0b	This bit indicates the SMBus controller slave interface is in the process of receiving data. Software should not try to access any other SMBus register when this bit is set. [Read-only]
SlaveInit	1	0b	Writing a 1 to this bit will initialize the slave. It is unnecessary to write it back to 0. A read from it will always return a 0.
SlaveStatus	2	0b	This bit is set by hardware to indicate a slave cycle event match of the SMBus slave command and SMBus Slave Event match. This bit can be cleared by writing a 1 to it.
Shadow1Status	3	0b	This bit is set by hardware to indicate a slave cycle address match of the SMB_Shadow1 port. This bit can be cleared by writing a 1 to it.

Shadow2Status	4	0b	This bit is set by hardware to indicate a slave cycle address match of the SMB_Shadow2 port. This bit can be cleared by writing a 1 to it.
AlertStatus	5	0b	This bit is set by hardware to indicate an SMBALERT_ signal. Software needs to "write '1' to clear the status.
Reserved	7:6	00b	Reserved

SMBusControl - RW - 8 bits - [SMBUS:02h]			
Field Name	**Bits**	**Default**	Description
InterruptEnable	0	0b	Enable the generation of interrupts on the completion of current host transaction.
Kill	1	0b	Stop the current host transaction in process.
SMBusProtocol	4:2	000b	000: Quick Read or Write 001: Byte Read or Write 010: Byte Data Read or Write 011: Word Data Read or Write 100: Reserved 101: Block Read or Write 110: Reserved 111: Reserved
Reserved	5	0b	Reserved
Start	6	0b	Writing a 1 in this field initiates SMBus controller host interface to execute the command programmed in the SMBusProtocol field.
Reset	7	0b	Write only. Set the bit to 1 to stop smbus transaction and reset smbus controller state machine.

SMBusHostCmd - RW – 8 bits - [SMBUS:03h]			
Field Name	**Bits**	**Default**	Description
SMBusHostCmd	7:0	00h	This field contains the data transmitted in the command field of SMBus host transaction.

SMBusAddress - RW - 8 bits - [SMBUS:04h]			
Field Name	**Bits**	**Default**	Description
SMBusRdWr	0	0b	0:Execute a Write command 1: Execute a Read command
SMBusAddr	7:1	00h	This field contains the 7-bit address of the target slave device.

SMBusData0 - RW - 8 bits - [SMBUS:05h]			
Field Name	**Bits**	**Default**	Description
SMBusData0	7:0	00h	This register should be programmed with a value to be transmitted in the data 0 field of an SMBus host interface transaction. For Block Write commands, the count of the memory should be stored in this field. The value of this register is loaded into the block transfer count field. A valid value for block command count is between 1 and 32. For block reads, count received from SMBus device is stored here.

SMBusData1 - RW - 8 bits - [SMBUS:06h]			
Field Name	**Bits**	**Default**	Description
SMBusData1	7:0	00h	This register should be programmed with a value to be transmitted in the data 1 field of an SMBus host interface transaction. When SMBusPoll2Byte is set, and SMBusProtocol = Byte Read/Write or Byte Data Read/Write, this register is used as the data field in the second transaction.

SMBusBlockData - RW - 8 bits - [SMBUS:07h]			
Field Name	**Bits**	**Default**	Description
SMBusBlockData	7:0	00h	This register is used to transfer data into or out of the block data storage array.

SMBusSlaveControl - RW - 8 bits - [SMBUS:08h]			
Field Name	**Bits**	**Default**	Description
SlaveEnable	0	0b	Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the host controller slave port of 10h, a command field that matches the SMBus slave control register, and a match of corresponding enabled events.
SMBusShadow1En	1	0b	Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the SMBus Shadow 1 register.
SMBusShadow2En	2	0b	Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the SMBus Shadow 2 register.
SMBusAlertEnable	3	0b	Enable the generation of an interrupt or resume event on the assertion of AMBALERT_ signal. (This function is not supported). [Read-only]
HostSemaphore	4	0b	Bits 4 and 6 are meant to be used as software semaphore between the host and embedded controller. When both host and IMC want to use the same resource, they can write to these semaphore bits first, followed by a read. If the read returns a 1 in the semaphore bit, it means it has established the semaphore first. Write 1 to set this bit. This bit can only be set when EcSemaphore is clear. Writing 0 has no effect. Reading returns the value of this bit
ClrHostSemaphore	5	0b	Write 1 to clear HostSemaphore bit. Writing 0 has no effect and reading always returns 0
EcSemaphore	6	0b	Write 1 to set this bit. This bit can only be set when HostSemaphore is clear. Writing 0 has no effect. Reading returns the value of this bit
ClrEcSemaphore	7	0b	Write 1 to clear EcSemaphore bit. Writing 0 has no effect and reading always returns 0

SMBusShadowCmd - RW - 8 bits - [SMBUS:09h]			
Field Name	**Bits**	**Default**	Description
SMBusShadowCmd	7:0	00h	This field contains the command value that was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow ports.

SMBusSlaveEvent - RW - 16 bits - [SMBUS:0A-0Bh]			
Field Name	**Bits**	**Default**	Description
SMBusSlaveEvent	15:0	0000h	This field contains data bits used to compare against incoming data to the SMBus Slave Data register. When a bit in this register is 1 and a corresponding bit in SMBus Slave register is set, then an interrupt or resume event is generated if the command value matches the value in the SMBus slave control register and the access was to SMBus host address 10h.

SlaveData - RW - 16 bits - [SMBUS:0C-0Dh]			
Field Name	**Bits**	**Default**	Description
SlaveData	15:0	0000h	This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

SMBusTiming - RW - 8 bits - [SMBUS:0Eh]			
Field Name	**Bits**	**Default**	Description
SMBusTiming	7:0	B0h	This register controls the frequency on the SMBUS. The formula to calculate the frequency is: **Frequency = 66Mhz/(SmBusTiming * 4)**

I2CbusConfig - RW - 8 bits – [SMBUS: 10h]			
Field Name	**Bits**	**Default**	Description
I2CbusInterrupt	0	0b	0 : SMI# 1 : IRQ
I2CRevision	7:4	0000b	Sm bus controller revision
I2CbusConfig register: Registers D2-D5 control the interface when this chip is the I2C slave.			

I2CCommand - RW - 8 bits - [SMBUS: 11h]			
Field Name	**Bits**	**Default**	Description
I2Ccommand	7:0	00h	I2C Host Slave Command; this value specifies the command value to be matched for I2C master accesses to the I2Ccontroller host slave interface.

I2CShadow1- RW - 8 bits - [SMBUS: 12h]			
Field Name	**Bits**	**Default**	Description
Read/Write ShadowPort1	0	0b	Read/Write for Shadow Port 1 This bit must be programmed to 0 because I2C slave controller only responds to Word Write Transaction.
I2CslaveAddr1	7:1	00h	SMBus Slave Address for shadow port 1 This value specifies the address used to match against incoming I2C addresses for Shadow port 1.

I2Cshadow2- RW - 8 bits - [SMBUS: 13h]			
Field Name	**Bits**	**Default**	Description
Read/Write ShadowPort2	0	0b	Read/Write for Shadow Port 2 This bit must be programmed to 0 because I2C slave controller only responds to Word Write Transaction.
I2CslaveAddr2	7:1	00h	SMBus Slave Address for shadow port 2 This value specifies the address used to match against incoming I2C addresses for Shadow port 2.

SMBusAutoPoll - RW - 8 bits - [SMBUS:14h]			
Field Name	**Bits**	**Default**	**Description**
SMBusAutoPollEn	0	0b	When set, SMBUS will periodically execute the last command whenever SMBusCounter expires. The polling interval is defined by SMBusPollPeriod. The purpose of this function is to use the SMBUS to read CPU temperature via TSI. Values in offset 0x06 and 0x05 are to be used for controlling the fan speed
SMBusPollPeriod	3:1	010b	000b: poll every 1/16 second 001b: poll every 1/8 second 010b: poll every 1/ 4 second 011b: poll every 1/ 2 second 1xxb: poll every 1 second
Reserved	6:4	000b	Reserved
SMBusPoll2Byte	7	1b	When set, if SMBusProtocol = Byte Read/Write or Byte Data Read/Write, the last command will be performed twice at each polling interval. SMBusData1 contains data transmitted and retrieved from the second transaction. SMBusHostCmd2 contains data transmitted in the command field in the second transaction.

SMBusCounter - RO - 8 bits - [SMBUS:15h]			
Field Name	**Bits**	**Default**	**Description**
SMBusCounter	7:0	-	This counter shows the remaining time until the next read. The interval is based on SMBusPollPeriod. For example, if SMBusPollPeriod is 000b, then each tick in this counter represents 1/16 / 256 = 244us.

SMBusStop - RW - 8 bits - [SMBUS:16h]			
Field Name	**Bits**	**Default**	**Description**
SMBusPausePoll	0	0	This is to be used as a semaphore mechanism by software to stop the next polling. If SW wants to use the SMBUS for other purpose but the hardware has already been enabled (SMBusAutoPollEn=1) to perform auto polling, SW can halt the next polling by setting this bit to 1. If the halt is successful, this bit will return 1. If the HW has already started the polling operation at the same time SW tries to set this bit, this bit will return 0. When the pending polling operation is finally complete, this bit will then get set. When this bit is set, polling counter will temporarily stop (not reset). It is now safe for SW to access the SMBUS. Upon completion, SW must restore the previous command in the appropriate register prior to setting this bit. SW should also clear this bit so the counter can resume counting.

SMBusHostCmd2 - RW – 8 bits - [SMBUS:17h]			
Field Name	**Bits**	**Default**	Description
SMBusHostCmd2	7:0	00h	This field contains the data transmitted in the command field in the second command when SMBusPoll2Byte is set and SMBusProtocol = Byte Data Read or Write (3’b010).

3.10 ASF SMBus Host Interface Registers

The ASF SMBus host registers are located at the IO address space defined by PMIO register 0x28. In addition, they can be accessed through the system MMIO offset 0x900:9FF.

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Register Name	Offset Address
HostStatus	00h
HostControl	02h
HostCommand	03h
SlaveAddress	04h
Data0	05h
Data1	06h
Data	07h
PEC	08h
ListenAdr	09h
ASFStatus	0Ah
StatusMask0	0Bh
StatusMask1	0Ch
SlaveControl	0Dh
RemoteCtrlAdr	0Eh
DataReadPointer	10h
DataWritePointer	11h
SetDatareadpointer	12h
DataBankSel	13h
Semaphore	14h
SlaveEn	15h
DelayMasterTimer	16h

HostStatus – R - 8 bits - [ASF_IO: 00h]			
Field Name	**Bits**	**Default**	**Description**
HostBusy	0	0b	0: SM bus host is idle 1: SM bus host is busy
INTR	1	0b	This bit is set by termination of a command and can be cleared by writing a 1.
DevError	2	0b	0: Slave device behaving correctly 1: No ACK or Slave device behaving incorrectly
BusCollision	3	0b	0: No bus collision 1: Bus collision
PECError	4	0b	0: No CRC error 1: CRC error has occurred
Reserved	6:5	00b	Reserved
LastByte	7	0b	0: Last byte has not been received 1: Last byte has been received

HostControl – RW - 8 bits - [ASF_IO: 02h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
KillHost	1	0b	0: Enable SM master 1: Reset SM master
Protocol	4:2	000b	000: Quick 001: Byte 010: Byte Data 011: Word Data 100: Process call 101: Block 110: Block write-Block read-process call
PECAppend	5	0b	0: No PEC append 1: Automatic PEC append. ASF HC calculates CRC code and appends to the tail of the data packets.
Start	6	0b	WO: 0: Always read 0 on reads 1: Writing 1 to initiate the command
PECEnable	7	0b	0: PEC disable 1: PEC enable, enable CRC checking when ASF HC presents as SM master and SM slave.

HostCommand – RW - 8 bits - [ASF_IO: 03h]			
Field Name	**Bits**	**Default**	**Description**
HostCommand	7:0	00h	Command to be transmitted by master

SlaveAddress– RW - 8 bits - [ASF_IO: 04h]			
Field Name	**Bits**	**Default**	**Description**
RW	0	0b	0: Write 1: Read
Address	7:1	00h	Provide the SM address of slave

Data0– RW - 8 bits - [ASF_IO: 05h]			
Field Name	**Bits**	**Default**	**Description**
Data0	7:0	00h	Contains count or DATA0 field of transaction

Data1– RW - 8 bits - [ASF_IO: 06h]			
Field Name	**Bits**	**Default**	**Description**
Data1	7:0	00h	Contains DATA1 field of transaction

DataIndex– RW - 8 bits - [ASF_IO: 07h]			
Field Name	**Bits**	**Default**	**Description**
DataIndex	7:0	00h	Index to 32 Data registers.

PEC– RW - 8 bits - [ASF_IO: 08h]			
Field Name	**Bits**	**Default**	**Description**
PEC	7:0	00h	PEC byte to be sent to slave.

ListenAdr– RW - 8 bits - [ASF_IO: 09h]			
Field Name	**Bits**	**Default**	**Description**
ListenAdrEn	0	0	1: Enable ListenMode when the slave address equals to ListenAdr[7:1] 0: Disable ListenMode when the slave address equals to ListenAdr[7:1]
ListenAdr	7:1	00h	The slave address which ASF slave response as ListenMode.

ASFStatus – RW - 8 bits - [ASF_IO: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
SlaveBusy	7	0b	Indicate if ASF slave is receiving data
SlaveIntr	6	0b	ASF Slave interrupt Status. Can be cleared to 0 by writing 1.
Reserved	5:4	00b	Reserved
RemotePowerCycle	3	0b	1: Power cycle has been triggered by ASF. 0: No power cycle ASF event Can be cleared to 0 by writing 1.
RemotePowerUp	2	0b	1: Power up has been triggered by ASF. 0: No Power up ASF event Can be cleared to 0 by writing 1.
RemotePowerDown	1	0b	1: Power down has been triggered by ASF 0: no Power down ASF event Can be cleared to 0 by writing 1.
RemoteReset	0	0b	1: Reset has been triggered by ASF 0: no Reset cycle ASF event Can be cleared to 0 by writing 1.

StatusMask0– RW - 8 bits - [ASF_IO: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Temp0StatusEnable	0	0b	1: Report Temp0 status to ASF 0: No report
Temp1StatusEnable	1	0b	1: Report Temp1 status to ASF 0: No report
Temp2StatusEnable	2	0b	1: Report Temp2 status to ASF 0: No report
Temp3StatusEnable	3	0b	1: Report Temp3 status to ASF 0: No report
AMDSIStatusEnable	4	0b	1: Report AMDSI status to ASF 0: No report
FanSpeed0StatusEnable	5	0b	1: Report Fan0 Speed Status to ASF 0: No report
FanSpeed1StatusEnable	6	0b	1: Report Fan1 Speed Status to ASF 0: No report
FanSpeed2StatusEnable	7	0b	1: Report Fan2 Speed Status to ASF 0: No report

StatusMask1– RW - 8 bits - [ASF_IO: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
AnalogIo0StatusEnable	0	0b	1: Report AnalogIo0 status to ASF 0: No report
AnalogIo1StatusEnable	1	0b	1: Report AnalogIo1 status to ASF 0: No report
AnalogIo2StatusEnable	2	0b	1: Report AnalogIo2 status to ASF 0: No report
AnalogIo3StatusEnable	3	0b	1: Report AnalogIo3 status to ASF 0: No report
AnalogIo4StatusEnable	4	0b	1: Report AnalogIo4 status to ASF 0: No report
AnalogIo5StatusEnable	5	0b	1: Report AnalogIo5 status to ASF 0: No report
AnalogIo6StatusEnable	6	0b	1: Report AnalogIo6 status to ASF 0: No report
AnalogIo7StatusEnable	7	0b	1: Report AnalogIo7 status to ASF 0: No report

SlaveStatus- RW – 8 bits - [ASF_IO: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
SlavePECError	0	0b	RO 0: No PEC error 1: PEC error
SlaveBusCollision	1	0b	RO 0: No BusCollision 1: BusCollision happens
SlaveDevError	2	0b	RO 0: Expected response 1: Unexpected response
WrongSP	3	0b	RO 0: No SP error 1: No SP symbol is detected when bus turns to read
Reserved	7:4	0000b	

RemoteCtrlAdr– RW - 8 bits - [ASF_IO: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
RemoteCtrlAdr	7:1	00h	SM address of Remote Control device.

SensorAdr– RW - 8 bits - [ASF_IO: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
SensorAdr	7:1	00h	SM address of Sensor.

DataReadPointer– R - 8 bits - [ASF_IO: 10h]			
Field Name	**Bits**	**Default**	**Description**
DataReadPointer	7:0	00h	Current read pointer to the value specified in this register

DataWritePointer– R - 8 bits - [ASF_IO: 11h]			
Field Name	**Bits**	**Default**	**Description**
DataWritePointer	7:0	00h	Show current write pointer to the value specified in this register

SetDataReadPointer– RW - 8 bits - [ASF_IO: 12h]			
Field Name	**Bits**	**Default**	**Description**
SetDataReadPointer	7:0	00h	Force the current write pointer to the value specified in this register

DataBankSel – RW - 8 bits - [ASF_IO: 13h]			
Field Name	**Bits**	**Default**	**Description**
DataBank	1:0	0	Bit 0: 0: Data Bank 0 is the latest touched data bank. 1: Data Bank 1 is the latest touched data bank. Bit 1: 0: Data Bank still has space. 1: Data Bank is now full.
DataBank0_Full	2	0	0: Data Bank 0 is free. 1: Data Bank 0 is full. Writing 1 clears status.
DataBank1_Full	3	0	0: Data Bank 1 is free. 1: Data Bank 1 is full. Writing 1 clears status.
SetReadRevDataBank	5:4	00	00: Select to read data from Data Bank 0. 01: Select to read data from Data Bank 1 10: Select to read data from Data Bank 1 11: Select to read data from Data Bank 1
Reserved	6	0	Reserved
SetReadHostDataBank	7	0	0: Select to read data from Data Bank 0 or Data Bank 1 as decided by SetReadRevDataBank bits. 1: Select to read data from Host Data Bank.

Semaphore - RW - 4 bits - [ASF_IO:14h]			
Field Name	**Bits**	**Default**	**Description**
HostSemaphore	0	0b	Bits [0] and [2] are meant to be used as software semaphore between the host and the IMC. When both host and IMC want to use the same resource, they can write to these semaphore bits first, then followed by a read. If the read returns a 1 in the semaphore bit, it means it has established the semaphore first. Write 1 to set this bit. This bit can only be set when EcSemaphore is clear. Writing 0 has no effect. Read returns the value of this bit
ClrHostSemaphore	1	0b	Write 1 to clear HostSemaphore bit. Write 0 has no effect and read always returns 0
EcSemaphore	2	0b	Write 1 to set this bit. This bit can only be set when HostSemaphore is clear. Writing 0 has no effect. Read returns the value of this bit
ClrEcSemaphore	3	0b	Write 1 to clear EcSemaphore bit. Writing 0 has no effect and read always returns 0

SlaveEn - RW - 8 bits - [ASF_IO: 15h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved
SlaveIntrListenEn	1	0b	Set to 1 to allow ASF slave to generate slave interrupt when the address of received packet is the same as the one specified in ListenAdr register [ASF_IO:09h].
IntruderAlertStsEn	2	0b	RW: 0: FanSpeed2Status is returned 1: IntruderAlertSts is returned
SuspendSlave	3	0b	RW Write 1 to Suspend (stop) ASF Slave state machine
KillSlave	4	0b	RW Write 1 to reset Slave ASF Slave state machine
LegacySensorEn	5	0b	RW 0: Disable Legacy Sensor 1: Enable Legacy Sensor
TmrOutEn	6	0b	RW 0: Disable timer out function 1: Enable timer out function
FairArbEn	7	0b	RW 0: Disable Fair arbiter logic 1: Enable Fair Arbiter logic, which forces ASF master to give up SMBus for a certain time, specified in register at offset 16h.

DelayMasterTimer – RW - 8 bits - [ASF_IO: 16h]			
Field Name	**Bits**	**Default**	**Description**
FairArbTimer	7:0	10h	Specify how long ASF master has to wait before submitting next packet. Wait time = the value * 2us.

The following commands are supported for the ASF remote control. BIOS should report these values accordingly in the ASF table if the system supports ASF function.

ASF Commands		
	Control Command	**Control Data Value**
Reset	00h	00h
Power Up	01h	00h
Power Down	02h	00h
Power Cycle	03h	00h
Sensor polling	23h	00h

3.11 WatchDogTimer Registers

WatchDogTimer registers are located at the IO address space defined by PMIO register 0x48. In addition, they can be accessed through the system MMIO offset 0xB00:BFF

Register Name	Offset Address
WatchDogControl	00h
WatchDogCount	04h

WatchDogControl - RW - 32 bits - [WD_Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
WatchDogRunStopB	0	0b	This bit is used to control or indicate whether the watchdog is in the Running and Stopped states. 1: Watchdog is in the Running state 0: Watchdog is in the Stopped state If the watchdog is in the Stopped state and a 1 is written to bit [0], the watchdog moves to the Running state, but a count interval is not started until a 1 is written to bit [7]. If the watchdog is in the Running state, writing a 1 to bit 0 has no effect. The bit is only valid when the watchdog is enabled.
WatchDogFired	1	0b	A value of "1" indicates that the watchdog timer has expired and caused the current restart. The bit is cleared by writing a "1" to bit 1 in the Watchdog Control register. Writing a "0" has no effect. The bit is cleared by a power cycle or by the operating system and it must remain cleared for any restart that is not caused by the watchdog timer firing. The bit is only valid when the watchdog is enabled.
WatchDogAction	2	0b	This bit determines the action to be taken when the watchdog timer expires. 0: System reset 1: System power off The bit is only valid when the watchdog is enabled.
WatchDogDisable	3	0b	This bit reflects the state of the watchdog timer hardware. 0: Enable 1: Disable
Reserved	6:4		
WatchDogTrigger (WO)	7	0b	Write only. Setting this bit triggers the watchdog to start a new count interval, counting down from the value that was last written to the Watchdog Count Register. This bit is always read as zero. Setting this bit has no effect if the watchdog is disabled or stopped.
Reserved	31:8		

WatchDogCount - RW - 32 bits - [WD_Mem_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
WatchDogCount	15:0	----	This defines the countdown time for the counter. The units are defined in the Units field in the Watchdog Resource Table (WDRT). The maximum value is defined in the Max Count field in the WDRT. Reading this register returns in the current counter value.
Reserved	31:16		

3.12 High Precision Event Timers (HPET)

High Precision Event Timer registers are accessed by memory-mapped IOs. The base address is defined in PMIO register offset 50h. The HPET MMIO base address is FED0_0000h by default. The registers can also be accessed partially through the AcpiMmio registers that range from "AcpiMMioAddr" + 0xC00 to "AcpiMMioAddr" + 0xCff. (The base address "AcpiMMioAddr" is defined in PM_reg x24, with the default base address at "FED8_0000.")

Register Name	Offset Address
ID	000h
Config	010h
Interrupt Status	020h
Main_Counter	0F0h
Tmr0_Conf_Cap	100h
Tmr0_Comp	108h
Tmr1_Conf_Cap	120h
Tmr1_Comp	128h
Tmr2_Conf_Cap	140h
Tmr2_Comp	148h

ID - R - 64 bits - [HPET_Reg: 000h]			
Field Name	**Bits**	**Default**	**Description**
RevID	7:0	10h	Revision ID.
Num_Tmr_Cap	12:8	02h	Three timers are supported.
Counter_Size_Cap	13	0b	Main counter is 32-bits wide (and cannot operate in 64-bit mode).
Reserved	14	0b	Reserved.
Legacy_Cap	15	1b	Legacy replacement interrupt is supported.
VendorID	31:16	1022h	AMD vendor ID.
Counter_Clk_Period	63:32	0429B17Eh	Specifies the clock period of each HPET timer tick. HPET main counter runs at 14.31818 MHz. The unit is femptoseconds (10 ^ -15 seconds). **Note:** The value of this register can be modified through MISC_Reg: 34h.

Config - RW - 64 bits - [HPET_Reg: 010h]			
Field Name	**Bits**	**Default**	**Description**
TmrEn	0	0b	0: Pause main counter and disable all timer interrupts. 1: Allow main counter to run and allow timer interrupts if enabled.
LegacyEn	1	0b	If LegacyEn is set to 1b then: Timer0 interrupt goes to IRQ0 of PIC controller, INT2 of IoAPIC; Timer1 interrupt goes to IRQ8 of PIC controller, INT8 of IoAPIC.
Reserved	63:2	0h	Reserved.

Interrupt Status - RW - 64 bits - [HPET_Reg: 020h]			
Field Name	**Bits**	**Default**	**Description**
Tmr0IntrSts	0	0b	0: Timer0 interrupt is not active. 1: Timer0 interrupt is active. Write 1 to clear if timer0 is set to level-triggered mode. When set to edge-triggered mode, software should ignore this bit and always write 0b to this bit.
Tmr1IntrSts	1	0b	0: Timer1 interrupt is not active. 1: Timer1 interrupt is active. Write 1 to clear if timer1 is set to level-triggered mode. When set to edge-triggered mode, software should ignore this bit and always write 0b to this bit.
Tmr2IntrSts	2	0b	0: Timer2 interrupt is not active. 1: Timer2 interrupt is active. Write 1 to clear if timer2 is set to level-triggered mode. When set to edge-triggered mode, software should ignore this bit and always write 0b to this bit.
Reserved	63:3	0h	Reserved.

Main_Counter – RW - 64 bits - [HPET_Reg: 0F0h]			
Field Name	**Bits**	**Default**	**Description**
MainCounter	31:0	0h	32-bit main counter, increment by 1 on every clock. Counter should be written to only when halted.
Reserved	63:32	0h	Reserved.

Tmr<N>_Conf_Cap - R - 64 bits - [HPET_Reg: 100h + <N>*020h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved.
TmrIntTyp	1	0b	Control timer interrupt polarity: 0: Edge triggered 1: Level triggered
TmrIntEn	2	0b	Set to 1 to enable timer interrupt.
TmrTyp	3	0b	Select the timer interrupt type: 0: Non-periodic 1: Periodic
TmrTypCap	4	1b	The timer supports periodic interrupt delivery mode. Read only.
TmrSizeCap	5	0b	The timer is 32-bits wide. Read only.
TmrSetPer	6	0b	Set to 1 to allow software to set the timer's accumulator if the timer is set to periodic mode. The bit is automatically cleared when 'Comparator' is written by software.
Reserved	7	0b	Reserved.
Tmr32ModeEn	8	0b	64-bit timer is not supported. Read only.
TmrIntRoute	13:9	00h	These 5 bits specify which INT entry of IoAPIC the timer is routed to when LegacyEn is not set.
TmrFsbEn	14	0b	Set to 1 to enable FSB (Front Side Bus) delivery of interrupt.
TmrFsbCap	15	1b	FSB delivery is supported. Read only.
Reserved	31:16	0h	Reserved.

Tmr<N>_Conf_Cap - R - 64 bits - [HPET_Reg: 100h + <N>*020h]			
Field Name	**Bits**	**Default**	**Description**
TmrIntRouteCap	63:32	00C00000h	Indicates which INT entry of IoAPIC can be assigned to the timer interrupt. Read only.
Note: Hardware supports 3 timers, <N> is 0, 1 or 2.			

Tmr<N>_Comp - RW - 64 bits - [HPET_Reg: 108h + <N>*020h]			
Field Name	**Bits**	**Default**	**Description**
Comparator	31:0	FFFFFFFFh	The timer 32-bit wide comparator. **In non-periodic mode:** 'Comparator' is writeable. **In periodic mode:** 'Comparator' can be modified after TmrSetPer is set to 1. 'Comparator' is periodically incremented by the value last written to this register. By default, value is incremented by 0xFFFFFFFF.
Reserved	63:32	0h	Reserved.
Note: Hardware supports 3 timers, <N> is 0, 1 or 2.			

3.13 Real Time Clock (RTC)

For software compatibility, the RTC registers and RAM are accessed through IO ports 70h/71h and with the banks (Bank 0 and Bank 1) address selected, which are shown in the diagram below. Bank 0 is selected if DV0 = 0 (DV0 is the 5th bit of Register A) while Bank 1 is chosen if DV0 = 1. Although there are 2 banks defined, the first 64 bytes (00h – 3Fh) are identical in each bank and should return the same value. Note: when Bank 1 is selected, byte offsets 00h - 0Dh Time/Alarm/Control registers and byte offsets 0Eh - 3Fh User RAM are read-only.

There are extended RAM space, x80 ~ xFF, defined later and accessed in a different way. One way to access the extended RAM space from x80 ~ xFF is through the indirect access of Bank 1, offset 50h/53h, which is defined to be the ExtendedRAMAddressPort.

The RAM space can be viewed in an alternate mapping by setting PM_Reg: 0x57[5] = 1 (AltCmosMapEn). Under this configuration, RAM location 0x0E: 0x7F are accessible from Bank 0 and 0x8E:0xFF from Bank 1.

A third way to access the extended RAM is through IO port 72h/73h, which are defined as the address/data ports for the extended RAM space. These two ports do not use the Bank 0 / Bank 1 scheme. Memory can be accessed directly using the 8-bit address port. Use of the two IO ports 72h/73h to access the RTC RAM is highly recommended.

Note: Some RTC RAM space can be protected from read/write if corresponding bits are set to 1 in RTCProtect register (PCI_Reg 6Ah).

An additional 16 bytes of RAM space has been added to Bolton. Software will need to set PM_Reg: 0x57[6] =1 first and then access the space through IO port 72h/73h. Due to the physical construction of the memory cells, they are located at index 0x00 through 0x03, 0x40 through 0x43, 0x80 through 0x83, and 0xC0 through 0xC3. Care should be taken to make sure PM_Reg 0x57[6] is set back to 0 after access to OS, otherwise other applications will access the wrong location.

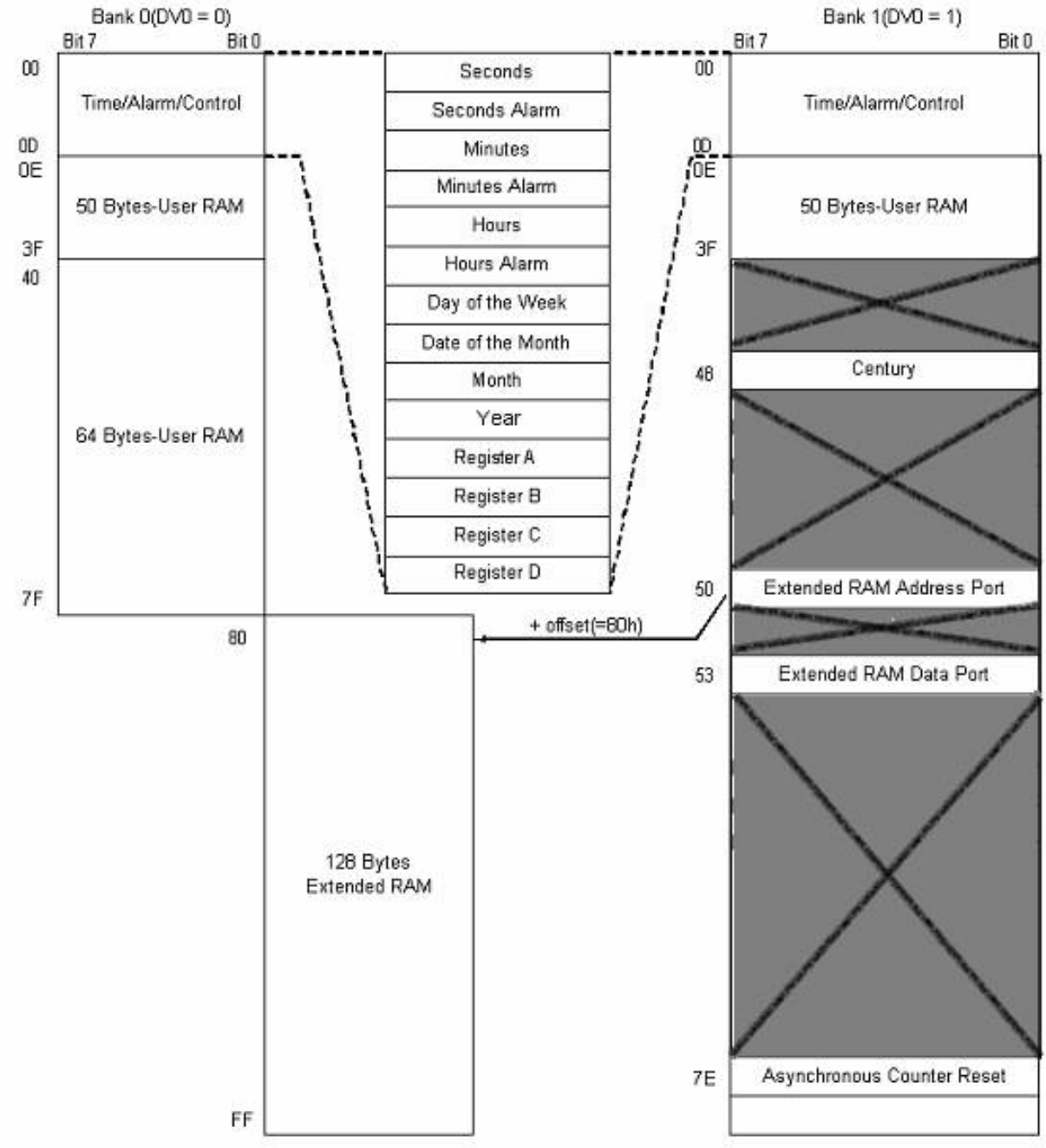

Figure 3-1. Register Bank Definition and Memory Address Mapping

The analog portion consists of two major parts: one is a 256-byte CMOS RAM and the other a 44-bit ripple counter.

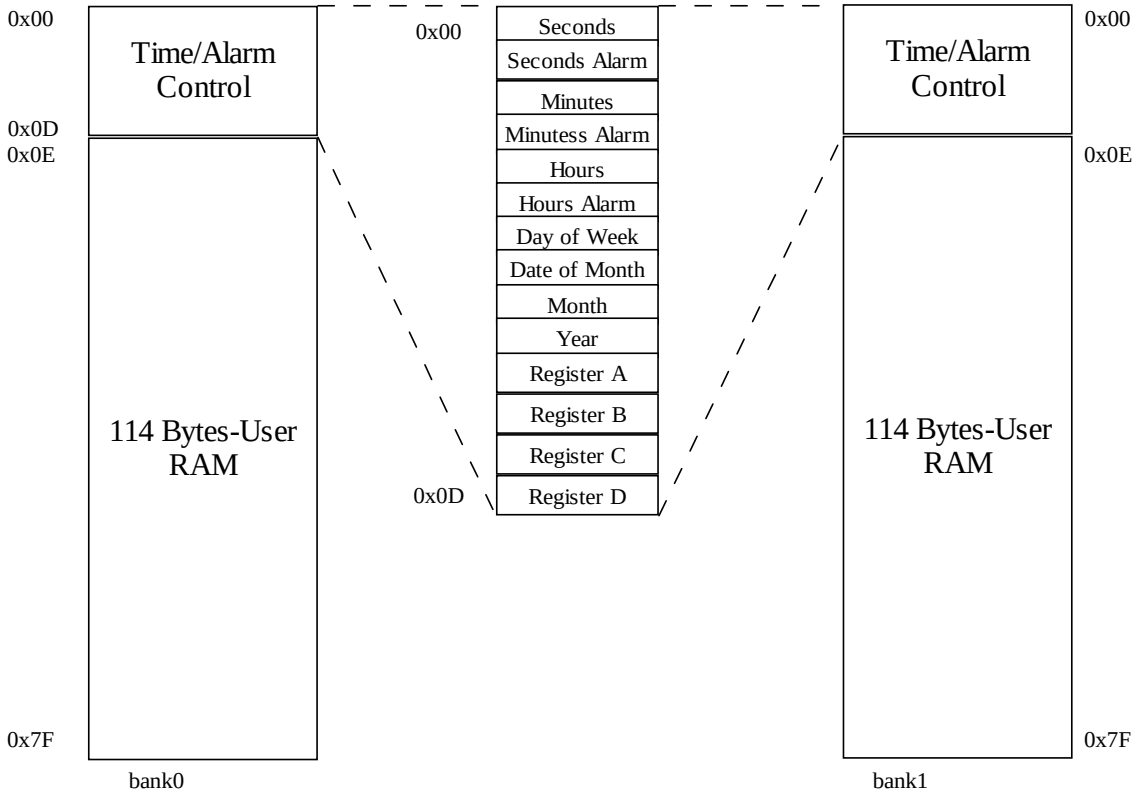

Figure 3-2. Alternate Memory Address Mapping

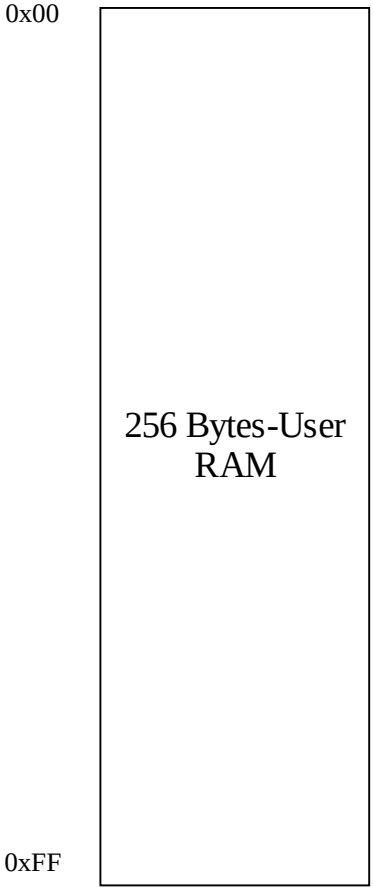

Figure 3-3. Memory Address Mapping through IO 0x72/73

Register Name	Offset Address
Seconds	00h
Seconds Alarm	01h
Minutes	02h
Minutes Alarm	03h
Hours	04h
Hours Alarm	05h
Day of Week	06h
Date of Month	07h
Month	08h
Year	09h
Register A	0Ah
Register B	0Bh
Register C	0Ch
Register D	0Dh
AltCentury (when DV0=0)	32h
Century (when DV0=1)	48h
Extended RAM Address Port	50h
Extended RAM Data Port	53h
RTC Time Clear	7Eh
RTC RAM Enable	7Fh

Note: Registers that are implemented in the internal RTC are described below.

Seconds - RW – 8 bits - [RTC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Seconds	7:0	00h	Binary-Code-Decimal format. Range:00 – 59 This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every second. When set by software, hardware updating is disabled.
Seconds register			

Seconds Alarm - RW – 8 bits - [RTC_Reg: 01h]			
Field Name	**Bits**	**Default**	**Description**
Seconds Alarm	7:0	00h	Binary-Code-Decimal format. If set bit = 1, the Seconds Alarm Register will never match with Seconds Register, else If bits [7:6] = [11], the Seconds Alarm Register always matches with Seconds Register.
Seconds Alarm register			

Minutes - RW – 8 bits - [RTC_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Minutes	7:0	00h	Binary-Code-Decimal format. Range:00 – 59 This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every minute. When set by software, hardware updating is disabled.
Minutes register			

Minutes Alarm - RW – 8 bits - [RTC_Reg: 03h]			
Field Name	**Bits**	**Default**	**Description**
Minutes Alarm	7:0	00h	Binary-Code-Decimal format. If set bit = 1, the Minutes Alarm Register will never match with Minutes Register, else If bits [7:6] = [11], the Minutes Alarm Register always matches with Minutes Register.
Minutes Alarm register			

Hours - RW – 8 bits - [RTC_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Hours	7:0	00h	Binary-Code-Decimal format. Range:00 – 23 This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every hour. When set by software, hardware updating is disabled.
Hours register			

Hours Alarm- RW – 8 bits - [RTC_Reg: 05h]			
Field Name	**Bits**	**Default**	**Description**
Hours Alarm	7:0	00h	Binary-Code-Decimal format. If set bit = 1, the Hours Alarm Register will never match with Hours Register, else If bits [7:6] = [11], the Hours Alarm Register always matches with Hours Register.
Hours Alarm register			

Day of Week - RW – 8 bits - [RTC_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Day of Week	7:0	00h	Binary-Code-Decimal format. Range: 01 – 07 (Sunday = 1). No leap year correction capability. Leap year correction has to be done by software. This register can be set by a software (set bit of Register B = 1) or can be automatically updated by hardware everyday. When set by software, hardware updating is disabled.
Day of Week register			

Date of Month - RW – 8 bits - [RTC_Reg: 07h]			
Field Name	**Bits**	**Default**	**Description**
Date of Month	7:0	00h	Binary-Code-Decimal format. Range: 01 – 28 for February and no leap year capability. Leap year correction has to be done by software. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware everyday. When set by software, hardware updating is disabled.
Date of Month register			

Month - RW – 8 bits - [RTC_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Month	7:0	00h	Binary-Code-Decimal format. Range: 01 – 12. No leap year correction capability. Leap year correction has to be done by software. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every month. When set by software, hardware updating is disabled.
Month register			

Year - RW – 8 bits - [RTC_Reg: 09h]			
Field Name	**Bits**	**Default**	**Description**
Year	7:0	00h	Binary-Code-Decimal format. Range: 00 – 99. No leap year correction capability. Leap year correction has to be done by software. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every year. When set by software, hardware updating is disabled.
Year register			

Register A - RW – 8 bits - [RTC_Reg: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
Rate Selection(RS0)	0	0b	These four rate-selection bits select one of the 13 taps on the 15-stage frequency divider or disable the divider output (flat output signal). The tap selected can be used to generate a periodic interrupt. See the following table for the frequency selection.
Rate Selection(RS1)	1	0b	
Rate Selection(RS2)	2	0b	
Rate Selection(RS3)	3	0b	
Bank Selection(DV0)	4	0b	DV0 = 0 selects Bank 0; DV0 = 1 selects Bank 1. The FCH has an alternate way to access the RAM without the use of bank select bit. Port 72/73 can be used as the index to access the full 256 bytes of RAM directly.
Reserved	6:5		
Update In Progress(UIP)	7	0b	If set bit = 1, UIP is cleared. If UIP = 1, the update transfer will soon occur. If UIP = 0, the update transfer will not occur for at least 244us. [Read-only]
Register A: Control register			

Rate Selection Bits				Tap Frequency(Interrupt Rate)
RS3	**RS2**	**RS1**	**RS0**	
0	0	0	0	Flat Signal(None)
0	0	0	1	256 Hz (3.90625 ms)
0	0	1	0	128 Hz (7.8125 ms)
0	0	1	1	8.192 kHz (122.070 us)
0	1	0	0	4.096 kHz (244.141 us)
0	1	0	1	2.048 kHz (488.281 us)
0	1	1	0	1.024 kHz (976.5625 us)
0	1	1	1	512 Hz (1.953125 ms)
1	0	0	0	256 Hz (3.90625 ms)
1	0	0	1	128 Hz (7.8125 ms)
1	0	1	0	64 Hz (15.625 ms)
1	0	1	1	32 Hz (31.25 ms)
1	1	0	0	16 Hz (62.5 ms)
1	1	0	1	8 Hz (125 ms)
1	1	1	0	4 Hz (250 ms)
1	1	1	1	2 Hz (500 ms)

Register B - RW – 8 bits - [RTC_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Daylight Saving Enable	0	0b	Both this bit and RtcExt_Reg: 00h bit[0] need to be set to 1 to enable RTC daylight saving feature.
HourMode	1	0b	Hour mode 0: 12 hour mode 1: 24 hour mode
Reserved	3:2	00	
Update Ended Interrupt Enable(UIE)	4	0b	UIE enables the Update End Flag (UF) bit in Register C to assert IRQ. If set bit = 1, UIE is cleared.
Alarm Interrupt Enable (AIE)	5	0b	AIE enables the Alarm Flag (AF) bit in Register C to assert IRQ.
Periodic Interrupt Enable (PIE)	6	0b	PIE enables the Periodic Interrupt Flag (PF) bit in Register C to assert IRQ.
Set new time (SET)	7	0b	If set bit = 1, no internal updating for Time Registers is allowed. If set bit = 0, the Time Registers are updated every second.

Register B - RW – 8 bits - [RTC_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Register B: Control register			

Register C - R – 8 bits - [RTC_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	
Update Ended Interrupt Flag(UF)	4	0b	This bit is set to one after each update cycle. Reading Register C clears UF.
Alarm Interrupt Flag (AF)	5	0b	This bit is set to one if second, minute and hour time has matched the second, minute and hour alarm time. Reading Register C clears AF bit.
Periodic Interrupt Flag (PF)	6	0b	This bit is set to one when an edge is detected on the selected tap (through RS3 to RS0) of the frequency divider. Reading Register C clears PF bit.
Interrupt Request Flag (IRQF)	7	0b	Logically, IRQF = (PF*PIE)+(AF*AIE)+(UF*UIE)+(WF*WIE) where WF and WIE are defined in Extended Control Register 4A and 4B. Reading Register C clears IRQF bit. Any time the IRQF bit is set to one, the #IRQ pin is driven low.
Register C: Control register			

DateAlarm - RW – 8 bits - [RTC_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
DateAlarm	5:0	00h	DateAlarm in BCD format and is considered when it is set to non-zero value. If this value is set to 0, then date is not compared for alarm generation.
Scratchbit	6	0b	
VRT	7	1b	Valid RAM and Time; refer to VRT_T1 and VRT_T2 registers (PMIO 3E/3F)
Date Alarm Register			

AltCentury - RW – 8 bits - [RTC_Reg: 32h]			
Field Name	**Bits**	**Default**	**Description**
AltCentury	7:0	00h	(This register is accessed only when DV0=0 and PM_Reg 7Ch Bit4=1.) Binary-Code-Decimal format. Leap year correction is done through hardware. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every century. When set by software, hardware updating is disabled.
AltCentury Register			

Century - RW – 8 bits - [RTC_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
Century	7:0	00h	(This register is accessed only when DV0=1) Binary-Code-Decimal format. Leap year correction is done through hardware. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every century. When set by software, hardware updating is disabled.
Century Register			

Extended RAM Address Port - RW – 8 bits - [RTC_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
ExtendedRAMAddr	6:0	00h	Because only 7 address bits are used in port x70, only lower 128 bytes are accessible through port x71. The Extended RAM (upper 128 bytes) are physically located at address 80H to FFH. In order to access these address, an address offset should be programmed into this register and access them through Extended RAMDataPort. (An offset of x80H will automatically add to this 7-bit address).
Reserved	7		
Extended RAM Address Port register: The address port to access Extended RAM.			

Extended RAM Data Port - RW – 8 bits - [RTC_Reg: 53h]			
Field Name	**Bits**	**Default**	**Description**
Extended RAM Data Port	7:0	xxxxxxxx	There is no physical register corresponding to this data port but the data port address is used for decoding to generate appropriate internal control signals.
Extended RAM Data Port register.			

RTC Time Clear - RW – 8 bits - [RTC_Reg: 7Eh]			
Field Name	**Bits**	**Default**	**Description**
RtcTimeClear	0	0b	Setting this bit will clear the RTC second and RTC time will stop
Reserved	7:1	0000000b	
RTC Time Clear register.			

RTC RAM Enable - RW – 8 bits - [RTC_Reg: 7Fh]			
Field Name	**Bits**	**Default**	**Description**
RtcRamEnable	0	1b	Setting this bit will enable access to the RTC RAM
Reserved	7:1	0000000b	
RTC RAM Enable register.			

3.14 RTC Extended Registers

The RTC extended register block is accessed through PM_Reg: 5E/5F Index/Data port.

Register Name	Offset Address
DltSavEnable	00h
SprFwdCtrl	01h
SprFwdMonth	02h
FallBackCtrl	03h
FallBackMonth	04h

DltSavEnable – RW – 8 bits – [RtcExt_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
DltSavEnable	0	-	Set to 1 to enable RTC daylight saving feature.
Reserved	7:6		
DltSavEnable register			

SprFwdCtrl – RW – 8 bits – [RtcExt_Reg: 01h]			
Field Name	**Bits**	**Default**	**Description**
SprFwdHour	5:0	-	This BCD value determines which hour (24 hour mode) to do the “spring forward”. Setting of 02h means 2am. Default is 00h which also denotes 2am. Spring forward is usually 2am in United States and 1am in Europe.
SprFwdWeek	6	-	This value determines which Sunday morning to do the “spring forward”. Default is 0 which denotes the 1st week. Setting of 1 means the last week of the month. Spring forward is usually at the 1st Sunday of April in United States and last Sunday of March in Europe.
Reserved	7		
SprFwdCtrl register			

SprFwdMonth – RW – 8 bits – [RtcExt_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
SprFwdMonth	4:0	-	This BCD value determines which month to “spring forward”. Setting of 04h means April. Default is 00h, which also denotes April. Spring forward is usually at April in United States and March in Europe.
Reserved	7:5		
SprFwdMonth register			

FallBackCtrl – RW – 8 bits – [RtcExt_Reg: 03h]			
Field Name	**Bits**	**Default**	**Description**
FallBackHour	5:0	-	This BCD value determines which hour (24 hour mode) to do the “fall back”. Setting of 02h means 2am. Default is 00h which also denotes 2am. Fall back is usually 2am in United States and 1am in Europe.
FallBackWeek	6	-	This value determines which Sunday morning to do the “fall back”. Default is 0 which denotes the last week. Setting of 1 means the first week of the month. Fall back is usually at the last Sunday of October in both United States and Europe.
Reserved	7		
FallBackCtrl register			

FallBackMonth – RW – 8 bits – [RtcExt_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
FallBackMonth	4:0	-	This BCD value determines which month to “fall back”. Setting of 10h means October. Default is 00h which also denotes October. Fall back is usually at October in both United States and Europe.
Reserved	7:5		
FallBackMonth register			

3.14.1Week Timer Registers

The 16-bit Week Timer is a battery-powered down counter timer that supports 1ms, 1 second, and 1minute resolution and auto reloads when the timer reaches 0. The WEEK_ALRM interrupt is asserted when the timer reaches 0 and stays asserted until the timer is disabled. The Week Timer registers are located in RTC extended register block index 10h through 14h.

WeekTimerControl – RW – 8 bits – [RtcExt_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Enable	0	-	This bit is used to start and stop the Week Timer. 0: Disable 1: Enable
Resolution	2:1	-	These bits are used to control the resolution of the Week Timer counter. 00: 1 minute 01: 1 second 10: 1ms 11: Reserved
Reserved	7:3		
Note: The Enable should be cleared when changing the Resolution setting.			

WeekTimerReloadLow – RW – 8 bits – [RtcExt_Reg: 11h]			
Field Name	**Bits**	**Default**	**Description**
WeekTimerReloadLow	7:0	-	This register is used to program the lower 8 bits of the 16-bit WeekTimerReload register. Writing the WeekTimerReloadLow register causes the 16-bit WeekTimerReload to be written into the Week Timer.
Note: The Enable in the WeekTimerControl register should be cleared before performing a write access to the WeekTimerReloadLow or WeekTimerReload High register.			

WeekTimerReloadHigh – RW – 8 bits – [RtcExt_Reg: 12h]			
Field Name	**Bits**	**Default**	**Description**
WeekTimerReloadHigh	7:0	-	This register is used to program the upper 8 bits of the 16-bit WeekTimerReload register. This register should be programmed before writing the WeekTimerReloadLow register.
Note: The Enable in the WeekTimerControl register should be cleared before performing a write access to the WeekTimerReloadLow or WeekTimerReload High register.			

WeekTimerDataLow – R – 8 bits – [RtcExt_Reg: 13h]			
Field Name	**Bits**	**Default**	**Description**
WeekTimerDataLow	7:0	-	This register is used to read the current state of the 16-bit Week Timer. Reading from the WeekTimerDataLow register returns the lower 8 bits of the 16-bit Week Timer and cause the upper 8 bits to be latched into the WeekTimerDataHigh register.
Note: Two reads are required to read the current state of the 16-bit Week Timer: the first read from the WeekTimerDataLow register returns the lower 8 bits of the 16-bit Week Timer and the second read from the WeekTimerDataHigh register return the upper 8 bits of the 16-bit Week Timer.			

WeekTimerDataHigh – R – 8 bits – [RtcExt_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
WeekTimerDataHigh	7:0	-	This register is used to read the current state of the 16-bit Week Timer. Reading from the WeekTimerDataHigh register returns the upper 8 bits of the 16-bit Week Timer latched by a previous read from the WeekTimerDataLow register.
Note: Two reads are required to read the current state of the 16-bit Week Timer: the first read from the WeekTimerDataLow register returns the lower 8 bits of the 16-bit Week Timer and the second read from the WeekTimerDataHigh register return the upper 8 bits of the 16-bit Week Timer.			

3.15 Legacy Block Registers

The following legacy blocks are in the IO-mapped address space. These registers control the legacy functions such as DMA, timers, PIC, interrupt routing for PIC, RTC, and the Bolton specific control registers.

3.15.1IO-Mapped Control Registers

Register Name	IO Address
Dma_Ch 0	00h
Dma_Ch 1	02h
Dma_Ch 2	04h
Dma_Ch 3	06h
Dma_Status	08h
Dma_WriteRequest	09h
Dma_WriteMask	0Ah
Dma_WriteMode	0Bh
Dma_Clear	0Ch
Dma_MasterClr	0Dh
Dma_ClrMask	0Eh
Dma_AllMask	0Fh
IntrCntrlReg1	20h
IntrCntrlReg2	21h
TimerCh0	40h
TimerCh1	41h
TimerCh2	42h
Tmr1CntrlWord	43h
Nmi_Status	61h
Nmi_Enable	70h
RtcDataPort	71h
AlternatRtcAddrPort	72h
AlternatRtcDataPort	73h
Dma_PageCh2	81h
Dma_PageCh3	82h
Dma_PageCh1	83h
Dma_Page_Reserved1	84h
Dma_Page_Reserved2	85h
Dma_Page_Reserved3	86h
Dma_PageCh0	87h
Dma_Page_Reserved4	88h
Dma_PageCh6	89h
Dma_PageCh7	8Ah
Dma_PageCh5	8Bh
Dma_Page_Reserved5	8Ch
Dma_Page_Reserved6	8Dh
Dma_Page_Reserved7	8Eh
Dma_Refresh	8Fh
FastInit	92h
IntrCntrl2Reg1	A0h
IntrCntrl2Reg2	A1h
Dma2_Ch4Addr	C0h
Dma2_Ch4Cnt	C2h
Dma2_Ch5Addr	C4h
Dma2_Ch5Cnt	C6h
Dma2_Ch6Addr	C8h
Dma2_Ch6Cnt	CAh
Dma2_Ch7Addr	CCh
Dma2_Ch7Cnt	CEh
Dma_Status	D0h
Dma_WriteRequest	D2h
Dma_WriteMask	D4h
Dma_WriteMode	D6h
Dma_Clear	D8h

Register Name	IO Address
Dma_Clear	DAh
Dma_ClrMask	DCh
Dma_ClrMask	DEh
NCP_Error	F0h
Reserved	40Bh
IntrEdgeControl	4D0h
Reserved	4D6h
Pci_Intr_Index	C00h
Pci_Intr_Data	C01h
Pci_Error	C14h
Isa_Misc	C6Fh
PM2_Index	CD0h
PM2_Data	CD1h
BIOSRAM_Index	CD4h
BIOSRAM_Data	CD5h
PM_Index	CD6h
PM_Data	CD7h

Note: The PCI I/O registers are 32-bit registers decoded from the full 32-bit PCI address and C/BE[3:0]#. Therefore, the bytes within a 32-bit address are selected with the valid byte enables. Registers and bits within a register marked as reserved are not implemented. Writes have no effect on reserved registers. All PCI I/O registers can be accessed via 8, 16, or 32-bit cycles (i.e., each byte is individually selected by the byte enables).

Dma_Ch 0- RW – 16 bits - [IO_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Ch 0	15:0	0000h	DMA1 Ch0 Base and Current Address
Dma_Ch 0 register			

Dma_Ch 1- RW – 16 bits - [IO_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Ch 1	15:0	0000h	DMA1 Ch1 Base and Current Address
Dma_Ch 1 register			

Dma_Ch 2- RW – 16 bits - [IO_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Ch 2	15:0	0000h	DMA2 Ch2 Base and Current Address
Dma_Ch 2 register			

Dma_Ch 3- RW – 16 bits - [IO_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Ch 3	15:0	0000h	DMA1 Ch3 Base and Current Address
Dma_Ch 3 register			

Dma_Status- RW – 8 bits - [IO_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Status	7:0	00h	Returns status when read; command for write
Dma_Status register			

Dma_WriteRequest- RW – 8 bits - [IO_Reg: 09h]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteRequest	7:0	00h	Request register.
Dma_WriteRequest register			

Dma_WriteMask- RW – 8 bits - [IO_Reg: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteMask	7:0	00h	Channel mask register.
Dma_WriteMask register			

Dma_WriteMode- RW – 8 bits - [IO_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteMode	7:0	00h	Mode register.
Dma_WriteMode register			

Dma_Clear- RW – 8 bits - [IO_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Dma_Clear	7:0	00h	Channel 0-3 DMA clear byte pointer
Dma_Clear register			

Dma_MasterClr- RW – 8 bits - [IO_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Dma_MasterClr	7:0	00h	Intermediate register.
Dma_MasterClr register			

Dma_ClrMask- RW – 8 bits - [IO_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Dma_ClrMask	7:0	00h	Channel 0-3 DMA Clear Mask
Dma_ClrMask register			

Dma_AllMask- RW – 8 bits - [IO_Reg: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
Dma_AllMask	7:0	00h	Mask register.
Dma_AllMask register			

IntrCntrl1Reg1- RW – 8 bits - [IO_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
IntrCntrl1Reg1	7:0	00h	IRQ0 – IRQ7: Read IRR, ISR Write ICW1, OCW2, OCW3
IntrCntrl1Reg1register			

IntrCntrl1Reg2- RW – 8 bits - [IO_Reg: 21h]			
Field Name	**Bits**	**Default**	**Description**
IntrCntrl1Reg2	7:0	00h	IRQ0 – IRQ7: Read IMR Write ICW2, ICW3, ICW4, OCW1
IntrCntrl1Reg2 register			

IMCR_Index- RW – 8 bits - [IO_Reg: 22h]			
Field Name	**Bits**	**Default**	**Description**
IMCR_Index	7:0	00h	The IMCR is supported by two read/writeable IO ports 22/23h; which are used as index and data port respectively. The actual IMCR register is located at index 70h.
IMCR_Index register			

IMCR_Data- RW – 8 bits - [IO_Reg: 23h]			
Field Name	**Bits**	**Default**	**Description**
IMCR_Data	7:0	00h	The IMCR is supported by two read/writeable IO ports 22/23h; which are used as index and data port respectively. The actual IMCR register is located at index 70h and it is at bit 0. The actual IMCR bit can only be accessed when bit port 22 is set to 70h. Default value of IMCR is 0.
IMCR_Data register			

TimerCh0- RW – 8 bits - [IO_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
TimerCh0	7:0	00h	8254 Timer 1: Counter 0 Data Port This timer is known as the System Clock timer and it is always on. It is clocked internally by OSC/12 (1.19318MHz), and asserts IRQ0 every time the timer rolls over. This timer is used for time-of-day, diskette time-out, and other system timing functions.
TimerCh0 register			

TimerCh1- RW – 8 bits - [IO_Reg: 41h]			
Field Name	**Bits**	**Default**	**Description**
TimerCh1	7:0	00h	8254 Timer 1: Counter 1 Data Port This timer is normally used for ISA refresh cycles and is also clocked by OSC/12 (1.19818MHz). Since this refresh function is no longer needed (we don't have an external ISA bus), it can be used as a general purpose timing function.
TimerCh1 register			

TimerCh2- RW – 8 bits - [IO_Reg: 42h]			
Field Name	**Bits**	**Default**	**Description**
TimerCh2	7:0	00h	8254 Timer 1: Counter 2 Data Port This is the speaker tone generator and is enabled by IO port 61H. It is clocked by OSC/12 (1.19318MHz) and directly drives the output SPKR that goes to a speaker.
TimerCh2 register			

Tmr1CntrlWord - RW – 8 bits - [IO_Reg: 43h]			
Field Name	**Bits**	**Default**	**Description**
CntDownSelect	0	0b	0: Binary countdown 1: BCD countdown
ModeSelect	3:1	000b	000: Asserts OUT signal at end of count 001: Hardware re-triggerable one-shot 010: Rate generator 011: Square wave output 100: Software triggered strobe 101: Hardware triggered strobe 110 – 111: Not used
CmmandSelect	5:4	00b	00: Counter latch command 01: Read/write least significant byte 10: Read/write most significant byte 11: Read/write least, and then most significant byte
CounterSelect	7:6	00b	00: Select counter 0 01: Select counter 1 10: Select counter 2 11: Read back command
Tmr1CntrlWord register: This is the control word to access the 8254 timer 1. It is used to select which counter will be accessed and how it will be accessed. This register specifies the counter, the operating mode, the order and size of the count value, and whether it counts down in a 16 bit or BCD format. If a counter is programmed to read or write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter; otherwise, the counter will be loaded with an incorrect value. The count must always be completely loaded with both bytes.			

Nmi_Status - RW – 8 bits - [IO_Reg: 61h]			
Field Name	**Bits**	**Default**	**Description**
SpkrEnable	0	0b	0: Disable counter 2 1: Enable counter 2
SpkrTmrEnable	1	0b	0: Speaker timer off 1: Speaker timer on
Parity_Nmi_En	2	1b	0: Enable Parity Error to NMI generation (from SERR# or PERR#) 1: Disable Parity Error to NMI generation and clear bit 7
Iochk_Nmi_En	3	1b	0: Enable IoChk to NMI generation 1: Disable IoChk to NMI generation
RefClk	4	-	The output of the counter 1 (8254). [Read-only]
SpkrClk	5	-	The output of the counter 2. [Read-only]
IoChk_Nmi	6	-	NMI is triggered by serial IOCHK. [Read-only]
ParErr_Nmi	7	-	NMI is caused by parity error (either PERR# or SERR#). [Read-only]
Nmi_Status register: Independent read and write registers will be accessed at this port. When writing to port 61H, bits[3:0] allow software to enable/disable parity error NMI's and control the speaker timer. When reading port 61H, status on parity errors, speaker count, speaker control and refresh cycles is returned.			

Nmi_Enable - RW – 8 bits - [IO_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
RTC Address Port	6:0	00h	This is used with either internal RTC or external RTC
NmiEnable	7	0b	0: NMI enable 1: NMI disable [Write-only]
Nmi_Enable register			

RtcDataPort - RW – 8 bits - [IO_Reg: 71h]			
Field Name	**Bits**	**Default**	**Description**
RTC Data Port	7:0	00h	This is used with either internal RTC or external RTC
RtcDataPort			

AlternatRtcAddrPort - RW – 8 bits - [IO_Reg: 72h]			
Field Name	**Bits**	**Default**	**Description**
AlternatRTCAddrPort	7:0	00h	This is used with internal RTC. This port allows user to specify the full 8 bit address (instead of bank0/bank1 indexing) to access the 256 byte RTC RAM
AlternatRtcAddrPort			

AlternatRtcDataPort - RW – 8 bits - [IO_Reg: 73h]			
Field Name	**Bits**	**Default**	**Description**
AlternatRTC Data Port	7:0	00h	This is used with internal RTC in conjunction with port h72
AlternatRtcDataPort			

Dma_PageCh2 - RW – 8 bits - [IO_Reg: 81h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh2	7:0	00h	DMA2 ch 2 page register
Dma_PageCh2 register			

Dma_PageCh3 - RW – 8 bits - [IO_Reg: 82h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh3	7:0	00h	DMA2 ch 3 page register
Dma_PageCh3 register			

Dma_PageCh1 - RW – 8 bits - [IO_Reg: 83h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh1	7:0	00h	DMA2 ch 1 page register
Dma_PageCh1 register			

Dma_Page_Reserved1- RW – 8 bits - [IO_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved1	7:0	00h	DMA Page Reserved1 register
Dma_Page_Reserved1 register			

Dma_Page_Reserved2- RW – 8 bits - [IO_Reg: 85h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved2	7:0	00h	DMA Page Reserved2 register
Dma_Page_Reserved2 register			

Dma_Page_Reserved3- RW – 8 bits - [IO_Reg: 86h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved3	7:0	00h	DMA Page Reserved3 register
Dma_Page_Reserved3 register			

Dma_PageCh0 - RW – 8 bits - [IO_Reg: 87h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh0	7:0	00h	DMA2 ch 0 page register
Dma_PageCh0 register			

Dma_Page_Reserved4- RW – 8 bits - [IO_Reg: 88h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved4	7:0	00h	Dma Page Reserved4 register
Dma_Page_Reserved4 register			

Dma_PageCh6 - RW – 8 bits - [IO_Reg: 89h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh6	7:0	00h	DMA2 ch 6 page register
Dma_PageCh6 register			

Dma_PageCh7 - RW – 8 bits - [IO_Reg: 8Ah]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh7	7:0	00h	DMA2 ch 7 page register
Dma_PageCh7 register			

Dma_PageCh5 - RW – 8 bits - [IO_Reg: 8Bh]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh5	7:0	00h	DMA2 ch 5 page register
Dma_PageCh5 register			

Dma_Page_Reserved5- RW – 8 bits - [IO_Reg: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved5	7:0	00h	Dma Page Reserved5 register
Dma_Page_Reserved5 register			

Dma_Page_Reserved6- RW – 8 bits - [IO_Reg: 8Dh]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved6	7:0	00h	Dma Page Reserved6 register
Dma_Page_Reserved6 register			

Dma_Page_Reserved7- RW – 8 bits - [IO_Reg: 8Eh]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved7	7:0	00h	Dma Page Reserved7 register
Dma_Page_Reserved7 register			

Dma_Refresh- RW – 8 bits - [IO_Reg: 8Fh]			
Field Name	**Bits**	**Default**	**Description**
Dma_Refresh	7:0	00h	DMA2 ch4 page register.
Dma_Refresh register			

FastInit- RW – 8 bits - [IO_Reg: 92h]			
Field Name	**Bits**	**Default**	**Description**
FastInit	0	0b	FAST_INIT. This read/write bit provides a fast software executed processor reset function. Writing a 1 to this bit will cause the INIT assertion for approximately 4ms. Before another INIT pulse can be generated via this register, this bit must be written back to a 0.
A20EnB	1	0b	A20Enable Bar bit; if set to 1 A20M# function is disabled.

IntrCntrl2Reg1- RW – 8 bits - [IO_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
IntrCntrl2Reg1	7:0	00h	IRQ8 – IRQ15: Read IRR, ISR Write ICW1, OCW2, OCW3
IntrCntrl2Reg1 register			

IntrCntrl2Reg2- RW – 8 bits - [IO_Reg: A1h]			
Field Name	**Bits**	**Default**	**Description**
IntrCntrl2Reg2	7:0	00h	IRQ8 – IRQ15: Read IMR Write ICW2, ICW3, ICW4, OCW1
IntrCntrl2Reg2 register			

Dma2_Ch4Addr - RW – 8 bits - [IO_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch4Addr	7:0	00h	DMA2 Ch4 Base and Current Address
Dma2_Ch4Addr register			

Dma2_Ch4Cnt – RW – 8 bits - [IO_Reg: C2h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch4Cnt	7:0	00h	DMA2 Ch4 Base and Current Count
Dma2_Ch4Cnt register			

Dma2_Ch5Addr - RW – 8 bits - [IO_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch5Addr	7:0	00h	DMA2 Ch5 Base and Current Address
Dma2_Ch5Addr register			

Dma2_Ch5Cnt - RW – 8 bits - [IO_Reg: C6h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch5Cnt	7:0	00h	DMA2 Ch4 Base and Current Count
Dma2_Ch5Cnt register			

Dma2_Ch6Addr - RW – 8 bits - [IO_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch6Addr	7:0	00h	DMA2 Ch6 Base and Current Address
Dma2_Ch6Addr register			

Dma2_Ch6Cnt - RW – 8 bits - [IO_Reg: CAh]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch6Cnt	7:0	00h	DMA2 Ch6 Base and Current Count
Dma2_Ch6Cnt register			

Dma2_Ch7Addr - RW – 8 bits - [IO_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch7Addr	7:0	00h	DMA2 Ch5 Base and Current Address
Dma2_Ch7Addr register			

Dma_Ch7Cnt - RW – 8 bits - [IO_Reg: CEh]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch7Cnt	7:0	00h	Channel 7 DMA base and current count
Dma2_Ch7Cnt register			

Dma_Status - RW – 8 bits - [IO_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Status	7:0	00h	DMA2 status register
Dma_Status register			

Dma_WriteRequest - RW – 8 bits - [IO_Reg: D2h]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteRequest	7:0	00h	DMA2 request register
Dma_WriteRequest register			

Dma_WriteMask - RW – 8 bits - [IO_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteMask	7:0	00h	DMA2 channel mask register
Dma_WriteMask register			

Dma_WriteMode - RW – 8 bits - [IO_Reg: D6h]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteMode	7:0	00h	DMA2 mode register
Dma_WriteMode register			

Dma_Clear - RW – 8 bits - [IO_Reg: D8h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Clear	7:0	00h	Channel 4-7 clear byte pointer
Dma_Clear register			

Dma_Clear - RW – 8 bits - [IO_Reg: DAh]			
Field Name	**Bits**	**Default**	**Description**
Dma_Clear	7:0	00h	Channel 4-7 DMA master clear
Dma_Clear register			

Dma_ClrMask - RW – 8 bits - [IO_Reg: DCh]			
Field Name	**Bits**	**Default**	**Description**
Dma_ClrMask	7:0	00h	Channel 4-7 DMA Clear Mask
Dma_ClrMask register			

Dma_ClrMask - RW – 8 bits - [IO_Reg: DEh]			
Field Name	**Bits**	**Default**	**Description**
Dma_AllMask	7:0	00h	DMA2 mask register
Dma_AllMask register			

NCP_Error - RW – 8 bits - [IO_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	6:0	00h	
WarmBoot	7	0b	Warm or cold boot indicator 0: Cold 1: Warm, this bit is set when any value is written to this register;
NCP_Error register: In addition to the WarmBoot function, writing to this port will assert IGNNE# if FERR# is true. If FERR# is false, then write to this port will not assert IGNNE#.			

IntrEdgeControl- RW – 16 bits - [IO_Reg: 4D0h]			
Field Name	**Bits**	**Default**	**Description**
IRQ0Control	0	0b	1: Level 0: Edge
IRQ1Control	1	0b	1: Level 0: Edge
Reserved	2	0b	
IRQ3Control	3	0b	1: Level 0: Edge
IRQ4Control	4	0b	1: Level 0: Edge
IRQ5Control	5	0b	1: Level 0: Edge
IRQ6Control	6	0b	1: Level 0: Edge
IRQ7Control	7	0b	1: Level 0: Edge
IRQ8Control	8	0b	(Read Only) Always Edge
IRQ9Control	9	0b	1: Level 0: Edge
IRQ10Control	10	0b	1: Level 0: Edge
IRQ11Control	11	0b	1: Level 0: Edge
IRQ12Control	12	0b	1: Level 0: Edge
Reserved	13	0b	
IRQ14Control	14	0b	1: Level 0: Edge
IRQ15Control	15	0b	1: Level 0: Edge
IntrEdgeControl register: This register programs each interrupt to be either edge or level sensitive.			

Pci_Intr_Index - RW – 8 bits - [IO_Reg: C00h]			
Field Name	**Bits**	**Default**	**Description**
Pci_Intr_Index	7:0	00h	PCI interrupt index –
Pci_Intr_Index register			

Pci_Intr_Data - RW – 8 bits - [IO_Reg: C01h]			
Field Name	**Bits**	**Default**	**Description**
Pci_Intr_Data	7:0	00h	PCI redirection register;
Pci_Intr_Data register			

Pci_Error - RW – 8 bits - [IO_Reg: C14h]			
Field Name	**Bits**	**Default**	**Description**
Serr_Nmi_Status	0	-	Set to 1 when NMI generation is enabled and SERR# has been asserted due to a PCI error. Cleared by writing a one to port 61h, bit 2. [Read-only]
Perr_Nmi_Status	1	-	Set to 1 when NMI generation is enabled and PERR# has been asserted due to a PCI data parity error. Cleared by writing a one to port 61h, bit 2. [Read-only]
Serr_Nmi	2	1b	Enable NMI generation from SERR# 0: Enable 1: Disable
Perr_Nmi	3	1b	Enable NMI generation from PERR# 0: Enable 1: Disable
Reserved	7:4	0h	
Pci_Error register			

PM2_Index - RW – 8 bits - [IO_Reg: CD0h]			
Field Name	**Bits**	**Default**	**Description**
PM2_Index	7:0	00h	Power management 2 index register. This register selects one of the Power Management 2 registers.
PM2_Index register			

PM2_Data - RW – 8 bits - [IO_Reg: CD1h]			
Field Name	**Bits**	**Default**	**Description**
PM2_Data	7:0	00h	Power management 2 data register. This register provides the read/write access to the indexed register.
PM2_Data register			

BIOSRAM_Index - RW – 8 bits - [IO_Reg: CD4h]			
Field Name	**Bits**	**Default**	**Description**
BiosRamIndex	7:0	00h	BIOS RAM index register. This register selects one of the 256 bytes of BIOS RAM. Data in this RAM is preserved until RSMRST# is asserted, or S5 power is lost.)
BiosRamIndex register			

BIOSRAM_Data - RW – 8 bits - [IO_Reg: CD5h]			
Field Name	**Bits**	**Default**	**Description**
BiosRamData	7:0	00h	Power management data register. This register provides the read/write access to the indexed register.
BiosRamData register			

PM_Index - RW – 8 bits - [IO_Reg: CD6h]			
Field Name	**Bits**	**Default**	**Description**
PM_Index	7:0	00h	Power management index register. This register selects one of the Power Management registers.

PM_Index register

PM_Data - RW – 8 bits - [IO_Reg: CD7h]			
Field Name	**Bits**	**Default**	**Description**
PM_Data	7:0	00h	Power management data register. This register provides the read/write access to the indexed register. (See ***???*** for more information.)
PM_Data register			

3.16 System Reset Register (IO CF9)

IO_Reg:CF9h is usually for generating system software resets. This register is defined to be a dual-port register, and can also be accessed through PM_IO Reg xC5, which is the CF9Shadow register.

3.17 Interrupt Routing Registers

Registers C00h and C01h will consolidate all interrupt mapping as follow:

Pci_Intr_Index - RW – 8 bits - [IO_Reg: C00h]			
Field Name	**Bits**	**Default**	**Description**
Pci_Intr_Index	6:0	00h	PCI interrupt index. Selects which PCI interrupt to map. 0h: INTA# 1h: INTB# 2h: INTC# 3h: INTD# 4h: INTE# 5h: INTF# 6h: INTG# 7h: INTH# 8h: Misc 9h: Misc0 Ah: Misc1 Bh: Misc2 Ch: INTA from serial irq Dh: INTB from serial irq Eh: INTC from serial irq Fh: INTD from serial irq 10h: SCI 11h: SMBUS0 12h: ASF 13h: HD audio 14h: FC 15h: GEC 16h: PerMon 20h: IMC INT0 21h: IMC INT1 22h: IMC INT2 23h: IMC INT3 24h: IMC INT4 25h: IMC INT5 30h: Dev18 (USB) IntA# 31h: Dev18 (USB) IntB# 32h: Dev19 (USB) IntA# 33h: Dev19 (USB) IntB# 34h: Dev22 (USB) IntA# 35h: Dev22 (USB) IntB# 36h: Dev20 (USB) IntC# 40h: IDE pci interrupt 41h: SATA PCI interrupt 50h: GPPInt0 51h: GPPInt1 52h: GPPInt2 53h: GPPInt3
Pci_Intr_Index	7	0b	0: select IRQ routing to PIC 1: select IRQ routing to IoApic

Pci_Intr_Data - RW – 8 bits - [IO_Reg: C01h]			
Field Name	**Bits**	**Default**	**Description**
Pci_Intr_Data	7:0	00h	For index other than Misc, Misc0, Misc1, Misc2, the register specifies the IRQ number in PIC mode if Pci_Intr_Index bit7 is set or INT number in IOAPIC if Pci_Intr_Index bit7 is set. In the case, only bit[4:0] is valid. Definition for Misc (default 00h): Bit 0: 0: 8254 timer as IRQ0 input source 1: Serial IRQ or PCI devices as IRQ0 input source Bit1: 0: IMC as IRQ1 input source 1: Serial Irq or PCI devices as IRQ1 input source Bit2: 0: Rtc is IRQ8 input source 1: Serial Irq or PCI devices as IRQ8 input source Bit3: 0: IMC as IRQ12 input source 1: Serial Irq or PCI devices as IRQ12 input source Bit[5:4]: 00: IRQ14 come from legacy IDE 01: IRQ14 come from SATA IDE 10: IRQ14 come from SATA2 11: IRQ14 come from SerIrq/Pci interrupt Bit[7:6]: 00: IRQ15 come from legacy IDE 01: IRQ15 come from SATA IDE 10: IRQ15 come from SATA2 11: IRQ15 come from SerIrq/Pci interrupt

Pci_Intr_Data - RW – 8 bits - [IO_Reg: C01h]			
Field Name	**Bits**	**Default**	**Description**
			Definition for Misc0 (default E7h): Bit0: 0: INT0 in IOAPIC comes from IRQ0 in PIC , INT2 in IOAPIC comes from INTR in PIC. 1: INT2 in IOAPIC comes from IRQ0 in PIC , INT0 in IOAPIC comes from INTR in PIC. Bit 1 (Merge_Ec_irq1): 0: Route serial IRQ1 to USB IRQ1 input 1: Route IMC IRQ1 to USB IRQ1 input Bit 2 (Merge_Ec_irq12): 0: Route serial IRQ12 to USB IRQ12 input 1: Route IMC IRQ12 to USB IRQ12 input Bit 3: MaskIrq1Irq12 0: turn on IRQ1 and IRQ12 1: Mask off IRQ1 and IRQ12 Bit 4: IrqInputEn 0: Mask off Irq input 1: Enable Irq input Bit 5: IRQ1 filter enable Bit 6: IRQ12 filter enable Bit7: INTR 600ns delay Misc2 and Misc1 define the capability bit in HPET capability register[15:0].

3.18 IO(x)APIC Registers

IO(x)APIC registers are defined as Memory/IO-mapped register space, the base address of which is defined through PM_Reg x34h.

3.18.1 Direct Access Registers

Note: The XAPIC_BASE_REGISTER has a power-on default value of FEC0_0000h.

IO Register Select Register - RW - [XAPIC_BASE_REGISTER + 00H]			
Field Name	**Bits**	**Default**	**Description**
Indirect Address Offset	7:0	00h	Indirect Address Offset to IO Window Register
Reserved	31:8		
Used to determine which register is manipulated during an IO Window Register read/write operation.			

IO Window Register - RW - [XAPIC_BASE_REGISTER + 10H]			
Field Name	**Bits**	**Default**	**Description**
IO Window	31:0	0h	Mapped by the value in the IO Register Select Register to the designated indirect access register. Technically a R/W register; however, the read/write capability is determined by the indirect access register referenced by the IO Register Select Register.

IRQ Pin Assertion Register - RW - [XAPIC_BASE_REGISTER + 20H]			
Field Name	**Bits**	**Default**	**Description**
Input IRQ	7:0	00h	IRQ number for the requested interrupt
Reserved	31:8	0000000h	
A write to this register will trigger an interrupt associated with the redirection table entry referenced by the IRQ number. Currently the redirection table has 24 entries. Write with IRQ number greater than 17H has no effect.			

EOI Register - W - [XAPIC_BASE_REGISTER + 40H]			
Field Name	**Bits**	**Default**	**Description**
Vector	7:0	00h	Interrupt vector
Reserved	31:8	0000000h	
A write to this register will clear the remote IRR bit in the redirection table entry found matching the interrupt vector. This provides an alternate mechanism other than PCI special cycle for EOI to reach IOXAPIC.			

3.18.2Indirect Access Registers

Software needs to first select the register to access using the IO Register Select Register, and then read or write using the IO Window Register.

IOAPIC ID Register - RW -[Indirect Address Offset = 00H]			
Field Name	**Bits**	**Default**	**Description**
Reserved	23:0	000000h	
ID	27:24	0h	IOAPIC device ID for APIC serial bus delivery mode
Reserved	31:28	0h	
Not used in XAPIC PCI bus delivery mode.			

IOXAPIC Version Register -R -[Indirect Address Offset = 01H]			
Field Name	**Bits**	**Default**	**Description**
Version	7:0	21h	PCI 2.2 compliant
Reserved	14:8	00h	
PRQ	15	1b	IRQ pin assertion supported
Max Redirection Entries	23:16	17h	24 entries [23:0]
Reserved	31:24	00h	

IOAPIC Arbitration Register -R - [Indirect Address Offset = 02H]			
Field Name	**Bits**	**Default**	**Description**
Reserved	23:0	000000h	
Arbitration ID	27:24	0h	Arbitration ID for APIC serial bus delivery mode
Reserved	31:28	0h	
Not used in XAPIC PCI bus delivery mode.			

Redirection Table Entry [0–23] - RW - [Indirect Address Offset = 11/10H–3F/3EH]			
Field Name	**Bits**	**Default**	**Description**
Vector	7:0	00h	Interrupt vector associated with this interrupt input
Delivery Mode	10:8	0h	000: Fixed 001: Lowest Priority 010: SMI/PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
Destination Mode	11	0b	0: Physical 1: Logical
Delivery Status	12	0b	Read Only 0: Idle 1: Send Pending
Interrupt Pin Polarity	13	0b	0: High 1: Low
Remote IRR	14	0b	Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
Trigger Mode	15	0b	0: Edge 1: Level
Mask	16	1b	Masks the interrupt injection at the input of this device. Write 0 to unmask
Reserved	31:17	0000h	
Reserved	55:32	000000h	
Destination ID	63:56	0	Bits [19:12] of the address field of the interrupt message

Chapter 4
LPC-ISA and PCI Bridges

To go to the section of interest, click on the following links:

4.1 LPC ISA Bridge (Device 20, Function 3)

4.1.1 PCI Configuration Registers

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID/Class Code	08h
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
BIST	0Fh
Base Address Reg 0	10h
Subsystem ID & Subsystem Vendor ID	2Ch
Capabilities Pointer	34h
PCI Control	40h
IO Port Decode Enable Register	44h
IO/Mem Port Decode Enable Register	48h
Memory Range Register	4Ch
Rom Protect 0	50h
Rom Protect 1	54h
Rom Protect 2	58h
Rom Protect 3	5Ch
PCI Memory Start Address for LPC Target Cycles	60h
PCI Memory End Address for LPC Target Cycles	62h
PCI IO base Address for Wide Generic Port	64h
LPC ROM Address Range 1 (Start Address)	68h
LPC ROM Address Range 1 (End Address)	6Ah
LPC ROM Address Range 2 (Start Address)	6Ch
LPC ROM Address Range 2 (End Address)	6Eh
Reserved	70h
Alternative Wide Io Range Enable	74h
Reserved	78h
TPM	7Ch
LPCCLKCntl	7Dh
Reserved	80h
TMKBC_BaseAddrLow	84h
TMKBC_BaseAddrHigh	88h
TMKBC_Remap	8Ch
Wide_IO2	90h
Gec_ShadowRom_Address	9Ch
Spi_Base	A0h
Imc_PortAddress	A4h
ROM_DMA_src_address	B0h
ROM_DMA_dst_address	B4h
RomDmaControl	B8h
ImcControl	BAh
HostControl	BBh
ImcRomWrOffset	C0
ImcRomRdOffset	C4
ClientRomProtect	C8
AutoRomCfg	CC
ClkGateCntrl	D0

PCI Function 3 configuration registers are described below.

Vendor ID- R - 16 bits - [PCI_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Vendor Identifier. The vendor ID is 0x1022.

Device ID- R - 16 bits - [PCI_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	780Eh	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.

Command- RW - 16 bits - [PCI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
IO Space	0	1b	I/O Access Enable. This bit controls access to the I/O space registers. When this bit is 1, it enables access to the legacy IDE ports, and PCI bus master IDE I/O registers are enabled.
Memory Space	1	1b	Memory Access Enable. This function is not implemented. This bit is always 1.
Bus Master	2	1b	Bus Master Enable. 1: Enable 0: Disable.
Special Cycles	3	1b	Special Cycle Recognition Enable. This feature is not implemented and this bit is always 1.
Memory Write and Invalidate Enable	4	0b	Memory Write and Invalidate Enable. Not implemented. This bit is always 0.
VGA Palette Snoop	5	0b	VGA Palette Snoop Enable. The FCH does not need to snoop VGA palette cycles. This bit is always 0.
Parity Error Response	6	0b	PERR# (Response) Detection Enable bit. If set to 1, The FCH asserts PERR# when it is the agent receiving data AND it detects a parity error. PERR# is not asserted if this bit is 0.
Stepping Control	7	0b	Wait Cycle Enable. The FCH does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
SERR# Enable	8	0b	SERR# Enable. If set to 1, the FCH asserts SERR# when it detects an address parity error. SERR# is not asserted if this bit is 0.
Fast Back-to-Back Enable	9	0b	Fast Back-to-back Enable. The FCH only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
Reserved	15:10	00h	

Command Register: The PCI specification defines this register to control a PCI device's ability to generate and respond to PCI cycles. Writes to this register, except bit 6, have no effect. Bits[3:0]=0fh and are read-only.

STATUS- RW - 16 bits - [PCI_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	
Capabilities List	4	0b	Read-only. When reg0x78[1] (Msi On) is 1, this bit reads 1; when reg0x78[1] (Msi On) is 0, this bit reads 0.
Reserved	7:5	0h	
Master Data Parity Error	8	0h	Data Parity Reported. Set to 1 if the FCH detects PERR# asserted while acting as PCI master (whether PERR# was driven by the FCH or not.)
Device Select Timing	10:9	1h	DEVSEL# Timing. Read-only. Indicates DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
Signaled Target Abort	11	0b	Signaled Target Abort. Set to 1 when the FCH signals Target Abort.
Received Target Abort	12	0b	Received Target Abort. Set to 1 when an FCH generated PCI cycle (the FCH is the PCI master) is aborted by a PCI target. Cleared by writing a 1 to it.
Received Master Abort	13	0b	Received Master Abort Status. Set to 1 when the FCH acts as a PCI master and aborts a PCI bus memory cycle. Cleared by writing a 1 to this bit.
Signaled System Error	14	0b	SERR# status. This bit is set to 1 when the FCH detects a PCI address parity error.
Detected Parity Error	15	0b	Detected Parity Error. This bit is set to 1 when the FCH detects a parity error.

Status Register: The PCI specification defines this register to record status information for PCI related events. This is a read/write register. However, writes can only reset bits. A bit is reset when the register is written and the data in the corresponding bit location is a 1.

Revision ID/Class Code - R - 32 bits - [PCI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	11h	These bits are hardwired to 11h to indicate the revision level of the chip design.
Class Code	31:8	060100h	Class Code.

Revision ID/Class Code Register: This read only register contains the device's revision information and generic function. Since FCH is an ISA bridge, its assigned class code is 060100h.

Cache Line Size - R - 8 bits - [PCI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	Cache Line Size.

Cache Line Size Register: This register specifies the system cache line size. This register is not implemented.

Latency Timer - R - 8 bits - [PCI_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Latency Timer	7:0	00h	Latency Timer.

Latency Timer Register: This register specifies the value of the Latency Timer in units of PCICLKs.

Header Type - R - 8 bits - [PCI_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	80h	Header Type.

Header Type Register: This register identifies the type of the predefined header in the configuration space. Since THE FCH is a multifunction device, the most significant bit is set.

BIST- R - 8 bits - [PCI_Reg: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
BIST	7:0	00h	BIST.

Built-in Self Test Register: This register is used for control and status for Built-in Self Test. LPC has no BIST modes.

Base Address Reg 0 - RW* - 32 bits - [PCI_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 0	31:0	FEC0_0000h	Base address register 0.

* This register is write-only. Reading it always returns 0000_0000h. It has an internal value used as base address for APIC memory space. Writing to the register will change its internal value, but only bits[31:5] are overwritten, and bits[4:0] are hardwired to 00000b. The default internal value is FEC0_0000h.

Subsystem ID & Subsystem Vendor ID - W/R* - 32 bits - [PCI_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	1022h	Subsystem Vendor ID.
Subsystem ID	31:16	780Eh	Subsystem ID.

* This 4-byte register is a write-once & read-only afterward register. The BIOS writes this register once (all 4 bytes at once) and software reads its value (when needed).

Capabilities Pointer - R - 32 bits - [PCI_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	00h	When reg0x78[1] (Msi On) is 0, this field reads 0; when reg0x78[1] is 1, this field reads 80h, pointing to the starting address of the MSI Capability register.
Reserved	31:8	000000h	

PCI Control - RW - 8 bits - [PCI_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0h	
Legacy DMA Enable	2	1b	Setting it to 1 enables LPC DMA cycle. Note: 32-bit DMA is not supported. Transfer size: Channels 0-3: 8 bits, channels 5-7: 16 bits.
Reserved	4:3	0h	
BiosSemaphore	5	0b	This bit is writeable by BIOS and read by the IMC. This is used as the software semaphore mechanism between BIOS and IMC to see who can access the common resource. BIOS should read bit[6] first to see if IMC has taken ownership of the resource first. If bit[6] is 0, then BIOS should write a 1 to this bit and then follow by a read to see if this bit is set. If this bit is set, it means BIOS has successfully taken ownership of the resource. If this bit returns 0 and bit[6] returns a 1, then IMC has taken ownership first. Software should always clear this bit after it has completed its access to the resource.
IMCSemaphore	6	0b	This bit is writeable by the IMC and read by BIOS. This is used as the software semaphore mechanism between BIOS and IMC to see who can access the common resource. IMC should read bit[5] first to see if BIOS has taken ownership of the resource first. If bit[5] is 0, then IMC should write a 1 to this bit and then follow by a read to see if this bit is set. If this bit is set, it means IMC has successfully taken ownership of the resource. If this bit returns a 0 and bit[5] returns a 1, then BIOS has taken ownership first. IMC should always clear this bit after it has completed its access to the resource.
IMCPresent	7	0b	This is a SW bit, which can be programmed by IMC only to indicate to the host that IMC is present.

IO Port Decode Enable - RW - 32 bits - [PCI_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
Parallel Port Enable 0	0	0b	Port enable for parallel port, 378-37fh
Parallel Port Enable 1	1	0b	Port enable for parallel port, 778-77fh
Parallel Port Enable 2	2	0b	Port enable for parallel port, 278-27fh
Parallel Port Enable 3	3	0b	Port enable for parallel port, 678-67fh
Parallel Port Enable 4	4	0b	Port enable for parallel port, 3bc-3bfh
Parallel Port Enable 5	5	0b	Port enable for parallel port, 7bc-7bfh
Serial Port Enable 0	6	0b	Port enable for serial port, 3f8-3ffh
Serial Port Enable 1	7	0b	Port enable for serial port, 2f8-2ffh
Serial Port Enable 2	8	0b	Port enable for serial port, 220-227h
Serial Port Enable 3	9	0b	Port enable for serial port, 228-22fh
Serial Port Enable 4	10	0b	Port enable for serial port, 238-23fh
Serial Port Enable 5	11	0b	Port enable for serial port, 2e8-2efh
Serial Port Enable 6	12	0b	Port enable for serial port, 338-33fh
Serial Port Enable 7	13	0b	Port enable for serial port, 3e8-3efh
Audio Port Enable 0	14	0b	Port enable for audio port, 230-233h (range 220-22fh needs to be enabled using bits 0 and 1)
Audio Port Enable 1	15	0b	Port enable for audio port, 240-253h
Audio Port Enable 2	16	0b	Port enable for audio port, 260-273h
Audio Port Enable 3	17	0b	Port enable for audio port, 280-293h
MIDI Port Enable 0	18	0b	Port enable for MIDI port, 300-301h
MIDI Port Enable 1	19	0b	Port enable for MIDI port, 310-311h
MIDI Port Enable 2	20	0b	Port enable for MIDI port, 320-321h
MIDI Port Enable 3	21	0b	Port enable for MIDI port, 330-331h
MSS Port Enable 0	22	0b	Port enable for MSS port, 530-537h
MSS Port Enable 1	23	0b	Port enable for MSS port, 604-60bh
MSS Port Enable 2	24	0b	Port enable for MSS port, e80-e87h

IO Port Decode Enable - RW - 32 bits - [PCI_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
MSS Port Enable 3	25	0b	Port enable for MSS port, f40-f47h
FDC Port Enable 0	26	0b	Port enable for FDC port, 3f0-3f7h
FDC Port Enable 1	27	0b	Port enable for FDC port, 370-377h
Game Port Enable	28	0b	Port enable for Game port, 200-20fh
KBC Port Enable	29	0b	Port enable for KBC port, 60 & 64h
ACPI Micro-Controller Port Enable	30	0b	Port enable for ACPI Micro-Controller port, 62 & 66h
Ad-Lib Port Enable	31	0b	Port enable for Ad-Lib port, 388-389h

This register controls the decoding of parallel, serial, audio, MID, and MSS, FDC, game, KBC, ACPI micro-controller, & Ad-lib ports. Writing 1 to a bit enables the corresponding I/O range.

IO/Mem Port Decode Enable - RW - 32 bits - [PCI_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
Super IO Configuration Port Enable	0	0b	Port enable for Super I/O Config Port, 2e-2fh
Alternate Super IO Configuration Port Enable	1	0b	Port enable for Alternate Super I/O Config Port, 4e-4fh
Wide Generic IO Port Enable	2	0b	Port enable for Wide Generic Port, see registers 64h-65h
Rom Range 1 Port Enable	3	0b	Port enable for LPC ROM address range 1 (memory), see registers 68h-6Bh
Rom Range 2 Port Enable	4	0b	Port enable for LPC ROM address range 2 (memory), see registers 6Ch-6Fh
Memory Range Port Enable	5	0b	Port enable for LPC memory target range, see registers 60h-63h
RTC IO Range Port Enable	6	0b	Port enable for RTC I/O range 70h~73h
Sync Timeout Counter Enable	7	0b	LPC sync timeout counter enabled when set to 1; otherwise the counter is disabled. This counter is used to avoid a deadlock condition if an LPC device drives sync forever. Timeout count is programmed in register0x49h. Write 0 to this bit if an LPC device is extremely slow & takes more than 255 LPC clocks to complete a cycle.
Sync Timeout Count	15:8	FFh	Sync Timeout Count. This is the number of LPC clocks that the state machine will wait when LPC data = sync before aborting the cycle (when Sync Timeout Counter Enable is set)
IO port enable 0	16	0b	Port enable for IO port 400h-43Fh
IO port enable 1	17	0b	Port enable for IO port 480h-4BFh
IO port enable 2	18	0b	Port enable for IO port 500h-53Fh
IO port enable 3	19	0b	Port enable for IO port 580h-5BFh
Mem port enable	20	0b	Port enable for 4K byte memory range defined in reg0x4C
IO port enable 4	21	0b	Port enable for IO port 80h
IO port enable 5	22	0b	Port enable for IO port 4700h-470Bh
IO port enable 6	23	0b	Port enable for IO port FD60h-FD6Fh
Wide_io1_enable	24	0b	Wide IO port 1 (defined in registers 66/67h) enable
Wide_io2_enable	25	0b	Wide IO port 2 (defined in registers 90/91h) enable
Reserved	31:26	0b	

This register controls the decoding of Super I/O configuration, alternate Super I/O configuration, wide generic ports, ROM1 & ROM2 ports, and memory port. Writing a 1 to a bit enables the corresponding IO/ROM/Memory range.

Memory Range - RW - 32 bits - [PCI_Reg: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	11:0	0	
Base Address	31:12	0	This register defines a 4K byte memory range from {Base Address, 000h} to {Base Address, FFFh}. The range is enabled by reg0x4A[4] (Mem port enable).

Rom Protect 0 - RW - 32 bits - [PCI_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
Write Protect	0	0b	When this bit is set, the memory range defined by this register is write-protected. Writing to the range has no effect.
Read Protect	1	0b	When this bit is set, the memory range defined by this register is read-protected. Reading any location in the range returns FFFF_FFFFh.
Rom Offset	10:2	000h	Rom range offset
Rom Base	31:11	000000h	Rom Base and Rom Offset together define the ROM range to be protected. The range is: From {Rom Base, 000_0000_0000b} to {Rom Base, 000_0000_0000b} + {0_0000_0000_0000b, Rom Offset, 11_1111_1111b}

For Host, this register is write/read, but it can only be written once after hardware reset. Subsequent writes to it have no effect. For IMC, this register is always write/read

Rom Protect 1 - RW - 32 bits - [PCI_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
This register has exactly the same definition as that of Rom Protect 0 except it is for another range.			

Rom Protect 2 - RW - 32 bits - [PCI_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
This register has exactly the same definition as that of Rom Protect 0 except it is for another range.			

Rom Protect 3 - RW - 32 bits - [PCI_Reg: 5Ch]			
Field Name	**Bits**	**Default**	**Description**
This register has exactly the same definition as that of Rom Protect 0 except it is for another range.			

PCI Memory Start Address for LPC Target Cycles - RW - 16 bits - [PCI_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
Memory Start Address	15:0	0000h	16-bit starting address of the LPC target (memory) range.

This register contains the upper 16 bits of the starting address of the LPC memory target range. The lower 16 bits of the starting address are considered 0's. This range can be enabled/disabled using reg0x48[5] (Memory Range Port Enable).

PCI Memory End Address for LPC Target Cycles - RW - 16 bits - [PCI_Reg: 62h]			
Field Name	**Bits**	**Default**	**Description**
Memory End Address	15:0	0000h	16-bit END address of the LPC target (memory) range.

This register contains the upper 16 bits of the ending address of the LPC memory target range. The lower 16 bits of the end address are considered 1's. This range can be enabled/disabled using reg0x48[5] (Memory Range Port Enable).

PCI IO base Address for Wide Generic Port - RW - 32 bits - [PCI_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
IO Base Address 0	15:0	0000h	16-bit PCI I/O base address for wide generic port range. 16/512byte wide range. This function is enabled by reg0x48[2] (Wide Generic IO Port Enable). When Alternative Wide Io Range Enable (0x74[0]) is set to 1, the range is 16 bytes; otherwise, the range is 512 bytes
IO Base Address 1	31:16	0000h	16-bit PCI I/O base address for wide generic port range. 512byte wide range. This function is enabled by reg0x4B[0] (0x48[24]) (Super IO Configuration Port Enable). When Alternative Wide Io Range Enable (0x74[2]) is set to 1, the range is 16 bytes; otherwise, the range is 512 bytes

This register contains two 16-bits of I/O base address for LPC I/O (wide generic port) target range. The limit address is found by adding 512 to the base address.

Note: The registers PCI_Reg: 68h – 6Eh below are used for both LPC and SPI flash.

ROM Address Range 1 (Start Address) - RW - 16 bits - [PCI_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
Rom Start Address 1	15:0	08h 00h (if the strap is disabled)	16-bit starting address of the ROM (memory) address range 1. Default is set to 512K below 1M.

This register contains the upper 16 bits of the starting address of the ROM address range 1. The lower 16 bits of the starting address are considered 0's. This range can be enabled/disabled using reg0x48[3] (Rom Range 1 Port Enable)

ROM Address Range 1 (End Address) - RW - 16 bits - [PCI_Reg: 6Ah]			
Field Name	**Bits**	**Default**	**Description**
Rom End Address 1	15:0	0fh, 00h (if the strap is disabled)	16-bit END address of the ROM (memory) address range 1.

This register contains the upper 16 bits of the ending address of the ROM address range 1. The lower 16 bits of the end address are considered 1's. This range can be enabled/disabled using reg0x48[3] (Rom Range 1 Port Enable)

ROM Address Range 2 (Start Address)- RW - 16 bits - [PCI_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
Rom Start Address 2	15:0	FFF8h, 00h (if the strap is disabled)	16-bit starting address of the ROM (memory) address range 2. Default is set to 512K below 4GB

This register contains the upper 16 bits of the starting address of the ROM address range 2. The lower 16 bits of the starting address are considered 0's. This range can be enabled/disabled using reg0x48[4] (Rom Range 2 Port Enable)

ROM Address Range 2 (End Address) - RW - 16 bits - [PCI_Reg: 6Eh]			
Field Name	**Bits**	**Default**	**Description**
Rom End Address 2	15:0	FFFFh, 00h (if the strap is disabled)	16-bit END address of the ROM (memory) address range 2.

This register contains the upper 16 bits of the ending address of the ROM address range 2. The lower 16 bits of the end address are considered 1's. This range can be enabled/disabled using reg0x48[4] (Rom Range 2 Port Enable)

Alternative Wide IO Range Enable - WR - 32 bits - [PCI_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
Alternative Wide Io Range Enable	0	0b	Wide I/O range is usually 512 bytes. With this bit set, the range changes to 16 bytes only. To use this feature, address in reg0x64~65 must be aligned to 16 bytes, i.e., bits[3:0] must be 0. If the address is not aligned to 16 bytes, the I/O range is from address[15:0] to {address[15:4], 0xF}.
Reserved	1	0b	
Alternative Wide Io 1 Range Enable	2	0b	Similar to bit[0], but it applies to I/O address defined in reg0x66~67.
Alternative Wide Io 2 Range Enable	3	0b	Similar to bit[0], but it applies to I/O address defined in reg0x90~91.
Reserved	7:4	00h	

Miscellaneous Control Bits - WR - 8 bits - [PCI_Reg: 78h]			
Field Name	**Bits**	**Default**	**Description**
No Hog	0	1b	1:when enabled, the internal bus will not be locked by LPC bridge during a slave access (eg. LPC DMA fetch). 0: If not set, LPC may hold the internal bus during a DMA transfer.
Msi On	1	0b	1: Turn on LPC MSI Capability. The following will be true: * Reg0x06[4] (Capabilities List) reads 1. * Reg0x34[7:0] (Capabilities Pointer) reads 80h 0: Turn off LPC MSI Capability. The following will be true: * Reg0x06[4] (Capabilities List) reads 0. * Reg0x34[7:0] (Capabilities Pointer) reads 0.
LDRQ0	2	0b	Enable LDRQ0# on LPC bus if set to 1
LDRQ1	3	0b	Enable LDRQ1# on LPC bus if set to 1
SMMWriteRomEn	4	1b	Enable Rom access in SMM mode
GateSpiAccessDis	5	0	Set to 1 to pass rom access to spi even it is strapped as lpc
GateWrongRx	6	0	Set to 1 to allow AltrxByteCount to be 0
AllowHostInDma	7	1	1: allow Host to access Lpc if acpi has not give gnt to lpc during dma transfer. 0: Dma hold LPc even acpi has not give gnt to lpc during dma transfer.
Msi Hidden	8	0	1: Host can change the value of PCI_Reg 80h 0: Host can not change the value of PCI_Reg 80h
Reserved	31:9	00000_000h	

TPM (trusted platform module) - WR - 8 bits - [PCI_Reg: 7Ch]			
Field Name	**Bits**	**Default**	**Description**
Tpm12_en	0	0b	When set to 1, it enables decoding of tpm (trusted platform module) cycles defined in TPM1.2 spec (refer to the addresses defined in bit[1] below). Note that tpm12_en and tpm_legacy are independent bits; they respectively turn on decoding of different tpm addresses.
Tpm_amd	1	0b	This bit is replaced with strap pin and no longer in use. It is read-only and returns 0. When the strap is 0, it ONLY supports these normal tpm cycles. Below are the cycle definitions (left-hand-side is system/software memory address, which is translated to LPC I/O address on the right hand side.) 0xFED4_0xxx --> 0x0xxx 0xFED4_1xxx --> 0x1xxx 0xFED4_2xxx --> 0x2xxx 0xFED4_3xxx --> 0x3xxx 0xFED4_4xxx --> 0x4xxx When the strap is 1, it ONLY supports these AMD tpm cycles. 0xFED4_0xxx --> 0x0xxx 0xFED4_1xxx --> 0x1xxx 0xFED4_2xxx --> 0x2xxx 0xFED4_3xxx --> 0x3xxx 0xFD_F920_0000~0xFD_F923_FFFF --> 0x4028 0xFD_F928_0000~0xFD_F928_0003 --> 0x4020 0xFD_F928_0004~0xFD_F928_0007 --> 0x4024~0x4027
Tpm_legacy	2	0b	When set to 1, it enables decoding of legacy tpm addresses, i.e., I/O addresses 7E/7F and EE/EF will be decoded.
Tmkbc_enable	3	0b	Enable bit for the TMKBC function
Tmkbc_set	4	0b	Write once bit. Once set, all tmkbc address/remap registers cannot be changed until the next reset.
Tmkbc_sel	6:5	0b	Select which one of the four sets of tmkbc registers (specified in the registers 84h, 88h, and 8Ch) to be accessed.
WiderTpmEn	7	0b	Set to 1 to force logic to decode FED4xxxx as TPM cycles instead of FED4_0xxx, FED4_1xxx, FED4_2xxx, FED4_3xxx, and FED4_4xxx.

Note: any tpm cycle above is decoded only when the cycle is started by ALinkBridge. Access from bus master devices is not allowed.

LPCCLKCntl - RW - 8 bits - [PCI_Reg: 7Dh]			
Field Name	**Bits**	**Default**	**Description**
GpioLpcClk1	0		Read only. Status of LpcClk1 port
GpioLpcClk1OeB	1	1b	R/W. 1: disable GpioLpcClk1 output 0: enable GpioLpcClk1 output
GpioLpcClk1Out	2	0b	R/W, control GpioLpcClk1 output value
LpcClk1IsGpio	3	1b	R/W. 1: Treat LpcClk1IsGpio as GPIO 0: Treat LpcClk1IsGpio as LpcClk1
Reserved	7:4	0000b	

Reserved – R – 32 bits – [PCI_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

TMKBC_BaseAddrLow - RW - 32 bits - [PCI_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	
Addr64	2	0b	Defines whether the address is 32 or 64 bits. 1: The address is 64 bits; 0: The address is 32 bits.
MaskBits10thru8	3	0b	Defines whether address bits[10:8] are masked ("masked" means bits[10:8] are don't care). 1: Masked 0: No mask
MaskBits11thru8	4	0b	Defines whether address bits [11:8] are masked. 1: Masked 0: No mask
MaskBits12thru8	5	0b	Defines whether address bits [12:8] are masked. 1: Masked 0: No mask
MaskBits13thru8	6	0b	Defines whether address bits [13:8] are masked. 1: Masked 0: No mask
TMKBC_BaseAddrLow	31:7	000000h	This register defines the lower 32 bit memory address used for the TMKBC function. There are actually four sets of such mapping. The selection is controlled by reg0x7C[6:5] (Tmkbc_sel). 00: set 0 01: set 1 10: set 2 11: set 3

TMKBC_BaseAddrHigh - RW - 32 bits - [PCI_Reg: 88h]			
Field Name	**Bits**	**Default**	**Description**
TMKBC_BaseAddrHigh	31:0	00000000h	This register defines the upper 32 bit memory address used for the TMKBC function. This register has no meaning if bit 2 of 84h is set to 0. There are actually four sets of such mapping. The selection is controlled by reg0x7C[6:5] (Tmkbc_sel). 00: set 0 01: set 1 10: set 2 11: set 3

TMKBC_Remap - RW - 16 bits - [PCI_Reg: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
TMKBC_Remap	15:8	00h	This register defines the remap address [15:8] on the LPC bus. There are actually four sets of such mapping. The selection is controlled by reg0x7C[6:5] (Tmkbc_sel). 00: set 0 01: set 1 10: set 2 11: set 3
Reserved	7:0	0h	

Wide IO 2 - RW - 16 bits - [PCI_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
IO Base Address 2	15:0	0000h	16-bit PCI I/O base address for wide generic port range. 512 byte wide range. This function is enabled by reg0x4B[1] (Wide_io2_enable). When Alternative Wide Io 1 Range Enable (0x74[3]) is set to 1, the range is 16 bytes; otherwise, it is defined as 512 bytes

IMC_LPC_Cntrl - RW - 16 bits - [PCI_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:9	0h	
IMCHoldLpc	8	0b	When set, IMC will hold the LPC bridge (i.e., host cannot access LPC)
Reserved	7:1	0h	
HostHoldLpc	0	0b	When set, host will hold the LPC bridge (i.e., it will prevent IMC from accessing the LPC bridge)

Gec_ShadowRom_Address - RW - 16 bits - [PCI_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
Gec_ShadowRomAddr	31:10	00000h	This is the base address to the GEC shadow ROM (2K alignment)
Gec_portActive	0	-	Indicates whether shadowRom is active. 1: Active 0: Not active

SPI Base_Addr - RW - 16 bits - [PCI_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved.
SpiRomEnable	1	1b	When this bit is set and chip is strapped to SPI Rom, SPI Rom is enabled, otherwise SPI Rom is disabled.
Reserved	2	0b	Reserved.
RouteTPM2SPI	3	0b	When set, TPM cycles are routed to SPI bus with TPM_SPI_CS# asserted (note TCG has not finalized the SPI TPM specification yet)
Reserved	4	0b	Reserved
SPI_BaseAddr	31:5	0000000h	This register defines the base address for the SPI ROM controller.

IMC_PortAddress - RW - 16 bits - [PCI_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
IMC_PortActive	0	1b	When set to 1, LPC can decode the address specified in ec_PortAddress; otherwise, LPC ignores it.
IMC_Addr15_1	15:1	0017h	When Addr15_1 is non-zero, and if an I/O cycle from host has address[15:1] = Addr15_1, the cycle will be routed to IMC instead of to LPC bus. By default, address[15:0] = 002Eh or 002Fh will be routed. Read-only to host if reg0xBA[3] (ec_PortHostAccessEn) = 0.

RomDmaSrcAddr - RW - 16 bits - [PCI_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0	
DmaStartAddr	31:6	00000000h	This register defines the starting DMA address to read from the ROM. Note this is not the same as the legacy DMA function. This is meant to be used by BIOS to fetch BOOT codes quicker.

RomDmadstAddr - RW - 16 bits - [PCI_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	5:0	0	
DmaDstAddr	31:6	00000000h	This register defines the target DMA address to be written in the system memory. Note this is not the same as the legacy DMA function. This is meant to be used by BIOS to fetch BOOT codes quicker.

RomDmaControl - RW - 16 bits - [PCI_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
DmaStart	0	0b	Setting this bit will cause LPC bridge to start the DMA function, with starting addresses defined by reg0xB0 and reg0xB4. This bit will return the status of the DMA transfer. A return value of 0 means DMA transfer is completed. A return value of 1 means DMA transfer is running. Software can read this bit but writing to it has no effect.
DmaErrorStatus	1	0b	Read-only. 1: Previous transfer has error. 0: Previous transfer has completed successfully.
Reserved	5:2	0000h	.
DWCount	15:6	0000h	This register defines the number of cacheline (64 bytes) to be fetched from the ROM when DMA is used.

IMCControl - RW - 8 bits - [PCI_Reg: BAh]			
Field Name	**Bits**	**Default**	**Description**
IMC Page Protect	0	0b	Enable the protection of IMC page registers. 1: 0xregBC~C7 are only read/writeable by IMC. Host write to them has no effect. Host read from them returns 0. 0: 0xregBC~C7 are read/writeable by both IMC and Host. (note: registers C5h~C7h are reserved and not shown here)

IMCControl - RW - 8 bits - [PCI_Reg: BAh]			
Field Name	**Bits**	**Default**	**Description**
SpiHoldOnGevent9Dis	1	0b	0: GEVENT9 and ROM_RST# are configured to SPI_HOLD# and SPI_WP# function. 1: GEVENT9 and ROM_RST# are NOT configured to SPI_HOLD# and SPI_WP# function.
PrefetchEnSPIFromIMC	2	0b	Set to 1 to enable prefetch a cacheline (64 bytes) when IMC reads code from the SPI rom.
IMC_PortHostAccessEn	3	0b	Set to 1 to allow Host to program ec_PortAddress register
IMCReadOfSwitch	4	0b	1: Upper 16 bits of IMC read request address are specified in EcRomRdOf. 0: Upper 16 bits of IMC read request address are specified by auto rom diction logic.
PrefetchMissEn	5	1b	Set to1 to force the on-going prefetch to stop if the address of the pending read is not within the prefetch range for IMC.
PrefetchEnSel	6	1b	0: Prefetch only the address of the read request is on the 4 byte boundary. 1: Prefetch only the address of the read request is on the 8 byte boundary.
PrefetchEnSPIFromUSB	7	0b	This is for performance enhancement purpose. When set, SPI controller will prefetch from the flash on behalf of USB3 controller

HostControl- RW - 8 bits - [PCI_Reg: BBh]			
Field Name	**Bits**	**Default**	**Description**
PrefetchEnSPIFromHost	0	0b	This is for performance enhancement purpose. When set, the SPI controller will prefetch from the flash on behalf of the host.
DisableLADPullUp	1	0b	0: enable LAD pull-up when IMC or Gec is enabled, or the system is in S0. 1: Disable LAD pull-up
Sync_t_start	2	0b	Set the bit to 1 to delay one LPC cyle delay before passing host cycle to SPI/LPC bus. The bit has to be set to 1 when ClkRun# is enabled.
AbortCycleChkEn	3	0b	1: Abort condition is determined at the third clock after SYNC 0: Abort condition is determined at the second clock after SYNC SW should set the bit to 1 all the time.
Reserved	5:4	0h	
PrefetchMissEnHost	6	1b	Set to1 to force the on-going prefetch to stop if the address of the pending read is not within the prefetch range for the host.
PwnSpiBus	7	0b	Set this bit to 1 to force all the SPI signals (SpiCs#, SpiDin, SpiDout, SpiWp#, SpiHold#) to be driven to low in S3/S4/S5 if IMC is not enabled.

Note: This register is read/write by IMC and host.

IMCRomWrOffset - RW - 32 bits - [PCI_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
IMCRomWrOffset	31:0	FFF2_0000h	Specify address of the IMC write request.

When reg0xBA[0] (IMC Page Protect) = 1, this register will return the variables as described above. When reg0xBA[0] (IMC Page Protect) = 0, this register will return all 0s.

IMCRomWrOffset - RW - 32 bits - [PCI_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
IMCRomRdOffset	31:0	FFF2_0000h	Specify upper address of the IMC read request.

When reg0xBA[0] (IMC Page Protect) = 1, this register will return the variables as described above. When reg0xBA[0] (IMC Page Protect) = 0, this register will return all 0s.

ClientRomProtect - RW - 32 bits - [PCI_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
IMCRomPortectEn	0	0	When set, SW cannot access IMC portion of the flash.
GecRomProtectEn	1	0	When set, SW cannot access integration GMAC portion of the flash.
UsbRomProtectEn	2	0	When set, SW cannot access USB portion of the flash.
Reserved	7:3	00000	Spare bits.

AutoRomCfg - RW - 32 bits - [PCI_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
AutoAddressSelect	1:0	00b	The FCH will auto detect the location of IMC, GEC, and USB3 firmware locations. After detection, it will write the address pointers of each firmware onto bits[31:2]. Bits[1:0] of this register configure which address to be returned on bits[31:2]. 00: -- 01: IMC 10: GEC 11: USB xHCI
AutoRomAddr	31:2	--	Based on AutoAddressSelect, this register returns the address value detected by the auto-rom detection logic (EcCodeOffset, MacRomOffset, XhciRomOffset)
Bits 1:0 are R/W, bits 31:2 are read-only.			

ClkGateCntrl - R - 32 bits - [PCI_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
ClkGateCntrl	1:0	10b	These two bits control whether the LPC module will allow clock gating to the internal 66Mhz core clock. 00: Disable the clock gating function 01: Wait 16 clocks before allowing clock gating to the LPC module 10: Wait 64 clocks before allowing clock gating to the LPC module 11: Wait 256 clocks before allowing clock gating to the LPC module
ClkRunDisable	2	0b	When set, we will not allow CLKRUN# assertion by PCIBridge. In other words, the internal CLKRUN# coming from LPC will always be 0, which means PCIbridge can never stop the clock.

4.1.2 SPI ROM Controller Registers

Register Name	Offset Address
SPI_Cntrl0	00h
SPI_RestrictedCmd	04h
SPI_RestrictedCmd2	08h
SPI_Cntrl1 Register	0Ch
SPI_CmdValue0	10h
SPI_CmdValue1	14h
SPI_CmdValue2	18h
Reserved	1Ch
Alt_SPI_CS	1Dh
SpiIndexAddr Register	1Eh
SpiIndexData Register	1Fh

Software can communicate with the SPI ROM through the default memory or alternate program method.

Memory access to the BIOS ROM address space is automatically handled by the hardware. The SPI ROM controller will translate the memory address onto the SPI bus and access the SPI ROM data. Any other commands besides memory_read or memory_write to the SPI ROM will need to go through the alternate program method. In this method, software will need to program the OpCode, SpiAddress, TxByteCount, RxByteCount, put the data into the transmit FIFO, and then execute the command. The hardware will then communicate with the SPI ROM using these parameters. This alternate method basically allows software to issue any flash vendor specific commands such as ERASE and STATUS.

SPI_Cntrl0 - RW - 32 bits - [Spi_Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
SPI_OpCode	7:0	0	When software uses the alternate program method to communicate with the SPI ROM, this register contains the OPCODE.
TxByteCount	11:8	0	Number of bytes to be sent to SPI ROM.
RxByteCount	15:12	0	Number of bytes to be received from the SPI ROM.
ExecuteOpCode	16	0	Write 1 to execute the transaction in the alternate program registers. Writing 0 has no effect. When the transaction is complete, this bit will return 0. If the command is an illegal command, the bit cannot be set and thereby cannot execute.
Reserved	17	0	Reserved
SpiReadMode[0]	18	0	Bit 0 of SpiReadMode. Specifies the SPI read mode. Refer to the definition of SpiReadMode in bits [30:29] below.
SpiArbEnable	19	0	If a MAC is sharing the ROM with the FCH, both chips will need to go through an arbitration process before either one can access the ROM. This bit enables the arbitration. If MAC is not sharing the SPI ROM, BIOS should set this bit to 0 to speed up the SPI ROM access.
FifoPtrClr	20	0	Write Only. A write of 1 to this bit will clear the internal FIFO pointer.
IllegalAccess	21	0	Read Only. 0: Legal Index mode access 1: Illegal Index mode access
SpiAccessMacRomEn	22	1	This is a clear-once protection bit; once set, software cannot access MAC's portion of the ROM space (lower 512KB). However, IMC can always read/write this bit.
SpiHostAccessRomEn	23	1	This is a clear-once protection bit; once set, MAC cannot access BIOS ROM space (upper 512KB). However, IMC can always read/write this bit.
ArbWaitCount	26:24	000	Under ROM sharing mode (with the MAC), this defines the amount of wait time this controller will assert HOLD# before it should access the SPI ROM. This time is to allow the MAC to sample HOLD#.

SPI_Cntrl0 - RW - 32 bits - [Spi_Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
SpiBridgeDisable	27	1	Setting this bit will disable the SPI bridge mode (FCH will act as a SPI-LPC bridge to the MAC).
SPIClkGate	28	0	Set to 1 to force the 7th spiclk to be removed when reading the last data.
SpiReadMode[2:1]	30:29	000	These two bits and bit 18 in the same register specify the Spi read mode: 000: Normal read (16.7MHz) 001: Reserved 010: Dual-io (1-1-2) (up to 66MHz, specified by fast speed register) 011: Quad-io (1-1-4) (up to 66MHz, specified by fast speed register) 100: Dual-io (1-2-2) (up to 66MHz, specified by fast speed register) 101: Quad-io (1-4-4) (up to 66MHz, specified by fast speed register) 110: Normal read (up to 66MHz, specified by normal speed register) Note: The pull-up and pull-down of SpiHold# and SpiWp# pads must be disabled by programming Gpio_reg 0x69 and Gpio_reg 0xA1 if Quad-io mode is enabled.
SpiBusy	31	0	Read-only. 0: SPI bus is idle 1: SPI bus is busy

SPI_RestrictedCmd - RW - 32 bits - [Spi_Mem_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
RestrictedCmd0	7:0	0	This defines a restricted command issued by the MAC which will be checked by the FCH. If the opcode issued by the MAC matches with this register and the address space is in the BIOS space, this controller will simply ignore the command for the case of bridge mode. For peer mode, the SPI controller will jam the entire interface as an attempt to stop that transaction. Note when either SpiAccessMacRomEn and/or SpiHostAccessRomEn bit are cleared, these registers become read-only and cannot be changed any more.
RestrictedCmd1	15:8	0	Same as RestrictedCmd0
RestrictedCmd2	23:16	0	Same as RestrictedCmd0
RestrictedCmd3	31:24	0	Same as RestrictedCmd0

SPI_RestrictedCmd2 - RW - 32 bits - [Spi_Mem_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
RestrictedCmd4	7:0	0	Same as RestrictedCmd0
RestrictedCmdWoAddr0	15:8	0	Same as RestrictedCmd0 except this command does not have address
RestrictedCmdWoAddr1	23:16	0	Same as RestrictedCmd0 except this command does not have address
RestrictedCmdWoAddr2	31:24	0	Same as RestrictedCmd0 except this command does not have address

SPI_Cntrl1 - RW - 32 bits - [Spi_Mem_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
SPIParameters	7:0	0	This is the TX/RX FIFO port which can take up to 8 bytes. To send data to SPI ROM, software writes data into this port. To retrieve data that are received from the SPI ROM, software reads from this port.
FifoPtr	10:8	000	This three bits show the internal pointer location.
TrackMacLockEn	11	0	When set, the controller will lock the SPI for the MAC when it has detected a command (from the MAC) matching the value defined in offset 10h or 11h. Conversely, it will unlock the bus when it has detected a command (from the MAC) matching the value defined in offset 12h or 13h.
NormSpeed	13:12	11	This defines the clock speed for the non-fast read command 00 – 66MHz 01 – 33MHz 10 – 22 MHz 11 – 16.5MHz
FastSpeed	15:14	01	This defines the clock speed for the fast read command 00 - 66MHz 01 - 33MHz 10 - 22 MHz 11 - 16.5MHz
WaitCount	21:16	00000	Specify the time unit (15ns * WaitCount): 0000: 15ns 0001: 2:15ns
ByteCommand	31:24	0	Specify the command byte for the Op code transaction.
Note: When either SpiAccessMacRomEn and/or SpiHostAccessRomEn of offset 00h are cleared, the fields RestrictedCmdWoAddr1 and RestrictedCmdWoAddr2 become read-only and cannot be changed any more.			

SPI_CmdValue0 - RW - 32 bits - [Spi_Mem_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
MacLockCmd0	7:0	06h	This is used to compare against the opcode sent out by the MAC. If SPI_Cntrl1[11] is set, the controller will lock the SPI bus for the MAC. In other words, the MAC has the exclusive access to the ROM; access by the CPU will be delayed until this is unlocked. This is to allow the MAC to do certain sequence of operations without interruption.
MacLockCmd1	15:8	20h	Same as MacLockCmd0.
MacUnlockCmd0	23:16	04h	This is used to compare against the opcode sent out by the MAC. If SPI_Cntrl1[11] is set, the controller will unlock the SPI bus for the MAC. In other words, access by the CPU will be allowed again.
MacUnlockCmd1	31:24	04h	Same as MacUnlockCmd0
Note: When either SpiAccessMacRomEn and/or SpiHostAccessRomEn of offset 00h are cleared, all of the bits become read only and cannot be changed any more.			

SPI_CmdValue1 - RW - 32 bits - [Spi_Mem_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
WREN	7:0	06h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the WREN (write enable) command from the MAC. In the bridge mode, FCH will need to decode commands from the MAC.
WRDI	15:8	04h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the WRDI (write disable) command from the MAC.
RDID	23:16	9Fh	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the RDID (read ID) command from the MAC.
RDSR	31:24	05h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the RDSR (read status register) command from the MAC.
Note: When either SpiAccessMacRomEn and/or SpiHostAccessRomEn of offset 00h are cleared, all of the bits become read only and cannot be changed any more.			

SPI_CmdValue2 - RW - 32 bits - [Spi_Mem_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Read	7:0	03h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the Read (Read byte) command from the MAC. In the bridge mode, FCH will need to decode commands from the MAC.
FRead	15:8	0Bh	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the FRead (fast read) command from the MAC.
PAGEWR	23:16	0Ah	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the PAGEWR (page write) command from the MAC.
BYTEWR	31:24	02h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the BYTEWR (byte write) command from the MAC.
Note: When either SpiAccessMacRomEn and/or SpiHostAccessRomEn of offset 00h are cleared, all of the bits become read only and cannot be changed any more.			

Reserved- RW - 8 bits - [Spi_Mem_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	FFh	

Alt_SPI_CS - RW - 8 bits - [Spi_Mem_Reg: 1Dh]			
Field Name	**Bits**	**Default**	**Description**
AltSpiCsEn	1:0	00b	These two bits enable the alternate SPI_CS# 00 – select xSPI_CS# 01 – select xSPI_CS1# 10 – select xSPI_CS2# 10 – select xSPI_CS3#
WriteBufferEn	2	0b	SPI write performance enhancement. When set, SPI bridge can take burst write from the host and transfer it to the SPI flash.
SpiProtectEn0	3	0b	Enable SPI read/write protection base on PCI reg 0x50, 0x54, 0x58, 0x5C.

Alt_SPI_CS - RW - 8 bits - [Spi_Mem_Reg: 1Dh]			
Field Name	**Bits**	**Default**	**Description**
SpiProtectEn1	4	0b	Enable SPI protection to prevent host from accessing IMC, GEC, and USB3 space.
SpiProtectLock	5	0b	Once set, bits 3, 4, and 5 are no longer writeable.
SPiCsDlySel	7	0b	1: 125ns minimum SpiCs# de-assertion time. 0: 75ns minimum SpiCs# de-assertion time.

SpiIndexAddr - RW - 8 bits - [Spi_Mem_Reg: 1Eh]			
Field Name	**Bits**	**Default**	**Description**
SpiIndexAddr	7:0	00h	This is the address port of the extended SPI register

SpiIndexData - RW - 8 bits - [Spi_Mem_Reg: 1Fh]			
Field Name	**Bits**	**Default**	**Description**
SpiIndexData	7:0	00h	This is the data port of the extended SPI register

4.1.3 SPI Extended Controller Registers

Register Name	Offset Address
DDR_CMD	00h
QDR_CMD	01h
DPR_CMD	02h
QPR_CMD	03h
ModeByte	14h

DDR_CMD- RW - 8 bits - [Spi_Ext_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
DDR_CMD	7:0	3Bh	Programmable value for DDR command

QDR_CMD- RW - 8 bits - [Spi_Ext_Reg: 01h]			
Field Name	**Bits**	**Default**	**Description**
QDR_CMD	7:0	6Bh	Programmable value for QDR command

DPR_CMD- RW - 8 bits - [Spi_Ext_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
DPR_CMD	7:0	BBh	Programmable value for DPR command

QPR_CMD - RW - 8 bits - [Spi_Ext_Reg: 03h]			
Field Name	**Bits**	**Default**	**Description**
QPR_CMD	7:0	EBh	Programmable value for QPR command

ModeByte - RW - 8 bits - [Spi_Ext_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
ModeByte	7:0	00h	Whenever DPR_CMD or QPR_CMD is used, ModeByte is also sent out onto the SPI stream.

4.2 Host PCI Bridge Registers (Device 20, Function 4)

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
PCI Command	04h
PCI Device Status	06h
Revision ID/Class Code	08h
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
Reserved	0Fh
Primary Bus Number	18h
Secondary Bus Number	19h
Subordinate Bus Number	1Ah
Secondary Latency Timer	1Bh
IO Base	1Ch
IO Limit	1Dh
Secondary Status	1Eh
Memory Base	20h
Memory Limit	22h
Prefetchable Memory Base	24h
Prefetchable Memory Limit	26h
IO Base Upper 16 Bits	30h
IO Limit Upper 16 Bits	32h
Capability pointer	34h
Reserved	36h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Bridge Control	3Eh
Chip Control	40h
Diagnostic Control	41h
CLK Control	42h
Arbiter Control and Priority Bits	43h
SMLT Performance	44h
PMLT Performance	46h
PCDMA	48h
Additional Priority	49h
PCICLK Enable Bits	4Ah
Misc Control	4Bh
AutoClockRun Control	4Ch
Dual Address Cycle Enable and PCIB_SCLK_Stop Override	50h
MSI Mapping Capability	54h
Signature Register for Microsoft Rework for Subtractive Decode	58h
Prefetch Timeout Limit	5Ch
SPCI IDSEL MaskB	5Eh
Prefetch Size Control	60h
Misc Control	64h

Vender ID - R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1022h	Vendor Identifier. The vendor ID is 0x1002.
Vendor ID register			

Device ID - R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	780Fh	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.
Device ID register			

Command - RW - 16 bits - [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Enable	0	0b	I/O Response Enable. PCIB responds to I/O space accesses on the primary bus. 0: Disable 1: Enable
Memory Enable	1	0b	Memory Response Enable. PCIB responds to memory space accesses on the primary bus. 0: Disable 1: Enable
Master Enable	2	0b	Provides the ability of PCIB to act as a PCI bus master on the primary bus. 0: Disable 1: Enable
Special Enable	3	0b	Hardwired to 0 to indicate that PCIB ignores special cycles.
Mem Invalidate	4	0b	Hardwired to 0 to indicate that PCIB doesn't issue memory write and invalidate command by itself.
VGA Snoop Enable	5	0b	0: VGA palette write transactions on the primary interface are ignored unless it falls into PCIB's I/O address range. 1: VGA palette write transactions are positively decoded and forwarded downstream.
Parity Error Enable	6	0b	Parity Error Response. 0: Disables PCIB from asserting P_SERR# and P_PERR# and from reporting Detected Parity Error to the Status register. 1: Enables PCIB to assert P_SERR# and P_PERR# and to report Detected Parity Error bit to the Status register.
Addr Stepping Enable	7	0b	Controls whether or not to do address/data stepping, PCIB doesn't support address stepping. Read Only
System Error Enable	8	0b	SERR# Enable. 0: Disable PCIB from asserting P_SERR# and from reporting Signaled System Error bit. 1: Enable PCIB to assert P_SERR# and to report Signaled System Error bit.
Fast Back-to-Back Enable	9	0b	Hardwired to 0 to indicate that PCIB is not capable of issuing fast back-to-back transactions on the primary bus.
Reserved	15:10	00h	Reserved
PCI Command register			

Status - RW - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Reserved
Capabilities List	4	0b	Read only. This bit is 1 when reg0x40[3] (MSI Cap Enable) = 1. At other times this bit is 0. 0: The bridge does not support Capabilities List 1: The bridge supports Capabilities List (reg0x34 is the pointer to the data structure).
66MHz Capable	5	1b	Hardwired to 1 to indicate PCIB support of 66MHz primary interface.
Reserved	6	0b	Reserved
Fast Back-to-Back Capbable	7	1b	Hardwired to 1 to indicate PCIB is capable of accepting fast back-to-back transactions on the primary bus.
Master Parity Error	8	0b	Master Data Parity Error. An assertion of P_PERR# (when PCIB acts as a master) is received. Writing a 1 clears it.
DevSel Timing	9:10	01b	Hardwired to 01b to indicate PCIB will assert DEVSEL# with medium timing.
Target Abort	11	0b	Signaled Target Abort. Writing a 1 clears it.
Received Target Abort	12	0b	Received Target Abort. Writing a 1 clears it.
Received Master Abort	13	0b	Received Master Abort. Writing a 1 clears it.
Signaled System Error	14	0b	Signaled System Error bit. Writing a 1 clears it.
Parity Error	15	0b	Detected Parity Error. PCIB detected a parity error and will assert P_PERR#. Writing a 1 clears it.
PCI device status register.			

Revision ID/Class Code - R - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	40h	These bits are hardwired to reg0x40 (CPCTRL) to indicate the revision level of the chip design.
Class Code	31:8	060401h/ 060400h	A class code of 06h indicates a bridge device. A subclass code of 04h indicates PCI bridge. A programming interface of 01h indicates subtractive decoding on the primary bus is supported; whereas 00h indicates it is not supported. The programming interface is read-only in this register, but when reg0x4B[7] (SubDecodeEnable) and reg0x40[5] (Sub Decode Enable) are both 1, it reads 01h; otherwise it reads 00h.

Cache Line Size - RW - 8 bits - [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	Read Only

Primary Master Latency Timer - RW - 8 bits - [PCI_Reg:0Dh]			
Field Name	**Bits**	**Default**	**Description**
Prim Latency Timer	7:0	00h	Primary master latency timer. Sets the minimum time that the primary bus master can retain the ownership of the bus.

Header Type - R - 8 bits - [PCI_Reg:0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	81h	Indicates the bridge is a multi-function device.

Primary Bus Number - RW - 8 bits - [PCI_Reg:18h]			
Field Name	**Bits**	**Default**	**Description**
Primary Bus Number	7:0	00h	Bus number of the PCI bus to which the primary interface is connected.

Secondary Bus Number - RW - 8 bits - [PCI_Reg:19h]			
Field Name	**Bits**	**Default**	**Description**
Secondary Bus Number	7:0	00h	Bus number of the PCI bus to which the secondary interface is connected.

SUBBN - RW - 8 bits - [PCI_Reg:1Ah]			
Field Name	**Bits**	**Default**	**Description**
SubordinateBusNum	7:0	00h	Bus number of the highest numbered PCI bus behind PCIB.
Subordinate Bus Number register			

Secondary Latency Timer - RW - 8 bits - [PCI_Reg:1Bh]			
Field Name	**Bits**	**Default**	**Description**
Secondary Latency Timer	7:0	00h	Secondary master latency control timer. Sets the minimum time that the secondary bus master can retain the ownership of the bus.
Secondary Master Latency Timer register			

IO Base - RW - 8 bits - [PCI_Reg:1Ch]			
Field Name	**Bits**	**Default**	**Description**
IO16	1:0	00b	Indicates a 16-bit I/O address space. Read Only. Can be changed to 32-bit when reg0x4B[5] (IO Mode) is set.
Reserved	3:2	00b	Reserved
IOBase	7:4	0h	Defines the bits[15:12] of the base address of 16-bit or 32-bit I/O space.

IO Limit - RW - 16 bits - [PCI_Reg:1Dh]			
Field Name	**Bits**	**Default**	**Description**
IO16	1:0	00b	Indicates a 16-bit I/O address space. Read Only. Can be changed to 32-bit when reg0x4B[5] (IO Mode) is set.
Reserved	3:2	00b	Reserved
IO Limit	7:4	0h	Defines bits [15:12] of the limit of 16-bit or 32-bit I/O space.

Secondary Status - RW - 16 bits - [PCI_Reg:1Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	4:0	00h	Reserved
Sec 66MHz Capable	5	0b	Indicates PCIB doesn't support 66MHz secondary interface. Read Only.
Reserved	6	0b	Reserved
Secondary Fast Back-to-Back Capable	7	1b	Indicates PCIB is capable of accepting fast back-to-back transactions on the secondary bus. Read Only.
Secondary Master Data Parity Error	8	0b	Master Data Parity Error on the secondary bus, assertion of S_PERR# (when PCIB acts as a master) is received, writing a 1 clears it.
Secondary DevSel Timing	10:9	01b	DEVSEL# timing, indicates PCIB will assert DEVSEL# with medium timing on the secondary bus. Read Only.
Secondary Target Abort	11	0b	Signaled Target Abort on the secondary bus, writing a 1 clears it.
Received Secondary Target Abort	12	0b	Received Target Abort on the secondary bus. Writing a 1 clears it.
Received Secondary Master Abort	13	0b	Received Master Abort on the secondary bus. Writing a 1 clears it.
Received Serr	14	0b	Received System Error on the secondary bus, PCIB asserts P_SERR# to propagate the error back to the primary bus. Writing a 1 clears it.
Data Parity Error	15	0b	Detected Parity Error on the secondary bus, PCIB detected a parity error and will assert S_PERR#. Writing a 1 clears it.

Memory Base - RW - 16 bits - [PCI_Reg:20h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Indicates a non-prefetchable 32-bit memory space. Read Only.
Non Pref Mem Base	15:4	000h	Defines the highest 12 bits ([31:20]) of the base address of this 32-bit memory space.

Memory Limit - RW - 16 bits - [PCI_Reg:22h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Indicates a non-prefetchable 32-bit memory space. Read Only.
Non Pref Mem Limit	15:4	000h	Defines the highest 12 bits ([31:20]) of the upper limit of this 32-bit memory space.

Prefetchable Memory Base - RW - 16 bits - [PCI_Reg:24h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Indicates a 32-bit only memory space. Read Only
Pref Mem Base	15:4	000h	Defines the highest 12 bits ([31:20]) of the base address of this 32-bit memory space.

Prefetchable Memory Limit - RW - 16 bits - [PCI_Reg:26h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Indicates a 32-bit only memory space. Read Only.
Perf Mem Limit	15:4	000h	Defines the highest 12 bits ([31:20]) of the upper limit of this 32-bit memory space.

IO Base Upper 16 Bits - RW - 16 bits - [PCI_Reg:30h]			
Field Name	**Bits**	**Default**	**Description**
IOBase Upper	15:0	0000h	Top 16 bits of the base address of 32-bit I/O transactions. If the I/O address decode mode bit, i.e., reg0x4B[5] (IO Mode), is cleared, then these bits will be 0s.

IO Limit Upper 16 bits - RW - 16 bits - [PCI_Reg:32h]			
Field Name	**Bits**	**Default**	**Description**
IOLimit Upper	15:0	0000h	Top 16 bits of the upper limit of 32-bit IO transactions. If the I/O address decode mode bit, i.e., reg0x4B[5] (IO Mode), is cleared, then these bits will be 0s.

Capabilities Pointer - R - 8 bits - [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	00h	Enhanced Capability Pointer. Read Only. Value = 54h when reg0x40[3] (MSI Cap Enable) is set to 1.

Interrupt Line - R - 8 bits - [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	Interrupt pin routing information, used as communication window between BIOS and the device driver.

Interrupt Pin - R - 8 bits - [PCI_Reg:3Dh]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin	7:0	00h	Interrupt pin usage information. 0 indicates PCIB does not support interrupt routing.

Bridge Control - RW - 16 bits - [PCI_Reg:3Eh]			
Field Name	**Bits**	**Default**	**Description**
Parity Error Enable	0	0b	Parity Error Response. 0: Disable PCIB from asserting P_SERR# and S_PERR# and from reporting Detected Parity Error to the Secondary Status register. 1: Enable PCIB to assert P_SERR# and S_PERR# and to report Detected Parity Error to the Secondary Status register.
SERRr# Enable	1	0b	SERR# Forward Enable. 0: PCIB doesn't drive P_SERR# when it detects S_SERR#. 1: PCIB drives P_SERR# when it detects S_SERR#, if reg0x04[8] (System Error Enable) is set.
ISA_Enable	2	0b	ISA Enable. 0: No ISA address mode 1: ISA address mode is supported.

Bridge Control - RW - 16 bits - [PCI_Reg:3Eh]			
Field Name	**Bits**	**Default**	**Description**
VGA_Enable	3	0b	VGA Enable. 0: Disable 1: Enable
VGA 16-bit Decode	4	0b	This bit only has meaning if either bit[3] (VGA Enable) of this register, or bit[5] (VGA Palette Snoop Enable) of the Command register, is also set to 1, thereby enabling VGA I/O decoding and forwarding by the bridge. The status after reset is 0. This read/write bit enables system configuration software to select between 10-bit and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from the primary to the secondary bus. 0: Execute 10-bit address decodes on VGA I/O accesses. 1: Execute 16-bit address decodes on VGA I/O Accesses.
Master Abort Report	5	0b	0: Do not report master aborts (return FFFF,FFFFh on reads and discard data on write) 1: Report master aborts by signaling target abort or by asserting SERR# if enabled.
Secondary Reset	6	0b	Secondary bus reset. This bit can be masked using ACPI PCI Config register (pmio reg0x04[25]). 0: Disable 1: Trigger reset
Secondary Fast Back-to-Back Enable	7	0b	PCIB is not capable of issuing fast back-to-back transactions on the secondary bus. Read Only
Primary Discard Timer	8	0b	Primary Discard Timer configuration 0: Configure the timer to 15-bit 1: Configure the timer to 10-bit
Secondary Discard Timer	9	0b	Secondary Discard Timer configuration 0: Configure the timer to 15-bit 1: Configure the timer to 10-bit
Discard Timer Status	10	0b	0: No discard timer error 1: Discard timer error
Discard Timer Serr# Enable	11	0b	0: Disable 1: Enable
Reserved	15:12	0h	Reserved

CPCTRL - RW - 8 bits - [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved
Mem Write Size Ctrl	1	0b	Controls the memory write size. When set, the memory write size will be cacheline aligned; else it will be 32-byte aligned.
Lock Enable	2	1b	Downstream locked transaction enable.
MSI Cap Enable	3	0b	MSI Capability Enable Guide bit. Setting this bit to 1 will change the status of reg0x06[4] (Capablities List) from 0 to 1 and will change reg0x34[7:0] (Capabilities Pointer) from the default value of 00h to 54h. 1: Enable 0: Disable
Reserved	4	0b	Reserved
Sub Decode Enable	5	0b	This bit is used only when reg0x4B[7] (SubDecodeEnable) = 1. 1: Subtractive decoding is enabled. 0: Subtractive decoding is disabled.

CPCTRL - RW - 8 bits - [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
Bridge Lock State	7:6	00b	Bridge secondary master lock states. Read Only 00: Free 01: Busy 10: Req 11: Locked
Chip control register			

DCTRL - RW - 8 bits - [PCI_Reg:41h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved
Timer Test Mode	2:1	00b	00: Normal operation, all bits are exercised 01: Byte 1 is exercised 10: Byte 2 is exercised 11: Byte 0 is exercised
Force Parity Error	3	0b	Force receiving/generating parity error 0: Receive 1: Generate
Force Data Parity Error	4	0b	Force data parity error 0: Disable 1: Enable
Force Addr Parity Error	5	0b	Force address parity error 0: Disable 1: Enable
Force Sec Parity Error	6	0b	Force secondary Parity Error Mode 0: Disable 1: Enable
Force Prim Parity Error	7	0b	Force primary Parity Error Mode 0: Disable 1: Enable
Diagnostic control register			

CLKCTRL - RW - 8 bits - [PCI_Reg:42h]			
Field Name	**Bits**	**Default**	**Description**
PCICLKStopEnable	0	0b	33MHz PCICLKs request bit. 1: 33 MHz PCI clocks are requested to stop.
PCICLKStopStatus	1	0b	Read only. 33MHz PCICLKs stop status: 1: Stopped 0: Running.
PCICLK0Enable	2	1b	33MHz PCICLK0 Enable.
PCICLK1Enable	3	1b	33MHz PCICLK1 Enable.
PCICLK2Enable	4	1b	33MHz PCICLK2 Enable.
PCICLK3Enable	5	1b	33MHz PCICLK3 Enable.
P2SControl	6	0b	P_CLK domain to S_CLK domain synch-up disable.
S2PControl	7	0b	S_CLK domain to P_CLK domain synch-up disable.
Clock control register			

ARCTRL - RW - 8 bits - [PCI_Reg:43h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	6:0	ffh	Reserved
ArbiterEnable	7	1b	Arbiter Enable. 0: Disabled to give PCIB the exclusive ownership of the secondary bus.
Arbiter control register			

SMLT_PERF - R - 16 bits - [PCI_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
SMLT_Perf	15:0	0000h	Count the total number of a burst being broken into multiple transactions due to MLT timeout.
Secondary MLT performance register			

PMLT_PERF - R - 16 bits - [PCI_Reg:46h]			
Field Name	**Bits**	**Default**	**Description**
PMLT_Perf	15:0	0000h	Count the total number of a burst being broken into multiple transactions due to MLT timeout.
Primary MLT performance register			

PCDMA - RW - 8 bits - [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
PCDMA Device Enable A	0	0b	Device enable for request 3. Needs to be enabled when there is a PCDMA device corresponding to request 3
PCDMA Device Enable B	1	0b	Device enable for request 4. Needs to be enabled when there is a PCDMA device corresponding to request 4
Fast Back to Back Retry Enable	2	0b	Retry Fast Back to Back transactions on Write buffer full.
Lock Operation Enable	3	1b	When reg0x40[2] (Lock Enable) =1, this bit should be set to 1 for the proper operation of the PCI LOCK# function.
Reserved	7:4	00h	Reserved
PCDMA Device Enable bits			

Additional Priority Bits - RW - 8 bits - [PCI_Reg:49h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	1b	Reserved
PCDMA Priority	1	1b	If enabled, include PCDMA request into the high priority list.
Reserved	7:2	03h	Reserved

PCICLK Enable Bits - RW - 8 bits - [PCI_Reg:4Ah]			
Field Name	**Bits**	**Default**	**Description**
PCICLK4Enable	0	1b	33MHz PCICLK4 Enable.
PCICLK5Enable	1	1b	33MHz PCICLK 5 Enable.
PCICLK6Enable	2	1b	33MHz PCICLK 6 Enable.
PCICLK7Enable	3	1b	33MHz PCICLK 7 Enable.
Reserved	7:4	3h	Reserved

Misc Control - RW - 8 bits - [PCI_Reg:4Bh]			
Field Name	**Bits**	**Default**	**Description**
GNT Bus Idle check enable	0	1b	When enabled, the PCI arbiter checks for Bus Idle before asserting GNT#.
Memory Read Burst Size	4:1	0h	Specifies up to how many double words burst to support during an upstream or downstream memory read. 1xxx: Burst up to 16 double words 01xx: Burst up to 8 double words 001x: Burst up to 4 double words 0001: Burst up to 2 double words Others: Burst up to 8 double words Note 1: It has no effect on a downstream normal memory read (other than read line and read multiple), which has no burst in this design. Note 2: It has no effective on an upstream memory read if the read is prefetchable as specified by reg0x64[7] (Prefetch Enable For Upstream Read Line and Read Multiple) and reg0x64h[21] (Prefetch Disable for Upstream Normal Mem Read), because a prefetchable read can have unlimited burst.
IOMode	5	0b	Control bit to change the I/O addressing mode to 32/16 bit. 0: 16-bit; 1: 32-bit.
MemReadCmdMatch	6	0b	Control bit to enable the match of memory read/memory read line commands when there is a read command in the Delay queue.
SubDecodeEnable	7	0b	Control bit for the subtractive decode status (reg0x08[8] (Class Code)). 0: No subtractive decode; 1: Whether subtractive decode is enabled depends on reg0x40[5] (Sub Decode Enable).

AutoClockRun Control - RW - 32 bits - [PCI_Reg:4Ch]			
Field Name	**Bits**	**Default**	**Description**
Autoclkrun Enable	0	0b	Enable the auto clkrun functionality.
Autoclkrun Count	31:1	0000_000 0h	Number of cycles after which the secondary clock stops when clkrun is enabled.

Dual Address Cycle Enable and PCIB_CLK_Stop Override - RW - 16 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
PCIB_Dual_EN_up	0	0b	Enable decoding of Dual Address Cycle on secondary side for upstream memory transactions.
PCIB_Dual_EN_dn	1	0b	Enable decoding of Dual Address Cycle on secondary side for downstream memory transactions.
Reserved	5:2	0h	
ClkrunOvrridePCICLK	6	0b	When set, overrides the CLKRUN# and 33MHz PCICLK continues to run.
ClkrunOvrridePCICLK1	7	0b	When set, overrides the CLKRUN# and 33MHz PCICLK1 continues to run.
ClkrunOvrridePCICLK2	8	0b	When set, overrides the CLKRUN# and 33MHz PCICLK2 continues to run.
ClkrunOvrridePCICLK3	9	0b	When set, overrides the CLKRUN# and 33MHz PCICLK3 continues to run.

Dual Address Cycle Enable and PCIB_CLK_Stop Override - RW - 16 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
ClkrunOvrridePCICLK4	10	0b	When set, overrides the CLKRUN# and 33MHz PCICLK4 continues to run.
ClkrunOvrrideLPCCLK	11	0b	When set, overrides the CLKRUN# and LPCCLK continues to run.
ClkrunOvrrideLPCCLK1	12	0b	When set, overrides the CLKRUN# and LPCCLK1 continues to run.
ClkrunOvrridePCICLKFB	13	0b	When set, overrides the CLKRUN# and 33MHz PCICLKFB continues to run. PCICLKFB is the feedback clock that is used internally by PCIB.
Reserved	14	0b	
Reserved	15	0b	

MSI Mapping Capability - R - 32 bits - [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	**Description**
MSI Cap ID	7:0	08h	MSI Capability ID
MSI Cap Pointer	15:8	00h	MSI Capabilities Pointer
MSI Cap Enable	16	1b	MSI Capabilities Enable
MSI Fixed	17	1b	MSI Fixed
MSI Reserved	26:18	000h	Reserved
MSI CapType	31:27	15h	MSI Capability Type

Signature Register for Microsoft Rework for Subtractive Decode - R - 32 bits - [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
Signature Register for Microsoft Rework for Subtractive Decode	31:0	00000000h	When Microsoft Rework for Subtractive Decode is done, this register will contain the signature value.

Prefetch Timeout Limit – RW - 16 bits - [PCI_Reg:5Ch]			
Field Name	**Bits**	**Default**	**Description**
Prefetch Timeout Limit	15:0	0085h	When deep prefetch is enabled (reg0x64h[7] (Prefetch Enable For Upstream Read Line and Read Multiple) =1), this timer determines when to flush the stale data in the buffer. Each count is 30ns.

SPCI IDSEL MaskB – RW - 16 bits - [PCI_Reg:5Eh]			
Field Name	**Bits**	**Default**	**Description**
PCI IDSEL MaskB	15:0	FFFFh	Each bit represents masking of the specific device on the PCI bus. The purpose of this register is to hide the device from the OS. 0: The corresponding IDSEL bit is masked. 1: The corresponding IDSEL bit is not masked.

Prefetch Size Control – RW - 32 bits - [PCI_Reg:60h]			
Field Name	**Bits**	**Default**	**Description**
Read Size	2:0	2h	If prefetch function is enabled, this defines the number of initial prefetch cachelines for a PCI READ command.
Read Size Adjustment	3	1b	When set, PCIBridge will adjust the prefetch size for READ automatically. If this bit is 0, then the prefetch size is always defined by bits[2:0].
Read Line Size	6:4	4h	If prefetch function is enabled, this defines the number of initial prefetch cachelines for a PCI READLINE command.
Read Line Adjustment	7	1b	When set, PCIBridge will adjust the prefetch size for READ_LINE automatically. If this bit is 0, then the prefetch size is always defined by bits[6:4].
Read Multiple Size	10:8	6h	If the prefetch function is enabled, this defines the number of initial prefetch cachelines for a PCI READ_MULTIPLE command.
Read Multiple Adjustment	11	1b	When set, PCIBridge will adjust the prefetch size for READ_MULTIPLE automatically. If this bit is 0, then the prefetch size is always defined by bits[10:8].
Prefetch Size Lower Limit	14:12	0h	The lower limit of the adjusted prefetch size.
Reserved	15	0b	
Prefetch Size Upper Limit	18:16	7h	The upper limit of the adjusted prefetch size.
Reserved	19	0b	
Prefetch Size Mlt Enable	20	1b	This also controls how PCIBridge adjusts the auto-prefetch size. When set, PCIBridge will only adjust the prefetch size if it knows it does not have enough or has too much data in the prefetch buffer. It is recommended to always set this bit.
Reserved	31:21	0h	
The fields in this register are effective only when prefetch is enabled, i.e., reg0x64[7] (Prefetch Enable For Upstream Read Line and Read Multiple) = 1.			

Misc Control Register - RW - 32 bits - [PCI_Reg:64h]			
Field Name	**Bits**	**Default**	**Description**
Downstream Config Cycle Flush Enable	0	0h	When this bit is 1, any downstream config cycle will flush all the upstream read prefetch buffers.
Downstream Write Cycle Flush Enable	1	1h	When this bit is 1, any downstream non-config write cycle will flush all the upstream read prefetch buffers.
Downstream Read Cycle Flush Enable	2	0h	When this bit is 1, any downstream non-config read cycle will flush all the upstream read prefetch buffers.
Prefetch Buffer Timeout Enable	3	1h	When this bit is 1, upstream read prefetch buffer timeout mechanism is enabled. If data stay in a buffer longer than the time specified in Prefetch Timeout Limit (reg0x5C), the buffer will be flushed.
AB Masking Prefetch Request Enable	4	1h	The purpose of this bit is to improve the internal bus efficiency and the recommendation is to have it set to 1.
AB Masking Non-prefetch Request Enable	5	1h	The purpose of this bit is to improve the internal bus efficiency and the recommendation is to have it set to 1.
Downstream Cycle Flush Control	6	0h	0: If a downstream cycle is qualified to flush upstream prefetch read buffer (depending on bits[2:0] in this register), the flush happens when the cycle is sent out onto the PCI bus with at least one data phase. 1: If a downstream cycle is qualified to flush upstream prefetch read buffer (depending on bits[2:0] in this register), the flush happens as soon as the cycle arrives at the PCI bus.

Misc Control Register - RW - 32 bits - [PCI_Reg:64h]			
Field Name	**Bits**	**Default**	**Description**
Prefetch Enable For Upstream Read Line and Read Multiple	7	1h	0: Prefetch is disabled for upstream memory read line and memory read multiple. 1: Prefetch is enabled for upstream memory read line and memory read multiple. Also refer to bit[21] (Prefetch Disable for Upstream Normal Mem Read).
Reserved	8	0h	
Arbiter 2 Enable	9	0h	Enables the use of the new PCI bus arbiter to replace the old arbiter.
Hold Current Grant	10	0h	When set, PCIGNT# will not be deasserted until the requesting agent deasserts its PCIREQ#. This only applies to the new PCI bus arbiter.
Single Cycle Prefetch Control	11	1h	If a prefetch read cycle comes from the SPCI bus, prefetching may not be necessary if the cycle is single data phase. PCIB can optionally treat the single cycle as non-prefetch and only asks for one dword from AB. 1: Turn on the ability to treat single data phase cycle as non-prefetch cycle. 0: Turn off the ability to treat single data phase cycle as non-prefetch cycle.
Fast Grant Deassert En	12	1h	This control bit applies only to the old (default) PCI arbiter. Normally PCIGNT# is deasserted two clocks after PCIREQ# deasserts. With this bit set, PCIGNT# will deassert 1 clock after PCIREQ# deasserts. It is recommended to have this bit set.
Reserved	14:13	0h	
Prim2SecHandshakeFix	15	0h	Set to enable additional handshake between internal A-Link and PCI bus.
Reserved	18:16	0h	
Upstream Flush Disable	19	0h	If an SPCI bus device has left some prefetched data in PCIB's prefetch buffer(s), and next time the same device comes back with another request that does not consume the prefetched data, the data is flushed. This is to ensure the prefetched data does not become stale when the same device no longer needs it. 0: Such flush is enabled. 1: Such flush is disabled.
One Prefetch Channel Enable	20	0h	When this bit is set to 1, the four upstream read prefetch channels are cut to one channel.
Prefetch Disable for Upstream Normal Mem Read	21	0	0: Prefetch is enabled for upstream normal memory read (other than read line or read multiple). However, if bit[7] (Prefetch Enable For Upstream Read Line and Read Multiple) = 0, this prefetch remains disabled. 1: Prefetch is disabled for upstream normal memory read (other than read line or read multiple). Also refer to bit[7] (Prefetch Enable For Upstream Read Line and Read Multiple).
Reserved	24:22	0h	
Spci Grant 3 Output Enable	25	0h	0: Disable spci gnt 3 output. 1: Enable spci gnt 3 output.
Reserved	31:26	0h	

Chapter 5
PCIe® Bridge Registers

Click the following link to go to the PCIe® Bridge Registers section:

section 5.1, "PCIe Bridge Registers (Device 21, Function 0/1/2/3)," on page 5- 516

5.1 PCIe Bridge Registers (Device 21, Function 0/1/2/3)

Bolton provides 4 lanes for PCIe GEN-2 connection, supporting up to 4 general purpose devices. Supported configurations include:

- 1 port : 4 lanes
- 2 ports: 2 lanes each
- 3 ports: port-1 with 2 lanes and port-2 and port-3 with 1 lane each
- 4 ports: 1 lane each

Each port is controlled by one PCIe bridge. The number of PCIe bridges goes from 1 to 4, depending on the system configuration. System software needs to program the proper port configuration through ABCFG_Reg xC0 before enabling any of the PCIe ports.

Register Name	Offset Address
VENDOR_ID	00h
DEVICE_ID	02h
COMMAND	04h
STATUS	06h
REVISION_ID	08h
PROG_INTERFACE	09h
SUB_CLASS	0Ah
BASE_CLASS	0Bh
CACHE_LINE	0Ch
LATENCY	0Dh
HEADER	0Eh
BIST	0Fh
SUB_BUS_NUMBER_LATENCY	18h
IO_BASE_LIMIT	1Ch
SECONDARY_STATUS	1Eh
MEM_BASE_LIMIT	20h
PREF_BASE_LIMIT	24h
PREF_BASE_UPPER	28h
PREF_LIMIT_UPPER	2Ch
IO_BASE_LIMIT_HI	30h
IRQ_BRIDGE_CNTL	3Eh
CAP_PTR	34h
INTERRUPT_LINE	3Ch
INTERRUPT_PIN	3Dh
EXT_BRIDGE_CNTL	40h
PMI_CAP_LIST	50h
PMI_CAP	52h
PMI_STATUS_CNTL	54h
PCIE_CAP_LIST	58h
PCIE_CAP	5Ah
DEVICE_CAP	5Ch
DEVICE_CNTL	60h
DEVICE_STATUS	62h
LINK_CAP	64h
LINK_CNTL	68h
LINK_STATUS	6Ah
SLOT_CAP	6Ch
SLOT_CNTL	70h
SLOT_STATUS	72h
ROOT_CNTL	74h
ROOT_CAP	76h
ROOT_STATUS	78h
DEVICE_CAP2	7Ch
DEVICE_CNTL2	80h
DEVICE_STATUS2	82h
LINK_CAP2	84h

Register Name	Offset Address
LINK_CNTL2	88h
LINK_STATUS2	8Ah
SLOT_CAP2	8Ch
SLOT_CNTL2	90h
SLOT_STATUS2	92h
MSI_CAP_LIST	A0h
MSI_MSG_CNTL	A2h
MSI_MSG_ADDR_LO	A4h
MSI_MSG_ADDR_HI	A8h
MSI_MSG_DATA_64	ACh
MSI_MSG_DATA	A8h
SSID_CAP_LIST	B0h
SSID_ID	B4h
MSI_MAP_CAP_LIST	B8h
PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST	100h
PCIE_VENDOR_SPECIFIC_HDR	104h
PCIE_VENDOR_SPECIFIC1	108h
PCIE_VENDOR_SPECIFIC2	10Ch
PCIE_VC_ENH_CAP_LIST	110h
PCIE_PORT_VC_CAP_REG1	114h
PCIE_PORT_VC_CAP_REG2	118h
PCIE_PORT_VC_CNTL	11Ch
PCIE_PORT_VC_STATUS	11Eh
PCIE_VC0_RESOURCE_CAP	120h
PCIE_VC0_RESOURCE_CNTL	124h
PCIE_VC0_RESOURCE_STATUS	12Ah
PCIE_VC1_RESOURCE_CAP	12Ch
PCIE_VC1_RESOURCE_CNTL	130h
PCIE_VC1_RESOURCE_STATUS	136h
PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST	140h
PCIE_DEV_SERIAL_NUM_DW1	144h
PCIE_DEV_SERIAL_NUM_DW2	148h
PCIE_ADV_ERR_RPT_ENH_CAP_LIST	150h
PCIE_UNCORR_ERR_STATUS	154h
PCIE_UNCORR_ERR_MASK	158h
PCIE_UNCORR_ERR_SEVERITY	15Ch
PCIE_CORR_ERR_STATUS	160h
PCIE_CORR_ERR_MASK	164h
PCIE_ADV_ERR_CAP_CNTL	168h
PCIE_HDR_LOG0	16Ch
PCIE_HDR_LOG1	170h
PCIE_HDR_LOG2	174h
PCIE_HDR_LOG3	178h
PCIE_ROOT_ERR_CMD	17Ch
PCIE_ROOT_ERR_STATUS	180h
PCIE_ERR_SRC_ID	184h
PCIE_ACS_ENH_CAP_LIST	190h
PCIE_ACS_CAP	194h
PCIE_ACS_CNTL	196h

VENDOR_ID - RW - 16 bits - pcieCfg0:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID (R)	15:0	1022	This field identifies the manufacturer of the device. 0FFFFh is an invalid value for Vendor ID.

Vendor Identification

DEVICE_ID - R - 16 bits - pcieCfg0:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	43A0/ 43A1/ 43A2/ 43A3	This field identifies the particular device. This identifier is allocated by the vendor. fun-0: 43A0 fun-1: 43A1 fun-2: 43A2 fun-3: 43A3

Device Identification

COMMAND - RW - 16 bits - pcieCfg0:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0. 0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0. 0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	Controls the ability of a PCI Express endpoint to issue Memory and I/O Read/Write requests, and the ability of a Root or Switch Port to forward Memory and I/O Read/Write requests in the upstream direction. 0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
PARITY_ERROR_RESPONSE	6	0x0	Parity Error Response. Default value of this field is 0. 0=Disable 1=Enable
AD_STEPPING (R)	7	0x0	Address and Data Stepping. Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
SERR_EN	8	0x0	When set, enables reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. 0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable

COMMAND - RW - 16 bits - pcieCfg0:0x4			
Field Name	**Bits**	**Default**	**Description**
INT_DIS	10	0x0	Controls the ability of a PCI Express device to generate INTx interrupt messages. When set, devices are prevented from generating INTx interrupt messages. Default value 0 0=Enable 1=Disable\

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

STATUS - RW - 16 bits - pcieCfg0:0x6			
Field Name	**Bits**	**Default**	**Description**
INT_STATUS (R)	3	0x0	Indicates that an INTx interrupt message is pending internally to the device.
CAP_LIST (R)	4	0x1	Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.
PCI_66_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
UDF_EN (R)	6	0x0	User Defined Status Enable 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Does not apply to PCI Express. Hardwired to 0.
MASTER_DATA_PARITY_ERROR	8	0x0	This bit is set by Requestor if its Parity Error Enable bit is set and either of the following two conditions occurs: 1) Requestor receives a Completion marked as poisoned 2) Requestor poisons a write Request 0=Inactive 1=Active
DEVSEL_TIMING (R)	10:9	0x0	Does not apply to PCI Express. Hardwired to 0.
SIGNAL_TARGET_ABORT	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status. 0=No Abort 1=Target Abort
RECEIVED_TARGET_ABORT	12	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
RECEIVED_MASTER_ABORT	13	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	This bit must be set whenever the device asserts SERR#. 0=No Error 1=SERR assert
PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL message, and the SERR Enable bit in the Command register is 1.

The Status register is used to record status information for PCI bus related events.

REVISION_ID - R - 8 bits - pcieCfg0:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Major revision ID. Set by the vendor.
MAJOR_REV_ID	7:4	0x0	Minor revision ID. Set by the vendor.

Specifies a device specific revision identifier. The value is chosen by the vendor.

PROG_INTERFACE - R - 8 bits - pcieCfg0:0x9			
Field Name	**Bits**	**Default**	**Description**
PROG_INTERFACE	7:0	0x0	Unused, for test environment only

Register-Level Programming Interface Register

SUB_CLASS - R - 8 bits - pcieCfg0:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS	7:0	0x4	Read-only and used with the Base Class Code to identify the specific type of device.

Sub Class Code Register

BASE_CLASS - R - 8 bits - pcieCfg0:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS	7:0	0x6	Read-only and used to identify the generic function of the device.

Base Class Code Register

CACHE_LINE - RW - 8 bits - pcieCfg0:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	This read/write register specifies the system cacheline size in units of DWORDs.

Cache Line Size Register

LATENCY - RW - 8 bits - pcieCfg0:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER (R)	7:0	0x0	Primary/Master latency timer does not apply to PCI Express. Register is hardwired to 0.

Master Latency Timer Register

HEADER - RW - 8 bits - pcieCfg0:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE (R)	6:0	0x1	Type 0 or Type 1 Configuration Space
DEVICE_TYPE (R)	7	0x1	Single function or multi function device 0=Single-Function Device 1=Multi-Function Device

Configuration Space Header

BIST - RW - 8 bits - pcieCfg0:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP (R)	3:0	0x0	A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device-specific failure codes can be encoded in the non-zero value.
BIST_STRT (R)	6	0x0	Write a 1 to invoke BIST. Device resets the bit when BIST is complete. Software should fail the device if BIST is not complete after 2 seconds.
BIST_CAP (R)	7	0x0	This bit is read-only and returns a 1 if the bridge supports BIST, otherwise a 0 is returned.

Built In Self Test Register used for control and status of built-in self tests

SUB_BUS_NUMBER_LATENCY - RW - 32 bits - pcieCfg0:0x18			
Field Name	**Bits**	**Default**	**Description**
PRIMARY_BUS	7:0	0x0	Primary Bus Number. Records the bus number of the PCI bus segment to which the primary interface of the bridge is connected.
SECONDARY_BUS	15:8	0x0	Secondary Bus Number. Used to record the bus number of the PCIE bus segment to which the secondary interface of the brdige is connected.
SUB_BUS_NUM	23:16	0x0	Subordinate Bus Number. Used to record the bus number of the highest numbered PCI bus segment which is behind the bridge.
SECONDARY_LATENCY_TIMER (R)	31:24	0x0	Does not apply to PCI Express. Hardwired to 0.

Subordinate Bus Number Latency

IO_BASE_LIMIT - RW - 16 bits - pcieCfg0:0x1C			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_TYPE (R)	3:0	0x1	I/O Base Addressing Type 0=16-bit 1=32-bit
IO_BASE	7:4	0x0	I/O Base Register
IO_LIMIT_TYPE (R)	11:8	0x1	I/O Limit Addressing Type 0=16-bit 1=32-bit
IO_LIMIT	15:12	0x0	I/O Limit Register

I/O Base Register Limit is used by the bridge to determine when to forward I/O transactions from one interface to the other.

SECONDARY_STATUS - RW - 16 bits - pcieCfg0:0x1E			
Field Name	**Bits**	**Default**	**Description**
CAP_LIST (R)	4	0x0	Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.
PCI_66_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
UDF_EN (R)	6	0x0	User Defined Status Enable 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Does not apply to PCI Express. Hardwired to 0.
MASTER_DATA_PARITY_ERROR	8	0x0	This bit is set by Requestor if its Parity Error Enable bit is set and either of the following two conditions occurs: 1) Requestor receives a Completion marked as poisoned 2) Requestor poisons a write Request 0=No error 1=Parity error
DEVSEL_TIMING (R)	10:9	0x0	Does not apply to PCI Express. Hardwired to 0.
SIGNAL_TARGET_ABORT	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status. 0=No Abort 1=Target Abort asserted
RECEIVED_TARGET_ABORT	12	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=No CA Received 1=Received Completion Abort
RECEIVED_MASTER_ABORT	13	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=No UR Received 1=Received Unsupported Request
RECEIVED_SYSTEM_ERROR	14	0x0	This bit reports the detection of an system error on the secondary inteface of the bridge. 1 is assered if a system error has been detected. 0=No Error 1=Sent Error Meesage
PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL message, and the SERR Enable bit in the Command register is 1. 0=No Error 1=Received Poisoned TLP

Secondary Status Register. Its bits reflect status conditions of the secondary interface

MEM_BASE_LIMIT - RW - 32 bits - pcieCfg0:0x20			
Field Name	**Bits**	**Default**	**Description**
MEM_BASE_TYPE (R)	3:0	0x0	Memory Base Addressing Type 0=32-bit 1=64-bit
MEM_BASE_31_20	15:4	0x0	Memory Base Register
MEM_LIMIT_TYPE (R)	19:16	0x0	Memory Limit Addressing Type 0=32-bit 1=64-bit
MEM_LIMIT_31_20	31:20	0x0	Memory Limit Register

Memory Limit Register defines a memory mapped I/O address range which is used by the bridge to determine when to forward memory transactions from one interface to the other

PREF_BASE_LIMIT - RW - 32 bits - pcieCfg0:0x24			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_BASE_TYPE (R)	3:0	0x1	Prefetchable Memory Base Addressing Type 0=32-bit 1=64-bit
PREF_MEM_BASE_31_20	15:4	0x0	Prefetchable Memory Base Register
PREF_MEM_LIMIT_TYPE (R)	19:16	0x1	Prefetchable Memory Limit Addressing Type 0=32-bit 1=64-bit
PREF_MEM_LIMIT_31_20	31:20	0x0	Prefetchable Memory Limit Register

Prefetchable Memory Base Limit indicates 64-bit addresses are supported.

PREF_BASE_UPPER - RW - 32 bits - pcieCfg0:0x28			
Field Name	**Bits**	**Default**	**Description**
PREF_BASE_UPPER	31:0	0x0	Upper 32 bits for 64-bit address.

Prefetchable Memory Base Upper 32 bits.

PREF_LIMIT_UPPER - RW - 32 bits - pcieCfg0:0x2C			
Field Name	**Bits**	**Default**	**Description**
PREF_LIMIT_UPPER	31:0	0x0	Upper 32 bits for 64-bit address.

Prefetchable Memory Limit Upper 32 bits.

IO_BASE_LIMIT_HI - RW - 32 bits - pcieCfg0:0x30			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_31_16	15:0	0x0	Upper 16 bits for 32-bit address.
IO_LIMIT_31_16	31:16	0x0	Upper 16 bits for 32-bit address.

I/O Base and I/O Limit Upper 16 bits.

IRQ_BRIDGE_CNTL - RW - 16 bits - pcieCfg0:0x3E			
Field Name	**Bits**	**Default**	**Description**
PARITY_RESPONSE_EN	0	0x0	Parity Error Response Enable. Controls the response to poisoned TLPs.
SERR_EN	1	0x0	System Error Enable. Controls forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary.
ISA_EN	2	0x0	ISA Enable. Modifies the response by the bridge to ISA I/O addresses.
VGA_EN	3	0x0	VGA Enable. Modifies the response by the bridge to VGA compatible addresses.

IRQ_BRIDGE_CNTL - RW - 16 bits - pcieCfg0:0x3E			
Field Name	**Bits**	**Default**	**Description**
VGA_DEC	4	0x0	Enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 kB.
MASTER_ABORT_MODE (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
SECONDARY_BUS_RESET	6	0x0	Secondary Bus Reset. Triggers a hot reset on the corresponding PCI Express Port. 0=Run 1=Reset
FAST_B2B_EN (R)	7	0x0	Fast Back-to-Back Transactions Enable. Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable

Bridge Control Register

CAP_PTR - RW - 32 bits - pcieCfg0:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR (R)	7:0	0x50	Pointer to a linked list of additional capabilities implemented by this device. 50=Point to PM Capability

Capability Pointer

INTERRUPT_LINE - RW - 8 bits - pcieCfg0:0x3C			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0xff	Interrupt Line. Communicates interrupt line routing information.

Interrupt Line Register

INTERRUPT_PIN - RW - 8 bits - pcieCfg0:0x3D			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN	7:0	0x0	Read-only. Identifies the legacy interrupt message(s) the device (or device function) uses. NOTE: Bits 3:7 of this field are hardwired to ZERO.

Interrupt Pin Register

EXT_BRIDGE_CNTL - RW - 8 bits - pcieCfg0:0x40			
Field Name	**Bits**	**Default**	**Description**
IO_PORT_80_EN	0	0x0	Enable I/O port 80 decoding.

External Bridge Control Register

PMI_CAP_LIST - R - 16 bits - pcieCfg0:0x50			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x1	Capability ID. Must be set to 01h 1=PCIE Power Management Registers
NEXT_PTR	15:8	0x58	Next Capability Pointer

Power Management Capbility List

PMI_CAP - RW - 16 bits - pcieCfg0:0x52			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	2:0	0x3	Version 3=PMI Spec 1.2
PME_CLOCK (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0.
DEV_SPECIFIC_INIT (R)	5	0x0	Device Specific Initialization
AUX_CURRENT	8:6	0x0	AUX Current
D1_SUPPORT (R)	9	0x0	D1 Support 1=Support D1 PM State.
D2_SUPPORT (R)	10	0x0	D2 Support 1=Support D2 PM State.
PME_SUPPORT (R)	15:11	0x0	For a given device, this indicates the power states in which the device may generate a PME.

Power Management Capabilities Register

PMI_STATUS_CNTL - RW - 32 bits - pcieCfg0:0x54			
Field Name	**Bits**	**Default**	**Description**
POWER_STATE	1:0	0x0	Power State
NO_SOFT_RESET (R)	3	0x0	No Soft Reset
PME_EN	8	0x0	PME Enable
DATA_SELECT (R)	12:9	0x0	Data Select
DATA_SCALE (R)	14:13	0x0	Data Scale
PME_STATUS	15	0x0	PME Status
B2_B3_SUPPORT (R)	22	0x0	Does not apply to PCI Express. Hardwired to 0.
BUS_PWR_EN (R)	23	0x0	Bus Power/Clock Control Enable. Does not apply to PCI Express. Hardwired to 0.
PMI_DATA (R)	31:24	0x0	Data

Power Management Status/Control Register

PCIE_CAP_LIST - R - 16 bits - pcieCfg0:0x58			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x10	Indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure. 10=PCI Express Capable
NEXT_PTR	15:8	0xa0	Next Capability Pointer -- The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.

The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 2.3 configuration space capability list.

PCIE_CAP - RW - 16 bits - pcieCfg0:0x5A			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	3:0	0x2	Indicates PCI-SIG defined PCI Express capability structure version number. 0=PCI Express Cap Version
DEVICE_TYPE (R)	7:4	0x4	Indicates the type of PCI Express logical device. 0=PCI Express Endpoint 1=Legacy PCI Express Endpoint 4=PCI Express Root Complex
SLOT_IMPLEMENTED	8	0x0	When set, indicates that the PCI Express Link associated with this Port is connected to a slot.
INT_MESSAGE_NUM (R)	13:9	0x0	Interrupt Message Number.

The PCI Express Capabilities register identifies PCI Express device type and associated capabilities.

DEVICE_CAP - RW - 32 bits - pcieCfg0:0x5C			
Field Name	**Bits**	**Default**	**Description**
MAX_PAYLOAD_SUPPORT (R)	2:0	0x0	Indicates the maximum payload size that the device can support for TLPs. 0=128 Byte
PHANTOM_FUNC (R)	4:3	0x0	Indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers with the Tag identifier. 0=No Phantom Functions
EXTENDED_TAG (R)	5	0x1	Indicates the maximum supported size of the Tag field as a Requester. 0=5-bit Tag supported 1=8-bit Tag supported
L0S_ACCEPTABLE_LATENCY (R)	8:6	0x0	Indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state.
L1_ACCEPTABLE_LATENCY (R)	11:9	0x0	Indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state.
ROLE_BASED_ERR_REPORTING (R)	15	0x0	Indicates the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification 1.0a. 0=Role-Based Error Reporting Disabled 1=Role-Based Error Reporting Enabled
CAPTURED_SLOT_POWER_LIMIT (R)	25:18	0x0	(Upstream ports only) In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.
CAPTURED_SLOT_POWER_SCALE (R)	27:26	0x0	Specifies the scale used for the Slot Power Limit Value.
FLR_CAPABLE (R)	28	0x0	Indicates that a device is capable of initiating Function Level Resets.

The Device Capabilities register identifies PCI Express device specific capabilities.

DEVICE_CNTL - RW - 16 bits - pcieCfg0:0x60			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_EN	0	0x0	Controls reporting of correctable errors. Default value of this field is 0. 0=Disable 1=Enable
NON_FATAL_ERR_EN	1	0x0	Controls reporting of Non-fatal errors. Default value of this field is 0. 0=Disable 1=Enable
FATAL_ERR_EN	2	0x0	Controls reporting of Fatal errors. Default value of this field is 0. 0=Disable 1=Enable
USR_REPORT_EN	3	0x0	Enables reporting of Unsupported Requests when set. Default value of this field is 0. 0=Disable 1=Enable
RELAXED_ORD_EN	4	0x1	If set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. Default value of this bit is 1. 0=Disable 1=Enable
MAX_PAYLOAD_SIZE (R)	7:5	0x0	Sets maximum TLP payload size for the device. Default value of this field is 000b. 0=128B size
EXTENDED_TAG_EN	8	0x0	When set, enables a device to use an 8-bit Tag field as a requester. If the bit is cleared, the device is restricted to a 5-bit Tag field. Default value of this field is 0. 0=Disable 1=Enable
PHANTOM_FUNC_EN (R)	9	0x0	When set, enables a device to use unclaimed functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is cleared, the device is not allowed to use Phantom Functions. 0=Disable 1=Enable
AUX_POWER_PM_EN (R)	10	0x0	When set, enables a device to draw AUX power independent of PME AUX power. 0=Disable 1=Enable
NO_SNOOP_EN	11	0x1	If set to 1, the device is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Default value of this bit is 1. 0=Disable 1=Enable
MAX_REQUEST_SIZE (R)	14:12	0x0	Sets the maximum Read Request size for the Device as a Requester. Default value of this field is 010b. 0=128B size
BRIDGE_CFG_RETRY_EN (R)	15	0x0	Enables PCI Express to PCI/PCI-X bridges to return Configuration Request Retry Status (CRS) in response to configuration requests that target devices below the bridge. 0=Disable 1=Enable

The Device Control register controls PCI Express device specific parameters.

DEVICE_STATUS - RW - 16 bits - pcieCfg0:0x62			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR	0	0x0	Indicates the status of correctable errors detected.
NON_FATAL_ERR	1	0x0	Indicates the status of Nonfatal errors detected.
FATAL_ERR	2	0x0	Indicates the status of Fatal errors detected.
USR_DETECTED	3	0x0	Indicates that the device received an Unsupported Request.
AUX_PWR	4	0x0	Devices that require AUX power report this bit as set if AUX power is detected by the device.
TRANSACTIONS_PEND (R)	5	0x0	Endpoints: This bit when set indicates that the device has issued Non-Posted Requests which have not been completed. Root and Switch Ports: This bit when set indicates that a port has issued Non-Posted Requests on its own behalf (using the port's own Requester ID) which have not been completed.

The Device Status register provides information about PCI Express device specific parameters.

LINK_CAP - RW - 32 bits - pcieCfg0:0x64			
Field Name	**Bits**	**Default**	**Description**
LINK_SPEED (R)	3:0	0x1	Indicates the maximum link speed of the given PCI Express link. 1=2.5 Gb/s 2=5.0 Gb/s
LINK_WIDTH (R)	9:4	0x0	Indicates the maximum width of the given PCI Express link. 1=x1 2=x2 4=x4 8=x8 12=x12 16=x16 32=x32
PM_SUPPORT (R)	11:10	0x3	Indicates the level of ASPM supported on the given PCI Express link.
L0S_EXIT_LATENCY (R)	14:12	0x1	Indicates the L0s exit latency for the given PCI Express link. The value reported indicates the length of time this port requires to complete transition from L0s to L0.
L1_EXIT_LATENCY (R)	17:15	0x2	Indicates the L0s exit latency for the given PCI Express link. The value reported indicates the length of time this port requires to complete transition from L0s to L0.
CLOCK_POWER_MANAGEMENT (R)	18	0x0	Indicates whether the component tolerates the removal of REFCLK via the CLKREQ# mechanism when the link is in L1 and L23 Ready.
SURPRISE_DOWN_ERR_REPORTING (R)	19	0x0	Indicates whether the component supports the detecting and reporting of a Surprise Down error condition.
DL_ACTIVE_REPORTING_CAPABLE (R)	20	0x0	Indicates whether the component supports the reporting of DL_Active state of the DLLSM.
LINK_BW_NOTIFICATION_CAP (R)	21	0x0	Indicates whether the component supports the Link Bandwidth Notification status and interrupt mechanisms.
PORT_NUMBER (R)	31:24	0x0	Indicates the PCI Express port number for the given PCI Express link.

The Link Capabilities register identifies PCI Express Link specific capabilities.

LINK_CNTL - RW - 16 bits - pcieCfg0:0x68			
Field Name	**Bits**	**Default**	**Description**
PM_CONTROL	1:0	0x0	Controls the level of ASPM supported on the given PCI Express link. Defined encodings are: 00b=Disabled 01b=L0s Entry Enabled 10b=L1 Entry Enabled 11b=L0s and L1 Entry Enabled
READ_CPL_BOUNDARY (R)	3	0x0	Read Completion Boundary. Indicates the RCB value for the root port 0=64 Byte 1=128 Byte
LINK_DIS	4	0x0	Disables the link when set to 1b. Default value is 0b.
RETRAIN_LINK (W)	5	0x0	A write of 1b to this bit initiates link retraining by directing the Physical Layer LTSSM to the Recovery state. Reads of this bit always return 0b.
COMMON_CLOCK_CFG	6	0x0	When set, indicates that this component and the component at the opposite end of this link are operating with a distributed common reference clock. Default value of this field is 0b.
EXTENDED_SYNC	7	0x0	When set, forces the transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set.
CLOCK_POWER_MANAGEMENT_EN	8	0x0	Determines if device is permitted to use CLKREQ# signal to power manage link clock.
HW_AUTONOMOUS_WIDTH_DISABLE	9	0x0	When set to 1, disables hardware from changing the link width for reasons other than attempting to correct unreliable link operation by reducing link width.
LINK_BW_MANAGEMENT_INT_EN	10	0x0	Enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set.
LINK_AUTONOMOUS_BW_INT_EN	11	0x0	Enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set.

The Link Control register controls PCI Express Link specific parameters.

LINK_STATUS - RW - 16 bits - pcieCfg0:0x6A			
Field Name	**Bits**	**Default**	**Description**
CURRENT_LINK_SPEED (R)	3:0	0x1	Indicates the negotiated link speed of the given PCI Express link 1=2.5 Gb/s 2=5.0 Gb/s
NEGOTIATED_LINK_WIDTH (R)	9:4	0x0	Indicates the negotiated width of the given PCI Express link. Defined encodings are: 1=x1 2=x2 4=x4 8=x8 12=x12 16=x16 32=x32 All other encodings are reserved.
LINK_TRAINING (R)	11	0x0	Indicates that Link Training is in progress (Physical Layer LTSSM in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link Training has not yet begun. Hardware clears this bit once Link training is complete.

LINK_STATUS - RW - 16 bits - pcieCfg0:0x6A			
Field Name	**Bits**	**Default**	**Description**
SLOT_CLOCK_CFG (R)	12	0x1	Indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared. 0=Different clock 1=Same clock
DL_ACTIVE (R)	13	0x0	Indicates the status of the Data Link Control and Management State Machine. It returns 1b to indicate DL_Active state, 0b otherwise.
LINK_BW_MANAGEMENT_STATUS	14	0x0	Set by hardware to indicate that either of the following has occurred without the port transitioning through DL_Down status: - A link retraining has completed following a write of 1b to the Retrain Link bit. - Hardware has changed the link speed or width to attempt to correct unreliable link operation, either through an LTSSM timeout or a higer level process.
LINK_AUTONOMOUS_BW_STATUS	15	0x0	Set by hardware to indicate that hardware has autonomously changed link speed or width, without the port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable link operation.

The Link Status register provides information about PCI Express Link specific parameters.

SLOT_CAP - RW - 32 bits - pcieCfg0:0x6C			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESENT	0	0x0	When set, indicates that an Attention Button is implemented on the chassis for this slot.
PWR_CONTROLLER_PRESENT	1	0x0	When set, indicates that a Power Controller is implemented for this slot.
MRL_SENSOR_PRESENT	2	0x0	When set, indicates that an Manually-operated Retention Latch Sensor is implemented on the chassis for this slot.
ATTN_INDICATOR_PRESENT	3	0x0	When set,,indicates that an Attention Indicator is implemented on the chassis for this slot.
PWR_INDICATOR_PRESENT	4	0x0	When set, indicates that a Power Indicator is implemented on the chassis for this slo
HOTPLUG_SURPRISE	5	0x0	When set, indicates that a device present in this slot might be removed from the system without any prior notification.
HOTPLUG_CAPABLE	6	0x0	When set, indicates that this slot is capable of supporting Hot-Plug operations.
SLOT_PWR_LIMIT_VALUE	14:7	0x0	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.
SLOT_PWR_LIMIT_SCALE	16:15	0x0	Specifies the scale used for the Slot Power Limit Value.
ELECTROMECH_INTERLOCK_PRESENT	17	0x0	When set, indicates that an Electromechanical Interlock is implemented on the chassis for this slot.
NO_COMMAND_COMPLETED_SUPPORTED	18	0x1	When set, indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller.
PHYSICAL_SLOT_NUM	31:19	0x0	This hardware initialized field indicates the physical slot number attached to this Port.

The Slot Capabilities register identifies PCI Express slot specific capabilities.

SLOT_CNTL - RW - 16 bits - pcieCfg0:0x70			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESSED_EN	0	0x0	When set, enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event.
PWR_FAULT_DETECTED_EN	1	0x0	When set, enables software notification on a power fault event.
MRL_SENSOR_CHANGED_EN	2	0x0	When set, enables software notification on a MRL sensor changes event.
PRESENCE_DETECT_CHANGED_EN	3	0x0	When set, enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event.
COMMAND_COMPLETED_INTR_EN	4	0x0	When set, enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug Controller.
HOTPLUG_INTR_EN	5	0x0	When set, enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
ATTN_INDICATOR_CNTL	7:6	0x0	Reads to this field return the current state of the Attention Indicator; writes to this field set the Attention Indicator.
PWR_INDICATOR_CNTL	9:8	0x0	Reads to this field return the current state of the Power Indicator; writes to this field set the Power Indicator.
PWR_CONTROLLER_CNTL	10	0x0	When read, this field returns the current state of the Power applied to the slot; when written, sets the power state of the slot per the defined encodings.
ELECTROMECH_INTERLOCK_CNTL	11	0x0	If an electromechanical interlock is implemented, a write of 1b causes the state of the interlock to toggle.
DL_STATE_CHANGED_EN	12	0x0	If the Data Link Layer Link Active Capability is implemented, this bit when set enables software notification when Data Link Layer Link Active Reporting bit is changed.

The Slot Control register controls PCI Express Slot specific parameters.

SLOT_STATUS - RW - 16 bits - pcieCfg0:0x72			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESSED	0	0x0	This bit is set when the attention button is pressed.
PWR_FAULT_DETECTED	1	0x0	This bit is set when the power controller detected a power fault at this slot.
MRL_SENSOR_CHANGED	2	0x0	This bit is set when a MRL sensor state change is detected.
PRESENCE_DETECT_CHANGED	3	0x0	This bit is set when the value reported in the Presence Detect State bit is changed.
COMMAND_COMPLETED	4	0x0	This bit is set when the Hot-Plug Controller completes an issued command.
MRL_SENSOR_STATE (R)	5	0x0	Reports the status of the MRL sensor.
PRESENCE_DETECT_STATE (R)	6	0x0	Indicates the presence of an adapter in the slot.
ELECTROMECH_INTERLOCK_STATUS (R)	7	0x0	Indicates the status of the Electromechanical Interlock.
DL_STATE_CHANGED	8	0x0	This bit is set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed.

The Slot Status register provides information about PCI Express Slot specific parameters.

ROOT_CNTL - RW - 16 bits - pcieCfg0:0x74			
Field Name	**Bits**	**Default**	**Description**
SERR_ON_CORR_ERR_EN	0	0x0	System Error on Correctable Error Enable -- If set, indicates that a System Error should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_NONFATAL_ERR_EN	1	0x0	System Error on Non-Fatal Error Enable -- If set, indicates that a System Error should be generated if a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_FATAL_ERR_EN	2	0x0	System Error on Fatal Error Enable -- If set, indicates that a System Error should be generated if a Fatal error is reported by any of the devices in the hierarchy associated with this root port.
PM_INTERRUPT_EN	3	0x0	PME Interrupt Enable -- When set, enables interrupt generation upon receipt of a PME message.
CRS_SOFTWARE_VISIBILITY_EN	4	0x0	When set, enables the root port to return Configuration Request Retry Status Completion Status to software.

The Root Control register controls PCI Express Root Complex specific parameters.

ROOT_CAP - RW - 16 bits - pcieCfg0:0x76			
Field Name	**Bits**	**Default**	**Description**
CRS_SOFTWARE_VISIBILITY (R)	0	0x1	Indicates the root port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software.

The Root Capabilities register identifies PCI Express Root Complex specific capabilities.

ROOT_STATUS - RW - 32 bits - pcieCfg0:0x78			
Field Name	**Bits**	**Default**	**Description**
PME_REQUESTOR_ID (R)	15:0	0x0	Indicates the PCI requestor ID of the last PME requestor.
PME_STATUS	16	0x0	Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field.
PME_PENDING (R)	17	0x0	Indicates that another PME is pending when the PME Status bit is set.

The Root Status register provides information about PCI Express device specific parameters.

DEVICE_CAP2 - RW - 32 bits - pcieCfg0:0x7C			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_RANGE_SUPPORTED (R)	3:0	0x0	PCIE completion timeout range supported
CPL_TIMEOUT_DIS_SUPPORTED (R)	4	0x0	PCIE completion timeout disabled supported
ARI_FORWARDING_SUPPORTED (R)	5	0x0	ARI forwarding supported

The Device Capabilities 2 register identifies PCI Express device specific capabilities.

DEVICE_CNTL2 - RW - 16 bits - pcieCfg0:0x80			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_VALUE	3:0	0x0	PCIe completion timeout value
CPL_TIMEOUT_DIS	4	0x0	Disable PCIe completion timeout
ARI_FORWARDING_EN	5	0x0	ARI forwarding enable

The Device Control 2 register controls PCI Express device specific parameters.

DEVICE_STATUS2 - RW - 16 bits – pcieCfg0:0x82			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	Reserved

The Device Status 2 register provides information about PCI Express device specific parameters.

LINK_CAP2 - RW - 32 bits - pcieCfg0:0x84			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	Reserved

The Link Capabilities 2 register identifies PCI Express Link specific capabilities.

LINK_CNTL2 - RW - 16 bits - pcieCfg0:0x88			
Field Name	**Bits**	**Default**	**Description**
TARGET_LINK_SPEED	3:0	0x1	The upper limit on the operational speed. This field restricts the data rate values advertised by an upstream component.
ENTER_COMPLIANCE	4	0x0	Forces a port's transmitter to enter Compliance.
HW_AUTONOMOUS_SPEED_DISABLE	5	0x0	Controls the component's ability to autonomously direct changes in link speed.
SELECTABLE_DEEMPHASIS (R)	6	0x0	Selectable de-emphasis (in GEN 2 data rate) 0= -6dB 1= -3.6dB
XMIT_MARGIN	9:7	0x0	Controls the value of the non-deemphasized voltage level at the transmitter pins.
ENTER_MOD_COMPLIANCE	10	0x0	LTSSM transmits modified compliance pattern in Polling.Compliance if this bit is set to 1.
COMPLIANCE_SOS	11	0x0	When set to 1, the LTSSM is required to send SOS perioldically in between the (modified) compliance patterns.
COMPLIANCE_DEEMPHASIS	12	0x0	Sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the `enter compliance' bit being 1b. When the link is operating at 2.5 GT/s, the setting of this bit has no effect. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. 0=-6 dB 1=-3dB

The Link Control 2 register controls PCI Express Link specific parameters.

LINK_STATUS2 - RW - 16 bits - pcieCfg0:0x8A			
Field Name	**Bits**	**Default**	**Description**
CUR_DEEMPHASIS_LEVEL (R)	0	0x0	When the link is operating at 5GT/s speed, this bit reflects the level of de-emphasis.

The Link Status 2 register provides information about PCI Express Link specific parameters.

SLOT_CAP2 - RW - 32 bits - pcieCfg0:0x8C			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	Reserved

The Slot Capabilities 2 register identifies PCI Express slot specific capabilities.

SLOT_CNTL2 - RW - 16 bits - pcieCfg0:0x90			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	Reserved

The Slot Control 2 register controls PCI Express Slot specific parameters.

SLOT_STATUS2 - RW - 16 bits - pcieCfg0:0x92			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	Reserved

The Slot Status 2 register provides information about PCI Express Slot specific parameters.

MSI_CAP_LIST - R - 16 bits - pcieCfg0:0xA0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x5	Identifies whether a device function is MSI capable.
NEXT_PTR	15:8	0xb0	Pointer to the next item on the capabilities list.

Message Signaled Interrupt Capability Registers

MSI_MSG_CNTL - RW - 16 bits - pcieCfg0:0xA2			
Field Name	**Bits**	**Default**	**Description**
MSI_EN	0	0x0	Enable MSI messaging 0=Disable 1=Enable
MSI_MULTI_CAP (R)	3:1	0x0	Multiple Message Capable. Determines the number of requested messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_MULTI_EN	6:4	0x0	Multiple Message Enable. Written to to indicate the number of allocated messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_64BIT (R)	7	0x0	Indicates whether a device function is capable of generating a 64-bit message address. 0=Not capable of generating 1 64-bit message address 1=Capable of generating 1 64-bit message address

Message Signaled Interrupts Control Register

MSI_MSG_ADDR_LO - RW - 32 bits - pcieCfg0:0xA4			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_LO	31:2	0x0	Message Lower Address - use lower 32-bits of address

Message Lower Address

MSI_MSG_ADDR_HI - RW - 32 bits - pcieCfg0:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_HI	31:0	0x0	Message Upper Address - use upper 32-bit of address

Message Upper Address

MSI_MSG_DATA_64 - RW - 16 bits - pcieCfg0:0xAC			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA_64	15:0	0x0	Message Data. System specified.

64-bit MSI Message Data

MSI_MSG_DATA - RW - 32 bits - pcieCfg0:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA	15:0	0x0	Message Data. System specified.

MSI Message Data

SSID_CAP_LIST - R - 32 bits - pcieCfg0:0xB0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0xd	Capability ID
NEXT_PTR	15:8	0xb8	Pointer to next capability register

Subsystem ID Capability List

SSID_ID - R - 32 bits - pcieCfg0:0xB4			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x1022	Subsystem Vendor ID
SUBSYSTEM_ID	31:16	0x0	Subsystem ID

Subsystem ID

MSI_MAP_CAP_LIST - R - 32 bits - pcieCfg0:0xB8			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x8	Identifies this as a HyperTransport capability list item.
NEXT_PTR (R)	15:8	0x0	Pointer to the next item in the capabilities list. Must be NULL for the final item in the list. This field is read only.
EN	16	0x1	Indicates whether the mapping is active.
FIXD	17	0x1	Indicates whether the programming address is fixed.
CAP_TYPE	31:27	0x15	Indicates this as the MSI Mapping Capability block.

MSI Mapping Capability Register

PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x100			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xb	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x110	Contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Vendor Specific Capability

PCIE_VENDOR_SPECIFIC_HDR - R - 32 bits - pcieCfg0:0x104			
Field Name	**Bits**	**Default**	**Description**
VSEC_ID	15:0	0x1	Vendor-defined ID number.
VSEC_REV	19:16	0x1	Vendor-defined revision number.
VSEC_LENGTH	31:20	0x10	Number of bytes in the entire VSEC structure.

Vendor Specific Header

PCIE_VENDOR_SPECIFIC1 - RW - 32 bits - pcieCfg0:0x108			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCIe scratch register.

Vendor-Specific Scratch Register 1

PCIE_VENDOR_SPECIFIC2 - RW - 32 bits - pcieCfg0:0x10C			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCIe scratch register.

Vendor-Specific Scratch Register 2

PCIE_VC_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x110			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x2	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x140	Contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Virtual Channel Enhanced Capability Header

PCIE_PORT_VC_CAP_REG1 - R - 32 bits - pcieCfg0:0x114			
Field Name	**Bits**	**Default**	**Description**
EXT_VC_COUNT	2:0	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. This field is valid for all devices.
LOW_PRIORITY_EXT_VC_COUNT	6:4	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC group.
REF_CLK	9:8	0x0	Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration.
PORT_ARB_TABLE_ENTRY_SIZE	11:10	0x0	Indicates the size (in bits) of Port Arbitration table entry in the device.

Port VC Capability Register 1

PCIE_PORT_VC_CAP_REG2 - R - 32 bits - pcieCfg0:0x118			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_CAP	7:0	0x0	Indicates the types of VC Arbitration supported by the device for the Low Priority Virtual Channel group.
VC_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the VC Arbitration Table.

Port VC Capability Register 2

PCIE_PORT_VC_CNTL - RW - 16 bits - pcieCfg0:0x11C			
Field Name	**Bits**	**Default**	**Description**
LOAD_VC_ARB_TABLE (R)	0	0x0	Used for software to update the VC Arbitration Table.
VC_ARB_SELECT	3:1	0x0	Used for software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes.

Port VC Control Register

PCIE_PORT_VC_STATUS - R - 16 bits - pcieCfg0:0x11E			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the VC Arbitration Table

Port VC Status Register

PCIE_VC0_RESOURCE_CAP - R - 32 bits - pcieCfg0:0x120			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC.
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting.
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.

VC0 Resource Capability Register

PCIE_VC0_RESOURCE_CNTL - RW - 32 bits - pcieCfg0:0x124			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x1	Indicates the TCs that are mapped to the VC resource.
TC_VC_MAP_TC1_7	7:1	0x7f	Indicates the TCs that are mapped to the VC resource.
LOAD_PORT_ARB_TABLE (R)	16	0x0	When set, updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.

PCIE_VC0_RESOURCE_CNTL - RW - 32 bits - pcieCfg0:0x124			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_SELECT	19:17	0x0	Configures the VC resource to provide a particular Port Arbitration service.
VC_ID (R)	26:24	0x0	Assigns a VC ID to the VC resource.
VC_ENABLE (R)	31	0x1	When set, enables a Virtual Channel.

VC0 Resource Control Register

PCIE_VC0_RESOURCE_STATUS - R - 16 bits - pcieCfg0:0x12A			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the Port Arbitration Table associated with the VC resource.
VC_NEGOTIATION_PENDING	1	0x1	Indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state.

VC0 Resource Status Register

PCIE_VC1_RESOURCE_CAP - R - 32 bits - pcieCfg0:0x12C			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC.
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting.
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.

VC1 Resource Capability Register

PCIE_VC1_RESOURCE_CNTL - RW - 32 bits - pcieCfg0:0x130			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x0	Indicates the TCs that are mapped to the VC resource.
TC_VC_MAP_TC1_7	7:1	0x0	Indicates the TCs that are mapped to the VC resource.
LOAD_PORT_ARB_TABLE (R)	16	0x0	When set, updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	Configures the VC resource to provide a particular Port Arbitration service.
VC_ID	26:24	0x0	Assigns a VC ID to the VC resource.
VC_ENABLE	31	0x0	When set, enables a Virtual Channel.

VC1 Resource Control Register

PCIE_VC1_RESOURCE_STATUS - R - 16 bits - pcieCfg0:0x136			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the Port Arbitration Table associated with the VC resource.
VC_NEGOTIATION_PENDING	1	0x1	Indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state.

VC1 Resource Status Register

PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x140			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x3	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x150	Contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Device Serial Number Enhanced Capability header

PCIE_DEV_SERIAL_NUM_DW1 - R - 32 bits - pcieCfg0:0x144			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_LO	31:0	0x0	Lower 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)

PCI-Express Device Serial Number (1st DW)

PCIE_DEV_SERIAL_NUM_DW2 - R - 32 bits - pcieCfg0:0x148			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_HI	31:0	0x0	Upper 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)

PCI-Express Device Serial Number (2nd DW)

PCIE_ADV_ERR_RPT_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x150			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x1	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x190	Contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Advanced Error Reporting Enhanced Capability header

PCIE_UNCORR_ERR_STATUS - RW - 32 bits - pcieCfg0:0x154			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_STATUS	4	0x0	Data Link Protocol Error Status
SURPDN_ERR_STATUS (R)	5	0x0	Surprise Down Error Status
PSN_ERR_STATUS	12	0x0	Poisoned TLP Status
FC_ERR_STATUS (R)	13	0x0	Flow Control Protocol Error Status
CPL_TIMEOUT_STATUS	14	0x0	Completion Timeout Status
CPL_ABORT_ERR_STATUS	15	0x0	Completer Abort Status
UNEXP_CPL_STATUS	16	0x0	Unexpected Completion Status
RCV_OVFL_STATUS (R)	17	0x0	Receiver Overflow Status
MAL_TLP_STATUS	18	0x0	Malformed TLP Status
ECRC_ERR_STATUS	19	0x0	ECRC Error Status
UNSUPP_REQ_ERR_STATUS	20	0x0	Unsupported Request Error Status
ACS_VIOLATION_STATUS	21	0x0	ACS Violation Error Status

The Uncorrectable Error Status register reports error status of individual error sources on a PCI Express device.

PCIE_UNCORR_ERR_MASK - RW - 32 bits - pcieCfg0:0x158			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_MASK	4	0x0	Data Link Protocol Error Mask
SURPDN_ERR_MASK (R)	5	0x0	Surprise Down Error Mask
PSN_ERR_MASK	12	0x0	Poisoned TLP Mask
FC_ERR_MASK (R)	13	0x0	Flow Control Protocol Error Mask
CPL_TIMEOUT_MASK	14	0x0	Completion Timeout Mask
CPL_ABORT_ERR_MASK	15	0x0	Completer Abort Mask
UNEXP_CPL_MASK	16	0x0	Unexpected Completion Mask
RCV_OVFL_MASK (R)	17	0x0	Receiver Overflow Mask
MAL_TLP_MASK	18	0x0	Malformed TLP Mask
ECRC_ERR_MASK	19	0x0	ECRC Error Mask
UNSUPP_REQ_ERR_MASK	20	0x0	Unsupported Request Error Mask
ACS_VIOLATION_MASK	21	0x0	ACS Violation Mask

The Uncorrectable Error Mask register controls reporting of individual errors by the device to the PCI Express Root Complex via a PCI Express error Message.

PCIE_UNCORR_ERR_SEVERITY - RW - 32 bits - pcieCfg0:0x15C			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_SEVERITY	4	0x1	Data Link Protocol Error Severity
SURPDN_ERR_SEVERITY (R)	5	0x1	Surprise Down Error Severity
PSN_ERR_SEVERITY	12	0x0	Poisoned TLP Severity
FC_ERR_SEVERITY (R)	13	0x1	Flow Control Protocol Error Severity
CPL_TIMEOUT_SEVERITY	14	0x0	Completion Timeout Error Severity

PCIE_UNCORR_ERR_SEVERITY - RW - 32 bits - pcieCfg0:0x15C			
Field Name	**Bits**	**Default**	**Description**
CPL_ABORT_ERR_SEVERITY	15	0x0	Completer Abort Error Severity
UNEXP_CPL_SEVERITY	16	0x0	Unexpected Completion Error Severity
RCV_OVFL_SEVERITY (R)	17	0x1	Receiver Overflow Error Severity
MAL_TLP_SEVERITY	18	0x1	Malformed TLP Severity
ECRC_ERR_SEVERITY	19	0x0	ECRC Error Severity
UNSUPP_REQ_ERR_SEVERITY	20	0x0	Unsupported Request Error Severity
ACS_VIOLATION_SEVERITY	21	0x0	ACS Violation Severity

The Uncorrectable Error Severity register controls whether an individual error is reported as a Nonfatal or Fatal error.

PCIE_CORR_ERR_STATUS - RW - 32 bits - pcieCfg0:0x160			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_STATUS (R)	0	0x0	Receiver Error Status
BAD_TLP_STATUS	6	0x0	Bad TLP Status
BAD_DLLP_STATUS	7	0x0	Bad DLLP Status
REPLAY_NUM_ROLLOVER_STATUS	8	0x0	REPLAY_NUM Rollover Status
REPLAY_TIMER_TIMEOUT_STATUS	12	0x0	Replay Timer Timeout Status
ADVISORY_NONFATAL_ERR_STATUS	13	0x0	Advisory Non-Fatal Status

The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device.

PCIE_CORR_ERR_MASK - RW - 32 bits - pcieCfg0:0x164			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_MASK (R)	0	0x0	Receiver Error Mask
BAD_TLP_MASK	6	0x0	Bad TLP Mask
BAD_DLLP_MASK	7	0x0	Bad DLLP Mask
REPLAY_NUM_ROLLOVER_MASK	8	0x0	REPLAY_NUM Rollover Mask
REPLAY_TIMER_TIMEOUT_MASK	12	0x0	Replay Timer Timeout Mask
ADVISORY_NONFATAL_ERR_MASK	13	0x1	Advisory Non-Fatal Mask

The Correctable Error Mask register controls reporting of individual correctable errors by device to the PCI Express Root Complex via a PCI Express error Message.

PCIE_ADV_ERR_CAP_CNTL - RW - 32 bits - pcieCfg0:0x168			
Field Name	**Bits**	**Default**	**Description**
FIRST_ERR_PTR (R)	4:0	0x0	Identifies the bit position of the first error reported in the Uncorrectable Error Status register.
ECRC_GEN_CAP (R)	5	0x0	Indicates that the device is capable of generating ECRC.
ECRC_GEN_EN	6	0x0	When set, enables ECRC generation. Default value of this field is 0.
ECRC_CHECK_CAP (R)	7	0x0	Indicates that the device is capable of checking ECRC.
ECRC_CHECK_EN	8	0x0	When set, enables ECRC checking. Default value of this field is 0.

Advanced Error Capabilities and Control Register

PCIE_HDR_LOG0 - R - 32 bits - pcieCfg0:0x16C			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 1st DW

Header Log Register captures the Header for the TLP corresponding to a detected error;

PCIE_HDR_LOG1 - R - 32 bits - pcieCfg0:0x170			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 2nd DW

Header Log Register

PCIE_HDR_LOG2 - R - 32 bits – pcieCfg0:0x174			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 3rd DW

Header Log Register

PCIE_HDR_LOG3 - R - 32 bits – pcieCfg0:0x178			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 4th DW

Header Log Register

PCIE_ROOT_ERR_CMD - RW - 32 bits - pcieCfg0:0x17C			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_REP_EN	0	0x0	Correctable Error Reporting Enable -- When set, enables the generation of an interrupt when a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.
NONFATAL_ERR_REP_EN	1	0x0	Non-Fatal Error Reporting Enable -- When set, enables the generation of an interrupt when a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
FATAL_ERR_REP_EN	2	0x0	Fatal Error Reporting Enable -- When set, enables the generation of an interrupt when a Fatal error is reported by any of the devices in the hierarchy associated with this Root Port.

Root Error Command Register

PCIE_ROOT_ERR_STATUS - RW - 32 bits - pcieCfg0:0x180			
Field Name	**Bits**	**Default**	**Description**
ERR_CORR_RCVD	0	0x0	Set when a correctable error message is received and this bit is not already set. Default value of this field is 0.
MULT_ERR_CORR_RCVD	1	0x0	Set when a correctable error Message is received and ERR_COR Received is already set. Default value of this field is 0.
ERR_FATAL_NONFATAL_RCVD	2	0x0	Set when either a Fatal or a Non-fatal error message is received and this bit is not already set. Default value of this field is 0.
MULT_ERR_FATAL_NONFATAL_RCVD	3	0x0	Set when either a Fatal or a Non-fatal error is received and ERR_FATAL/NONFATAL Received is already set. Default value of this field is 0.
FIRST_UNCORRECTABLE_FATAL	4	0x0	Set to 1b when the first Uncorrectable error message received is for a Fatal error. Default value of this field is 0.
NONFATAL_ERROR_MSG_RCVD	5	0x0	Set to 1b when one or more Non-Fatal Uncorrectable error messages have been received. Default value of this field is 0.
FATAL_ERROR_MSG_RCVD	6	0x0	Set to 1b when one or more Fatal Uncorrectable error messages have been received. Default value of this field is 0.
ADV_ERR_INT_MSG_NUM (R)	31:27	0x0	Advanced Error Interrupt Message Number

Root Error Status Register

PCIE_ERR_SRC_ID - RW - 32 bits - pcieCfg0:0x184			
Field Name	**Bits**	**Default**	**Description**
ERR_COR_SRC_ID (R)	15:0	0x0	Loaded with the Requestor ID indicated in the received ERR_COR message when the ERR_COR Received register is not already set. Default value of this field is 0.
ERR_FATAL_NONFATAL_SRC_ID (R)	31:16	0x0	Loaded with the Requestor ID indicated in the received ERR_FATAL or ERR_NONFATAL Message when the ERR_FATAL/NONFATAL Received register is not already set. Default value of this field is 0.

The Error Source Identification register identifies the source (Requestor ID) of first correctable and uncorrectable (Non-fatal/Fatal) errors reported in the Root Error Status register.

PCIE_ACS_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x190			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xd	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x0	Contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

ACS Enhanced Capability header

PCIE_ACS_CAP - R - 16 bits - pcieCfg0:0x194			
Field Name	**Bits**	**Default**	**Description**
SOURCE_VALIDATION	0	0x0	When set, indicates that the component implements ACS Source Validation.
TRANSLATION_BLOCKING	1	0x0	When set, indicates that the component implements ACS Translation Blocking.
P2P_REQUEST_REDIRECT	2	0x0	When set, indicates that the component implements ACS P2P Request Redirect.
P2P_COMPLETION_REDIRECT	3	0x0	When set, indicates that the component implements ACS P2P Completion Redirect.
UPSTREAM_FORWARDING	4	0x0	When set, indicates that the component implements ACS Upstream Forwarding.
P2P_EGRESS_CONTROL	5	0x0	When set, indicates that the component implements ACS P2P Egress Control.
DIRECT_TRANSLATED_P2P	6	0x0	When set, indicates that the component implements ACS Direct Translated P2P.
EGRESS_CONTROL_VECTOR_SIZE	15:8	0x0	Encodings 01h-FFh directly indicate the number of applicable bits in the Egress Control Vector; the encoding 00h indicates 256 bits.

ACS Capability register

PCIE_ACS_CNTL - RW - 16 bits - pcieCfg0:0x196			
Field Name	**Bits**	**Default**	**Description**
SOURCE_VALIDATION_EN	0	0x0	When set, the component validates the Bus Number from the Requester ID of Upstream Requests against the secondary / subordinate bus numbers.
TRANSLATION_BLOCKING_EN	1	0x0	When set, the component blocks all Upstream Memory Requests whose Address Translation field is not set to the default value.
P2P_REQUEST_REDIRECT_EN	2	0x0	In conjunction with ACS P2P Egress Control and ACS Direct Translated P2P mechanisms, determines when the component redirects P2P Requests Upstream.
P2P_COMPLETION_REDIRECT_EN	3	0x0	Determines when the component redirects P2P Completions Upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is cleared.
UPSTREAM_FORWARDING_EN	4	0x0	When set, the component forwards Upstream any Request or Completion TLPs it receives that were redirected Upstream by a component lower in the hierarchy.

PCIE_ACS_CNTL - RW - 16 bits - pcieCfg0:0x196			
Field Name	**Bits**	**Default**	**Description**
P2P_EGRESS_CONTROL_EN (R)	5	0x0	In conjunction with the Egress Control Vector plus the ACS P2P Request Redirect and ACS Direct Translated P2P mechanisms, determines when to allow, disallow, or redirect P2P requests.
DIRECT_TRANSLATED_P2P_EN	6	0x0	When set, overrides the ACS P2P Request Redirect and ACS P2P Egress Control mechanisms with P2P Memory Requests whose Address Translation field indicates a Translated address.

ACS Control register

Chapter 6
VGA Registers

6.1 VGA Register Descriptions

The logic within FCH contains only the logic to perform DP to VGA translation. These registers are normally accessed by the graphic driver via the AUX channel. For debugging purpose, software can access these registers through FCH's MMIO at offset 0x1400:0x14FF.

Register Name	Offset Address
DPCD_DPCD_REV	DPCD_VGA:0x0
DPCD_MAX_LINK_RATE	DPCD_VGA:0x1
DPCD_MAX_LANE_COUNT	DPCD_VGA:0x2
DPCD_MAX_DOWNSPREAD	DPCD_VGA:0x3
DPCD_NORP	DPCD_VGA:0x4
DPCD_DOWNSTREAMPORT_PRESENT	DPCD_VGA:0x5
DPCD_MAIN_LINK_CHANNEL_CODING	DPCD_VGA:0x6
DPCD_DOWN_STREAM_PORT_COUNT	DPCD_VGA:0x7
DPCD_RECEIVE_PORT0_CAP_0	DPCD_VGA:0x8
DPCD_RECEIVE_PORT0_CAP_1	DPCD_VGA:0x9
DPCD_DWN_STRM_PORT0_CAP_0	DPCD_VGA:0x80
DPCD_LINK_BW_SET	DPCD_VGA:0x100
DPCD_LANE_COUNT_SET	DPCD_VGA:0x101
DPCD_TRAINING_PATTERN_SET	DPCD_VGA:0x102
DPCD_TRAINING_LANE0_SET	DPCD_VGA:0x103
DPCD_TRAINING_LANE1_SET	DPCD_VGA:0x104
DPCD_TRAINING_LANE2_SET	DPCD_VGA:0x105
DPCD_TRAINING_LANE3_SET	DPCD_VGA:0x106
DPCD_DOWNSPREAD_CTRL	DPCD_VGA:0x107
DPCD_MAIN_LINK_CHANNEL_CODING_SET	DPCD_VGA:0x108
DPCD_SINK_COUNT	DPCD_VGA:0x200
DPCD_DEVICE_SERVICE_IRQ_VECTOR	DPCD_VGA:0x201
DPCD_LANE0_1_STATUS	DPCD_VGA:0x202
DPCD_LANE2_3_STATUS	DPCD_VGA:0x203
DPCD_LANE_ALIGN_STATUS_UPDATED	DPCD_VGA:0x204
DPCD_SINK_STATUS	DPCD_VGA:0x205
DPCD_ADJUST_REQUEST_LANE0_1	DPCD_VGA:0x206
DPCD_ADJUST_REQUEST_LANE2_3	DPCD_VGA:0x207
DPCD_TRAINING_SCORE_LANE0	DPCD_VGA:0x208
DPCD_TRAINING_SCORE_LANE1	DPCD_VGA:0x209
DPCD_TRAINING_SCORE_LANE2	DPCD_VGA:0x20A
DPCD_TRAINING_SCORE_LANE3	DPCD_VGA:0x20B
DPCD_SYMBOL_ERROR_COUNT_LANE0	DPCD_VGA:0x210
DPCD_SYMBOL_ERROR_COUNT_LANE1	DPCD_VGA:0x212
DPCD_SYMBOL_ERROR_COUNT_LANE2	DPCD_VGA:0x214
DPCD_SYMBOL_ERROR_COUNT_LANE3	DPCD_VGA:0x216
DPCD_TEST_CRC_R_CR	DPCD_VGA:0x240
DPCD_TEST_CRC_G_Y	DPCD_VGA:0x242

Register Name	Offset Address
DPCD_TEST_CRC_B_CB	DPCD_VGA:0x244
DPCD_TEST_SINK_MISC	DPCD_VGA:0x246
DPCD_TEST_SINK	DPCD_VGA:0x270
DPCD_SRC_IEEE_OUI	DPCD_VGA:0x300
DPCD_BRANCH_IEEE_OUI	DPCD_VGA:0x500
DPCD_BRANCH_CHIPID0	DPCD_VGA:0x503
DPCD_BRANCH_CHIPID1	DPCD_VGA:0x504
DPCD_BRANCH_CHIPID2	DPCD_VGA:0x505
DPCD_BRANCH_CHIPID3	DPCD_VGA:0x506
DPCD_BRANCH_CHIPID4	DPCD_VGA:0x507
DPCD_BRANCH_CHIPID5	DPCD_VGA:0x508
DPCD_BRANCH_REV	DPCD_VGA:0x509
DPCD_BRANCH_SW_MAJ_REV	DPCD_VGA:0x50A
DPCD_BRANCH_SW_MIN_REV	DPCD_VGA:0x50B
DPCD_DPRL_LANESETUP0	DPCD_VGA:0x510
DPCD_DPRL_LANESETUP1	DPCD_VGA:0x511
DPCD_DPRL_IRQ_SERVICE	DPCD_VGA:0x512
DPCD_DPRL_IRQ_EN	DPCD_VGA:0x513
DPCD_DPRL_IRQ_GLOBEN	DPCD_VGA:0x514
DPCD_DPRL_INTIRQ_SERVICE	DPCD_VGA:0x516
DPCD_DPRL_INTIRQ_EN	DPCD_VGA:0x518
DPCD_DPRL_IRQ_TIMEOUT	DPCD_VGA:0x51C
DPCD_DPRL_IRQ_HPDTIME	DPCD_VGA:0x520
DPCD_DPRL_DEBUG	DPCD_VGA:0x523
DPCD_DPRL_PRBS23	DPCD_VGA:0x525
DPCD_DPRL_DEBUG_OUT	DPCD_VGA:0x528
DPCD_DPRL_CR_THRESH	DPCD_VGA:0x580
DPCD_DPRL_EQ_THRESH	DPCD_VGA:0x581
DPCD_DPRL_LFSRADV	DPCD_VGA:0x582
DPCD_DPRL_RFCHAL	DPCD_VGA:0x584
DPCD_DPRL_RFRESP	DPCD_VGA:0x588
DPCD_DPRL_RFCTRL	DPCD_VGA:0x58C
DPCD_DPRL_RFSTAT	DPCD_VGA:0x58D
DPCD_SET_POWER	DPCD_VGA:0x600
PCIERXVGAC_RX0_STATUS1	DPCD_VGA:0x80000
PCIERXVGAC_RX1_STATUS1	DPCD_VGA:0x80100
PCIERXVGAC_RX2_STATUS1	DPCD_VGA:0x80200
PCIERXVGAC_RX3_STATUS1	DPCD_VGA:0x80300
PCIERXVGAC_RX0_CONTROL1	DPCD_VGA:0x80004
PCIERXVGAC_RX1_CONTROL1	DPCD_VGA:0x80104
PCIERXVGAC_RX2_CONTROL1	DPCD_VGA:0x80204
PCIERXVGAC_RX3_CONTROL1	DPCD_VGA:0x80304
PCIERXVGAC_RX0_CONTROL2	DPCD_VGA:0x80008
PCIERXVGAC_RX1_CONTROL2	DPCD_VGA:0x80108
PCIERXVGAC_RX2_CONTROL2	DPCD_VGA:0x80208
PCIERXVGAC_RX3_CONTROL2	DPCD_VGA:0x80308
PCIERXVGAC_RX0_ARESET	DPCD_VGA:0x80010
PCIERXVGAC_RX1_ARESET	DPCD_VGA:0x80110
PCIERXVGAC_RX2_ARESET	DPCD_VGA:0x80210
PCIERXVGAC_RX3_ARESET	DPCD_VGA:0x80310

Register Name	Offset Address
PCIERXVGAC_RX_CLK_CONTROL	DPCD_VGA:0x80400
PCIERXPLL_MACRO_STATUS1	DPCD_VGA:0x81000
PCIERXPLL_MACRO_CONTROL1	DPCD_VGA:0x81004
PCIERXPLL_MACRO_CONTROL2	DPCD_VGA:0x81008
PCIERXPLL_MACRO_CONTROL3	DPCD_VGA:0x8100C
PCIERXPLL_PDNB_CONTROL	DPCD_VGA:0x81104
PCIERXPLL_RESET	DPCD_VGA:0x81108
PCIERXPLL_LOCK_CTRL	DPCD_VGA:0x8110C
PCIERXPLL_DEBUG1	DPCD_VGA:0x81230
PCIERXPLL_DEBUG2	DPCD_VGA:0x81234
PCIERXPLL_BIST_CH_EN	DPCD_VGA:0x81238
PCIERXPLL_BIST_MODE	DPCD_VGA:0x81239
PCIERXPLL_BIST_OVERRIDE_CRCTRL	DPCD_VGA:0x8123A
PCIERXPLL_BIST_DEBUG_SEL	DPCD_VGA:0x8123B
PCIERXPLL_BIST_LOOPDBG_SEL	DPCD_VGA:0x8123C
PCIERXPLL_BIST_CRCTRL_VAL	DPCD_VGA:0x8123D
PCIERXPLL_BIST_PHASEOUT_SEL	DPCD_VGA:0x8123E
PCIERXPLL_BIST_NCYCLE	DPCD_VGA:0x8123F
PCIERXPLL_BIST_DPHASE	DPCD_VGA:0x81240
PCIERXPLL_BIST_TEST	DPCD_VGA:0x81241
PCIERXPLL_BIST_ENABLE	DPCD_VGA:0x81242
PCIERXPLL_BIST_REGCTL	DPCD_VGA:0x81243
PCIERXPLL_BIST_DATA	DPCD_VGA:0x81244
PCIERXPLL_BIST_DBG	DPCD_VGA:0x81246
PCIERXPLL_P_B1X_CLK_DIV_CTRL	DPCD_VGA:0x81254
PCIERXPLL_IMPCTRL	DPCD_VGA:0x81260
PCIERXPLL_IMPVAL_STATUS	DPCD_VGA:0x81264
PCIERXPLL_PM_DBG_SEL	DPCD_VGA:0x81268
control	DPCD_VGA:0x82000
alpha_denom_exp	DPCD_VGA:0x82004
noadjust_line_threshold	DPCD_VGA:0x82008
getmaxlevel_cycles	DPCD_VGA:0x8200C
fifo_level	DPCD_VGA:0x82014
adjust	DPCD_VGA:0x8201C
locking_control	DPCD_VGA:0x82020
lock_count	DPCD_VGA:0x82024
overflow_count	DPCD_VGA:0x82028
underflow_count	DPCD_VGA:0x8202C
average_fifo_level	DPCD_VGA:0x82030
lock_count_threshold	DPCD_VGA:0x82034
irq_raw_status	DPCD_VGA:0x82040
irq_enable	DPCD_VGA:0x82044
irq_status	DPCD_VGA:0x82048
sca_offset	DPCD_VGA:0x82050
dfifo_debug	DPCD_VGA:0x82054
dfifo_mem_read_margin	DPCD_VGA:0x82074
EXTx_PPLL_REF_DIV_SRC	DPCD_VGA:0x83000
EXTx_PPLL_REF_DIV	DPCD_VGA:0x83004
EXTx_DIFF_POST_DIV_CNTL	DPCD_VGA:0x83010

Register Name	Offset Address
EXTx_PPLL_FB_DIV	DPCD_VGA:0x83014
EXTx_PPLL_FB_DIVIDER	DPCD_VGA:0x83018
EXTx_PPLL_POST_DIV	DPCD_VGA:0x8301C
EXTx_PPLL_CNTL	DPCD_VGA:0x83020
PxPLL_CNTL	DPCD_VGA:0x83024
PxPLL_INT_SS_DELAY	DPCD_VGA:0x8302C
PxPLL_DS_CNTL	DPCD_VGA:0x83034
PxPLL_VREG_CNTL	DPCD_VGA:0x83038
PxPLL_DEBUG	DPCD_VGA:0x8303C
PxPLL_MISC_CNTL	DPCD_VGA:0x83040
PxPLL_MISC2_CNTL	DPCD_VGA:0x83044
PxPLL_DTO_UNLOCK_CNTL	DPCD_VGA:0x83048
PxPLL_SS_CTRL1	DPCD_VGA:0x8304C
PxPLL_SS_CTRL2	DPCD_VGA:0x83050
PxPLL_FB_FORCE1	DPCD_VGA:0x83054
PxPLL_FB_FORCE2	DPCD_VGA:0x83058
DISPC_TEST_PATTERN_CONTROL	DPCD_VGA:0x84000
DISPC_TEST_PATTERN_PARAMETERS	DPCD_VGA:0x84004
DISPC_TEST_PATTERN_COLOR_MASK	DPCD_VGA:0x84008
DISPC_SW_TOTAL_H_TIME	DPCD_VGA:0x8400C
DISPC_SW_TOTAL_V_TIME	DPCD_VGA:0x84010
DISPC_SW_ACTIVE_H_TIME	DPCD_VGA:0x84014
DISPC_SW_ACTIVE_V_TIME	DPCD_VGA:0x84018
DISPC_SW_ACTIVE_H_START_TIME	DPCD_VGA:0x8401C
DISPC_SW_ACTIVE_V_START_TIME	DPCD_VGA:0x84020
DISPC_SW_HSYNC_TIME	DPCD_VGA:0x84024
DISPC_SW_VSYNC_TIME	DPCD_VGA:0x84028
DISPC_CONTROL	DPCD_VGA:0x8402C
DISPC_HW_TOTAL_H_TIME	DPCD_VGA:0x84030
DISPC_HW_TOTAL_V_TIME	DPCD_VGA:0x84034
DISPC_HW_ACTIVE_H_TIME	DPCD_VGA:0x84038
DISPC_HW_ACTIVE_V_TIME	DPCD_VGA:0x8403C
DISPC_HW_ACTIVE_H_START_TIME	DPCD_VGA:0x84040
DISPC_HW_ACTIVE_V_START_TIME	DPCD_VGA:0x84044
DISPC_HW_HSYNC_TIME	DPCD_VGA:0x84048
DISPC_HW_VSYNC_TIME	DPCD_VGA:0x8404C
DISPC_SYNC_CONTROL	DPCD_VGA:0x84050
DISPC_BLANK_PIXEL	DPCD_VGA:0x84054
DISPC_BLACK_PIXEL	DPCD_VGA:0x84058
DISPC_LAST_PIXEL	DPCD_VGA:0x8405C
DISPC_VCOUNT_STATUS	DPCD_VGA:0x84060
DISPC_HCOUNT_STATUS	DPCD_VGA:0x84064
DISPC_STATUS	DPCD_VGA:0x84068
DISPC_SW_TIMING_CONTROL	DPCD_VGA:0x8406C
DISPC_ERROR_STATUS	DPCD_VGA:0x84070
DISPC_ERROR_HCOUNT_STATUS	DPCD_VGA:0x84074
DISPC_ERROR_VCOUNT_STATUS	DPCD_VGA:0x84078
DISPC_ERROR_CONTROL	DPCD_VGA:0x8407C
DISPC_INTERRUPT_CONTROL	DPCD_VGA:0x84080
DISPC_FORCE_HCOUNT_DATA	DPCD_VGA:0x84084

Register Name	Offset Address
DISPC_FORCE_VCOUNT_DATA	DPCD_VGA:0x84088
DISPC_FRAME_COUNT	DPCD_VGA:0x8408C
DISPC_DISABLE_POINT_CONTROL	DPCD_VGA:0x84090
DISPC_ERROR_MASK	DPCD_VGA:0x84094
DISPC_TEST_PATTERN_COLOR	DPCD_VGA:0x84098
DISPC_DEBUG_MUX_CONTROL	DPCD_VGA:0x841F8
DISPC_DEBUG	DPCD_VGA:0x841FC
DAC_ENABLE	DPCD_VGA:0x85000
DAC_CRC_EN	DPCD_VGA:0x85008
DAC_CRC_CONTROL	DPCD_VGA:0x8500C
DAC_CRC_SIG_RGB_MASK	DPCD_VGA:0x85010
DAC_CRC_SIG_CONTROL_MASK	DPCD_VGA:0x85014
DAC_CRC_SIG_RGB	DPCD_VGA:0x85018
DAC_CRC_SIG_CONTROL	DPCD_VGA:0x8501C
DAC_SYNC_TRISTATE_CONTROL	DPCD_VGA:0x85020
DAC_AUTODETECT_CONTROL	DPCD_VGA:0x85028
DAC_AUTODETECT_CONTROL2	DPCD_VGA:0x8502C
DAC_AUTODETECT_CONTROL3	DPCD_VGA:0x85030
DAC_AUTODETECT_STATUS	DPCD_VGA:0x85034
DAC_FORCE_OUTPUT_CNTL	DPCD_VGA:0x8503C
DAC_FORCE_DATA	DPCD_VGA:0x85040
DAC_POWERDOWN	DPCD_VGA:0x85050
DAC_CONTROL	DPCD_VGA:0x85058
DAC_COMPARATOR_ENABLE	DPCD_VGA:0x8505C
DAC_COMPARATOR_OUTPUT	DPCD_VGA:0x85060
DAC_PWR_CNTL	DPCD_VGA:0x85068
DAC_DFT_CONFIG	DPCD_VGA:0x8506C
DAC_MACRO_CNTL	DPCD_VGA:0x85074
DAC_TEST_ENABLE	DPCD_VGA:0x8507C
DAC_MANUAL_DETECTION_CNTL	DPCD_VGA:0x85080
DAC_DEBUG_MUX_CNTL	DPCD_VGA:0x85084
DAC_BANDGAP_ADJUSTMENT	DPCD_VGA:0x85088
DAC_PIXEL_COMPARE_CONTROL	DPCD_VGA:0x8508C
DAC_PIXEL_COMPARE_ERROR_HCOUNT	DPCD_VGA:0x85090
DAC_PIXEL_COMPARE_ERROR_VCOUNT	DPCD_VGA:0x85094
DAC_PIXEL_COMPARE_ERROR_EXPECTED_PIXEL	DPCD_VGA:0x85098
DAC_PIXEL_COMPARE_ERROR_COMPUTED_PIXEL	DPCD_VGA:0x8509C
DAC_PIXEL_COMPARE_ERROR_STATUS	DPCD_VGA:0x850A0
DAC_LDO_CONTROL	DPCD_VGA:0x850A4
EFUS_DAC_ADJUSTMENT_CONTROL	DPCD_VGA:0x850A8
AUX_DPHY_TX_REF_CONTROL	DPCD_VGA:0x86000
AUX_DPHY_TX_CONTROL	DPCD_VGA:0x86004
AUX_DPHY_RX_CONTROL0	DPCD_VGA:0x86008
AUX_DPHY_TIMEOUTS	DPCD_VGA:0x8600C
AUX_DPHY_RX_CONTROL1	DPCD_VGA:0x86010
AUX_DPHY_STATUS	DPCD_VGA:0x86014
AUX_ERROR_STATUS	DPCD_VGA:0x86018
AUX_XACT_TIMEOUT_LEN	DPCD_VGA:0x8601C
AUX_TEST_MODE	DPCD_VGA:0x86020

Register Name	Offset Address
AUX_SCRATCH0	DPCD_VGA:0x86024
AUX_SCRATCH1	DPCD_VGA:0x86028
AUX_SCRATCH2	DPCD_VGA:0x8602C
AUX_SCRATCH3	DPCD_VGA:0x86030
AUX_SCRATCH4	DPCD_VGA:0x86034
AUX_PAD_CTRL	DPCD_VGA:0x86038
AUX_DETECT_TIMEOUT	DPCD_VGA:0x8603C
IMPCAL_AUXN	DPCD_VGA:0x86044
IMPCAL_PERIOD	DPCD_VGA:0x86048
IMPCAL_CTRL	DPCD_VGA:0x8604C
IMPCAL_PAD_TEST	DPCD_VGA:0x86050
DC_I2C_CONTROL	DPCD_VGA:0x87000
DC_I2C_ARBITRATION	DPCD_VGA:0x87004
DC_I2C_INTERRUPT_CONTROL	DPCD_VGA:0x87008
DC_I2C_SW_STATUS	DPCD_VGA:0x8700C
DC_I2C_DDC1_HW_STATUS	DPCD_VGA:0x87010
DC_I2C_DDC1_SPEED	DPCD_VGA:0x87014
DC_I2C_DDC1_SETUP	DPCD_VGA:0x87018
DC_I2C_TRANSACTION0	DPCD_VGA:0x8701C
DC_I2C_TRANSACTION1	DPCD_VGA:0x87020
DC_I2C_TRANSACTION2	DPCD_VGA:0x87024
DC_I2C_TRANSACTION3	DPCD_VGA:0x87028
DC_I2C_DATA	DPCD_VGA:0x8702C
DC_I2C_EDID_DETECT_CONTROL	DPCD_VGA:0x87030
DC_I2C_EDID_DETECT_READ_ADDRESS	DPCD_VGA:0x87034
DC_I2C_EDID_DETECT_WAIT_TIME	DPCD_VGA:0x87038
DC_I2C_EDID_DETECT_STATUS	DPCD_VGA:0x8703C
I2C_DEBUG_BUS	DPCD_VGA:0x87FFC
EC_SHARED_CLK_ENABLE	DPCD_VGA:0x88000
EC_EXT_VREG_OFF	DPCD_VGA:0x88004
EC_VGA_CLK_ENABLE	DPCD_VGA:0x88008
EC_SHARED_SOFT_RESET	DPCD_VGA:0x8800C
EC_VGA_SOFT_RESET	DPCD_VGA:0x88014
EC_CLK_MUX_CNTL	DPCD_VGA:0x88018
EC_DEBUG_CLKMUX_SEL	DPCD_VGA:0x8801C
EC_DACPM_CONTROL	DPCD_VGA:0x88020
EC_DACPM_DAC_WAIT_COUNT	DPCD_VGA:0x88024
EC_DACPM_DAC_BANDGAP_ON_COUNT	DPCD_VGA:0x88028
EC_DPLLPM_CONTROL	DPCD_VGA:0x88030
EC_DPLLPM_DPLL_REGULATOR_SETTLING_COUNT	DPCD_VGA:0x88034
EC_DPLLPM_DPLL_LOCK_COUNT	DPCD_VGA:0x88038
EC_DPLLPM_MEASURE_COUNT	DPCD_VGA:0x8803C
EC_DPLLPM_SOF_COUNT	DPCD_VGA:0x88040
EC_DPLLPM_MULTIPLIER_OFFSET	DPCD_VGA:0x88044
EC_REF_CLK_RATE	DPCD_VGA:0x88048
EC_REF_CLK_RATE_MHZ	DPCD_VGA:0x8804C
EC_PIXEL_RATE	DPCD_VGA:0x88050
EC_LS_CLK_RATE	DPCD_VGA:0x88054
EC_DPLL_POST_DIV	DPCD_VGA:0x88058
EC_DPLL_FB_DIVIDER	DPCD_VGA:0x8805C

Register Name	Offset Address
EC_DPLL_VCO_TARGET	DPCD_VGA:0x88060
EC_PCIEPM_CONTROL	DPCD_VGA:0x88070
EC_PCIEPM_PCIE_WAIT_COUNT	DPCD_VGA:0x88074
EC_PCIEPM_PCIE_FRONTEND_ON_COUNT	DPCD_VGA:0x88078
EC_PCIEPLLPM_CONTROL	DPCD_VGA:0x88080
EC_DPLLPM_DPLL_WAIT_VREG_RESET_COUNT	DPCD_VGA:0x88084
EC_DPLLPM_DPLL_VREG_RESET_COUNT	DPCD_VGA:0x88088
EC_DPLLPM_DPLL_BIAS_POWERUP_COUNT	DPCD_VGA:0x8808C
EC_DACPM_DAC_LDO_ON_COUNT	DPCD_VGA:0x88090
EC_DACPM_DAC_RGBDAC_ON_COUNT	DPCD_VGA:0x88094
dbgmux_control	DPCD_VGA:0x88180
dbgmux_zoomcontrol	DPCD_VGA:0x88184
dbgmux_gpiocontrol	DPCD_VGA:0x88188

DPCD_DPCD_REV - RW - 8 bits - DPCD_VGA:0x0

Field Name	Bits	Default	Description
DPCD_DPCD_REV (R)	7:0	0x11	Bits 3:0 = Minor revision number Bits 7:4 = Major revision number Read as 0x11 for DPCD Rev.1.1 Note: The DPCD revision number does not necessarily match the DisplayPort version number.

DPCD revision number

DPCD_MAX_LINK_RATE - RW - 8 bits - DPCD_VGA:0x1

Field Name	Bits	Default	Description
DPCD_MAX_LINK_RATE (R)	7:0	0xa	Indicates the maximum link rate supported

Maximum link rate of Main Link lanes = Value x 0.27 Gbps per lane

DPCD_MAX_LANE_COUNT - RW - 8 bits - DPCD_VGA:0x2

Field Name	Bits	Default	Description
DPCD_MAX_LANE_COUNT (R)	4:0	0x4	Bits 4:0 = MAX_LANE_COUNT For Rev.1.1, only the following three values are supported. All other values are reserved. Set by input sink_dprl_max_lane_count. 0x1 = One lane 0x2 = Two lanes 0x4 = Four lanes For one-lane configuration, Lane0 is used. For 2-lane configuration, Lane0 and Lane1 are used.
DPCD_ENHANCED_FRAME_CAP (R)	7	0x1	Bit 7 = ENHANCED_FRAME_CAP Read as 0x1 = Enhanced Framing symbol sequence for BS, SR, CPBS, and CPSR is supported

Maximum number of lanes = Value

DPCD_MAX_DOWNSPREAD - RW - 8 bits - DPCD_VGA:0x3			
Field Name	**Bits**	**Default**	**Description**
DPCD_MAX_DOWNSPREAD (R)	0	0x1	Read as 1 = Up to 0.5% downspread.
DPCD_NO_AUX_HANDSHAKE_LINK_TRAINING (R)	6	0x0	Read as 0x0 = Requires AUX CH handshake to synchronize DisplayPort transmitter

Maximum down-spread supported.

DPCD_NORP - RW - 8 bits - DPCD_VGA:0x4			
Field Name	**Bits**	**Default**	**Description**
DPCD_NORP (R)	0	0x0	Read as 0x1 = Only one stream (video) supported

Number of DP Receive Port

DPCD_DOWNSTREAMPORT_PRESENT - RW - 8 bits - DPCD_VGA:0x5			
Field Name	**Bits**	**Default**	**Description**
DPCD_DWN_STRM_PORT_PRESENT (R)	0	0x1	Indicates the presence of a downstream port For Nutmeg VGA: Read as 0x1 when VGA device is connected, else 0x0 For Nutmeg LVDS: Read 0x1 - Device is present
DPCD_DWN_STRM_PORT_TYPE (R)	2:1	0x1	Indicates Port0 type For Nutmeg VGA: Read as 0x01 - Analog VGA For Nutmeg LVDS: Read as 0x11 - Others
DPCD_FORMAT_CONVERSION (R)	3	0x1	Indicates presence of format conversion For Nutmeg VGA: Read as 0x0 - no format conversion For Nutmeg LVDS: Read as 0x1 - Format conversion

Downstream port present

DPCD_MAIN_LINK_CHANNEL_CODING - RW - 8 bits - DPCD_VGA:0x6			
Field Name	**Bits**	**Default**	**Description**
DPCD_ANSI_8B10B (R)	0	0x1	Coding type Read as 0x1 = ANSI 8B/10B

Main Link Channel Coding

DPCD_DOWN_STREAM_PORT_COUNT - RW - 8 bits - DPCD_VGA:0x7			
Field Name	**Bits**	**Default**	**Description**
DPCD_DWN_STRM_PORT_COUNT (R)	3:0	0x1	The number of down stream ports. Port types enumerated at address 0x00080. Read as 0x1 - One downstream
DPCD_OUI_SUPPORT (R)	7	0x0	Indicates support of IEEE OUI Read as 0x1 - Device supports OUI

Downstream port count

DPCD_RECEIVE_PORT0_CAP_0 - RW - 8 bits - DPCD_VGA:0x8			
Field Name	**Bits**	**Default**	**Description**
DPCD_LOCAL_EDID_PRESENT (R)	1	0x1	Indicates presence of Local EDID Read as 0x1 EDID present
DPCD_ASSOCIATED_TO_PRECEDING_PORT (R)	2	0x0	Indicates if port is associated to preceding port Read as 0x0, port used for Main Link video

Receive port capabilities 0

DPCD_RECEIVE_PORT0_CAP_1 - RW - 8 bits - DPCD_VGA:0x9			
Field Name	**Bits**	**Default**	**Description**
DPCD_BUFFER_SIZE (R)	7:0	0x0	Indicates size of receive buffer. Values are size of pixel fifo. For Nutmeg VGA: Read as 0x1E0 (decimal 480) For Nutmeg LVDS: Read as 0x120 (decimel 288)

Downstream port capabilities

DPCD_DWN_STRM_PORT0_CAP_0 - RW - 8 bits - DPCD_VGA:0x80			
Field Name	**Bits**	**Default**	**Description**
DPCD_DWN_STRM_PORT0_TYPE (R)	2:0	0x1	Indicates port type For Nutmeg VGA: Read as 0x001 - Analog VGA For Nutmeg LVDS: Read as 0x100 - others
DPCD_DWN_STRM_PORT0_HPD (R)	3	0x0	Indicates awareness of HPD. For Nutmeg VGA: Read as 0x1 -Downstream port is HPD aware For Nutmeg LVDS: Read as 0x0 - Downstream port is not HPD aware

Downstream port capabilities register

DPCD_LINK_BW_SET - RW - 8 bits - DPCD_VGA:0x100			
Field Name	**Bits**	**Default**	**Description**
DPCD_LINK_BW_SET	7:0	0xa	Sets Link BW speed 0xA - 2.7 Gbps per lane. Others - Reserved

Sets Link BW speed

DPCD_LANE_COUNT_SET - RW - 8 bits - DPCD_VGA:0x101			
Field Name	**Bits**	**Default**	**Description**
DPCD_LANE_COUNT_SET	4:0	0x0	0x4 - 4 Lanes (Nutmeg VGA only) 0x2 - 2 Lanes 0x1 - 1 Lane
DPCD_ENHANCED_FRAME_EN	7	0x0	Enables Enhanced Framing symbols 0x0 - Enhanced Framing symbol sequence is not enabled 0x1 - Enhanced Framing symbol sequence is enabled

Sets Numebr of active lanes in link

DPCD_TRAINING_PATTERN_SET - RW - 8 bits - DPCD_VGA:0x102			
Field Name	**Bits**	**Default**	**Description**
DPCD_TRAINING_PATTERN_SET	1:0	0x0	Link training pattern setting 0x0 - Training not in progress 0x1 - Training Pattern 1 0x2 - Training Pattern 2 0x3 - Reserved
DPCD_LINK_QUAL_PATTERN_SET	3:2	0x0	Link Quality Pattern set 0x0 - Link quality test pattern not transmitted 0x1 - D10.2 test pattern (unscrambled) 0x2 - Symbol Error Rate measurement pattern transmitted 0x3 - PRBS7 transmitted
DPCD_RECOVERED_CLOCK_OUT_EN	4	0x0	Recovered Clock Output 0x0 - Recovered clock output from a test pad of DisplayPort RX not enabled 0x1 - Recovered clock output from a test pad of DisplayPort Rx enabled
DPCD_SCRAMBLING_DISABLE	5	0x0	Scrambling disable 0x0 - DisplayPort Receiver descrambles data symbols after 8b10b decode 0x1 - DisplayPort Receiver does not descramble data symbols
DPCD_SYMBOL_ERROR_COUNT_SEL	7:6	0x0	Symbol Error Count Select 0x0 - Disparity Error and Illegal Symbol Error 0x1 - Disparity Error 0x2 - Illegal symbol error 0x3 - Reserved

Sets Transmitted data parameters

DPCD_TRAINING_LANE0_SET - RW - 8 bits - DPCD_VGA:0x103			
Field Name	**Bits**	**Default**	**Description**
DPCD_VOLTAGE_SWING_SET	1:0	0x0	Voltage swing set 0x0 - Training Pattern 1 with voltage swing level 0 0x1 - Training Pattern 1 with voltage swing level 1 0x2 - Training Pattern 1 with voltage swing level 2 0x3 - Training Pattern 1 with voltage swing level 3
DPCD_MAX_SWING_REACHED	2	0x0	Maximum Swing Reached 0x0 - Maximum driven current has not been reached 0x1 - Maximum driven current has been reached
DPCD_PRE_EMPHASIS_SET	4:3	0x0	Pre-emphasis set 0x0 - Training Pattern 2 without pre-emphasis 0x1 - Training Pattern 2 with pre-emphasis level 1 0x2 - Training Pattern 2 with pre-emphasis level 2 0x3 - Training Pattern 2 with pre-emphasis level 3
DPCD_MAX_PRE_EMPHASIS_REACHED	5	0x0	Maximum Pre-emphasis Reached 0x0 - Maximum Pre-emphasis level has not been reached 0x1 - Maximum Pre-emphasis level has been reached

Link Training Control Lane 0

DPCD_TRAINING_LANE1_SET - RW - 8 bits - DPCD_VGA:0x104			
Field Name	**Bits**	**Default**	**Description**
DPCD_VOLTAGE_SWING_SET	1:0	0x0	Voltage swing set 0x0 - Training Pattern 1 with voltage swing level 0 0x1 - Training Pattern 1 with voltage swing level 1 0x2 - Training Pattern 1 with voltage swing level 2 0x3 - Training Pattern 1 with voltage swing level 3
DPCD_MAX_SWING_REACHED	2	0x0	Maximum Swing Reached 0x0 - Maximum driven current has not been reached 0x1 - Maximum driven current has been reached

DPCD_TRAINING_LANE1_SET - RW - 8 bits - DPCD_VGA:0x104			
Field Name	**Bits**	**Default**	**Description**
DPCD_PRE_EMPHASIS_SET	4:3	0x0	Pre-emphasis set 0x0 - Training Pattern 2 without pre-emphasis 0x1 - Training Pattern 2 with pre-emphasis level 1 0x2 - Training Pattern 2 with pre-emphasis level 2 0x3 - Training Pattern 2 with pre-emphasis level 3
DPCD_MAX_PRE_EMPHASIS_REACHED	5	0x0	Maximum Pre-emphasis Reached 0x0 - Maximum Pre-emphasis level has not been reached 0x1 - Maximum Pre-emphasis level has been reached

Link Training Control Lane 1

DPCD_TRAINING_LANE2_SET - RW - 8 bits - DPCD_VGA:0x105			
Field Name	**Bits**	**Default**	**Description**
DPCD_VOLTAGE_SWING_SET	1:0	0x0	Voltage swing set 0x0 - Training Pattern 1 with voltage swing level 0 0x1 - Training Pattern 1 with voltage swing level 1 0x2 - Training Pattern 1 with voltage swing level 2 0x3 - Training Pattern 1 with voltage swing level 3
DPCD_MAX_SWING_REACHED	2	0x0	Maximum Swing Reached 0x0 - Maximum driven current has not been reached 0x1 - Maximum driven current has been reached
DPCD_PRE_EMPHASIS_SET	4:3	0x0	Pre-emphasis set 0x0 - Training Pattern 2 without pre-emphasis 0x1 - Training Pattern 2 with pre-emphasis level 1 0x2 - Training Pattern 2 with pre-emphasis level 2 0x3 - Training Pattern 2 with pre-emphasis level 3
DPCD_MAX_PRE_EMPHASIS_REACHED	5	0x0	Maximum Pre-emphasis Reached 0x0 - Maximum Pre-emphasis level has not been reached 0x1 - Maximum Pre-emphasis level has been reached

Link Training Control Lane 2

DPCD_TRAINING_LANE3_SET - RW - 8 bits - DPCD_VGA:0x106			
Field Name	**Bits**	**Default**	**Description**
DPCD_VOLTAGE_SWING_SET	1:0	0x0	Voltage swing set 0x0 - Training Pattern 1 with voltage swing level 0 0x1 - Training Pattern 1 with voltage swing level 1 0x2 - Training Pattern 1 with voltage swing level 2 0x3 - Training Pattern 1 with voltage swing level 3
DPCD_MAX_SWING_REACHED	2	0x0	Maximum Swing Reached 0x0 - Maximum driven current has not been reached 0x1 - Maximum driven current has been reached
DPCD_PRE_EMPHASIS_SET	4:3	0x0	Pre-emphasis set 0x0 - Training Pattern 2 without pre-emphasis 0x1 - Training Pattern 2 with pre-emphasis level 1 0x2 - Training Pattern 2 with pre-emphasis level 2 0x3 - Training Pattern 2 with pre-emphasis level 3
DPCD_MAX_PRE_EMPHASIS_REACHED	5	0x0	Maximum Pre-emphasis Reached 0x0 - Maximum Pre-emphasis level has not been reached 0x1 - Maximum Pre-emphasis level has been reached

Link Training Control Lane 3

DPCD_DOWNSPREAD_CTRL - RW - 8 bits - DPCD_VGA:0x107			
Field Name	**Bits**	**Default**	**Description**
DPCD_SPREAD_AMP	4	0x0	Down spreading control 0x0 - No downspread 0x1 - Equal to or less than 0.5% down spread

Down Spreading control

DPCD_MAIN_LINK_CHANNEL_CODING_SET - RW - 8 bits - DPCD_VGA:0x108			
Field Name	**Bits**	**Default**	**Description**
DPCD_SET_ANSI8B10B	0	0x0	Channel coding set 0x1 - ANSI 8b/10B 0x0 - Reserved

Main Link Channel Coding Set

DPCD_SINK_COUNT - RW - 8 bits - DPCD_VGA:0x200			
Field Name	**Bits**	**Default**	**Description**
DPCD_SINK_COUNT (R)	5:0	0x0	Sink device count For Nutmeg VGA: Read as 0x0 when VGA device is not connected, 0x1 else For Nutmeg LVDS: Read as 0x1
DPCD_CP_READY (R)	6	0x0	Content Protection Read Read as 0x0

Sink Device Count

DPCD_DEVICE_SERVICE_IRQ_VECTOR - RW - 8 bits - DPCD_VGA:0x201			
Field Name	**Bits**	**Default**	**Description**
DPCD_SINK_SPECIFIC_IRQ	6	0x0	Sink Specific IRQ 0x0 - No Interrupts pending 0x1 - Sink specific interrupts pending Check register 0x00513 (DPCD_DPRL_IRQ_SERVICE) and register 0x00516 (DPCD_DPRL_INTIRQ_SERVICE) for specific Interrupts

Device IRQ service vector.

In Nutmeg, Remote Control Command, DPCD Automated Test, and CP IRQ's are not supported

DPCD_LANE0_1_STATUS - RW - 8 bits - DPCD_VGA:0x202			
Field Name	**Bits**	**Default**	**Description**
DPCD_LANE0_CR_DONE (R)	0	0x0	Lane 0 Clock Recovery done
DPCD_LANE0_CHANNEL_EQ_DONE (R)	1	0x0	Lane 0 Channel Equalization done
DPCD_LANE0_SYMBOL_LOCKED (R)	2	0x0	Lane 0 8b/10b symbol locked
DPCD_LANE1_CR_DONE (R)	4	0x0	Lane 1 Clock Recovery done
DPCD_LANE1_CHANNEL_EQ_DONE (R)	5	0x0	Lane 1 Channel Equalization done
DPCD_LANE1_SYMBOL_LOCKED (R)	6	0x0	Lane 1 8b/10b symbol locked

Lane 0 and 1 Status register

DPCD_LANE2_3_STATUS - RW - 8 bits - DPCD_VGA:0x203			
Field Name	**Bits**	**Default**	**Description**
DPCD_LANE2_CR_DONE (R)	0	0x0	Lane 2 Clock Recovery done
DPCD_LANE2_CHANNEL_EQ_DONE (R)	1	0x0	Lane 2 Channel Equalization done
DPCD_LANE2_SYMBOL_LOCKED (R)	2	0x0	Lane 2 8b/10b symbol locked
DPCD_LANE3_CR_DONE (R)	4	0x0	Lane 3 Clock Recovery done
DPCD_LANE3_CHANNEL_EQ_DONE (R)	5	0x0	Lane 3 Channel Equalization done
DPCD_LANE3_SYMBOL_LOCKED (R)	6	0x0	Lane 3 8b/10b symbol locked

Lane 2 and 3 Status register

DPCD_LANE_ALIGN_STATUS_UPDATED - RW - 8 bits - DPCD_VGA:0x204			
Field Name	**Bits**	**Default**	**Description**
DPCD_INTERLANE_ALIGN_DONE (R)	0	0x0	Interlane alignment done 0x0 - Interlane alignment not achieved 0x1 - Interlane alignment achieved
DPCD_DOWNSTREAM_PORT_STATUS_CHANGED (R)	6	0x0	Downstream port status changed Read as 0x0
DPCD_LINK_STATUS_UPDATED (R)	7	0x0	Link status updated 0x0 - No change in status 0x1 - Link status and adjust request updated since the last read. Bit is cleared after read

Lane Alignment Status Updated

DPCD_SINK_STATUS - RW - 8 bits - DPCD_VGA:0x205			
Field Name	**Bits**	**Default**	**Description**
DPCD_RECEIVE_PORT_0_STATUS (R)	0	0x0	Port 0 status 0x0 - Sink device is out of synchronization. 0x1 - Sink device is in synchronization

Sink Status.

Port 1 is not present, and does not exist in registers

DPCD_ADJUST_REQUEST_LANE0_1 - RW - 8 bits - DPCD_VGA:0x206			
Field Name	**Bits**	**Default**	**Description**
DPCD_VOLTAGE_SWING_LANE0 (R)	1:0	0x0	Voltage swing request lane 0 0x0 - Level 0 0x1 - Level 1 0x2 - Level 2 0x3 - Level 3
DPCD_PRE_EMPHASIS_LANE0 (R)	3:2	0x0	Pre-emphasis request lane 0 0x0 - Level 0 0x1 - Level 1 0x2 - Level 2 0x3 - Level 3
DPCD_VOLTAGE_SWING_LANE1 (R)	5:4	0x0	Voltage swing request lane 1 0x0 - Level 0 0x1 - Level 1 0x2 - Level 2 0x3 - Level 3
DPCD_PRE_EMPHASIS_LANE1 (R)	7:6	0x0	Pre-emphasis request lane 1 0x0 - Level 0 0x1 - Level 1 0x2 - Level 2 0x3 - Level 3

Adjustment request register for lane 0 and 1

DPCD_ADJUST_REQUEST_LANE2_3 - RW - 8 bits - DPCD_VGA:0x207			
Field Name	**Bits**	**Default**	**Description**
DPCD_VOLTAGE_SWING_LANE2 (R)	1:0	0x0	Voltage swing request lane 2 0x0 - Level 0 0x1 - Level 1 0x2 - Level 2 0x3 - Level 3
DPCD_PRE_EMPHASIS_LANE2 (R)	3:2	0x0	Pre-emphasis request lane 2 0x0 - Level 0 0x1 - Level 1 0x2 - Level 2 0x3 - Level 3
DPCD_VOLTAGE_SWING_LANE3 (R)	5:4	0x0	Voltage swing request lane 3 0x0 - Level 0 0x1 - Level 1 0x2 - Level 2 0x3 - Level 3
DPCD_PRE_EMPHASIS_LANE3 (R)	7:6	0x0	Pre-emphasis request lane 3 0x0 - Level 0 0x1 - Level 1 0x2 - Level 2 0x3 - Level 3

Adjustment request register for lane 2 and 3

DPCD_TRAINING_SCORE_LANE0 - RW - 8 bits - DPCD_VGA:0x208			
Field Name	**Bits**	**Default**	**Description**
DPCD_TRAINING_SCORE_LANE (R)	7:0	0x0	Training score lane 0 Read as 0x0 - Score not implemented in Nutmeg

Training Score Lane 0

DPCD_TRAINING_SCORE_LANE1 - RW - 8 bits - DPCD_VGA:0x209			
Field Name	**Bits**	**Default**	**Description**
DPCD_TRAINING_SCORE_LANE (R)	7:0	0x0	Training score lane 1 Read as 0x0 - Score not implemented in Nutmeg

Training Score Lane 1

DPCD_TRAINING_SCORE_LANE2 - RW - 8 bits - DPCD_VGA:0x20A			
Field Name	**Bits**	**Default**	**Description**
DPCD_TRAINING_SCORE_LANE (R)	7:0	0x0	Training score lane 2 Read as 0x0 - Score not implemented in Nutmeg

Training Score Lane 2

DPCD_TRAINING_SCORE_LANE3 - RW - 8 bits - DPCD_VGA:0x20B			
Field Name	**Bits**	**Default**	**Description**
DPCD_TRAINING_SCORE_LANE (R)	7:0	0x0	Training score lane 3 Read as 0x0 - Score not implemented in Nutmeg

Training Score Lane 3

DPCD_SYMBOL_ERROR_COUNT_LANE0 - RW - 16 bits - DPCD_VGA:0x210			
Field Name	**Bits**	**Default**	**Description**
DPCD_ERROR_COUNT (R)	14:0	0x0	Error count For PRBS7 rate measurement, this is the number of bit errors For others, number of symbol errors.
DPCD_ERROR_COUNT_VALID (R)	15	0x0	Error count valid 0x0 - Error count is not valid. 0x1 - Error count is valid, bit is reset on read

Symbol Error Count Lane 0

DPCD_SYMBOL_ERROR_COUNT_LANE1 - RW - 16 bits - DPCD_VGA:0x212			
Field Name	**Bits**	**Default**	**Description**
DPCD_ERROR_COUNT (R)	14:0	0x0	Error count For PRBS7 rate measurement, this is the number of bit errors For others, number of symbol errors.
DPCD_ERROR_COUNT_VALID (R)	15	0x0	Error count valid 0x0 - Error count is not valid. 0x1 - Error count is valid, bit is reset on read

Symbol Error Count Lane 1

DPCD_SYMBOL_ERROR_COUNT_LANE2 - RW - 16 bits - DPCD_VGA:0x214			
Field Name	**Bits**	**Default**	**Description**
DPCD_ERROR_COUNT (R)	14:0	0x0	Error count For PRBS7 rate measurement, this is the number of bit errors For others, number of symbol errors.
DPCD_ERROR_COUNT_VALID (R)	15	0x0	Error count valid 0x0 - Error count is not valid. 0x1 - Error count is valid, bit is reset on read

Symbol Error Count Lane 2

DPCD_SYMBOL_ERROR_COUNT_LANE3 - RW - 16 bits - DPCD_VGA:0x216			
Field Name	**Bits**	**Default**	**Description**
DPCD_ERROR_COUNT (R)	14:0	0x0	Error count For PRBS7 rate measurement, this is the number of bit errors For others, number of symbol errors.
DPCD_ERROR_COUNT_VALID (R)	15	0x0	Error count valid 0x0 - Error count is not valid. 0x1 - Error count is valid, bit is reset on read

Symbol Error Count Lane 3

DPCD_TEST_CRC_R_CR - RW - 16 bits - DPCD_VGA:0x240			
Field Name	**Bits**	**Default**	**Description**
DPCD_TEST_CRC_R_CR (R)	15:0	0x0	16 bit CRC value

Stores 16 bit CRC value for R component

DPCD_TEST_CRC_G_Y - RW - 16 bits - DPCD_VGA:0x242			
Field Name	**Bits**	**Default**	**Description**
DPCD_TEST_CRC_G_Y (R)	15:0	0x0	16 bit CRC value

Stores 16 bit CRC value for G component

DPCD_TEST_CRC_B_CB - RW - 16 bits - DPCD_VGA:0x244			
Field Name	**Bits**	**Default**	**Description**
DPCD_TEST_CRC_B_CB (R)	15:0	0x0	16 bit CRC value

Stores 16 bit CRC value for B component

DPCD_TEST_SINK_MISC - RW - 8 bits - DPCD_VGA:0x246			
Field Name	**Bits**	**Default**	**Description**
DPCD_TEST_CRC_COUNT (R)	3:0	0x0	4 bit wrap counter which increments each time the TEST_CRC_x_x are updated. Reset to 0 when TEST_SINK bit 0 == 0
DPCD_TEST_CRC_SUPPORTED (R)	4	0x0	read as 0x1 - CRC supported by this device.

Misc CRC

DPCD_TEST_SINK - RW - 8 bits - DPCD_VGA:0x270			
Field Name	**Bits**	**Default**	**Description**
DPCD_TEST_SINK_START	0	0x0	0x0 - Stop calculating CRC on the next frame 0x1 - Start calculating CRC on the next frame

CRC Start control

DPCD_SRC_IEEE_OUI - RW - 24 bits - DPCD_VGA:0x300			
Field Name	**Bits**	**Default**	**Description**
DPCD_SRC_IEEE_OUI	23:0	0x0	Source IEEE OUI value

Source IEEE OUI value

DPCD_BRANCH_IEEE_OUI - RW - 24 bits - DPCD_VGA:0x500			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_IEEE_OUI (R)	23:0	0x1A0000	Read as 0x1A0000

Nutmeg IEEE OUI value

DPCD_BRANCH_CHIPID0 - RW - 8 bits - DPCD_VGA:0x503			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_CHIPID0 (R)	7:0	0x64	Byte 0 of Chip ID

Byte 0 of Chip ID

DPCD_BRANCH_CHIPID1 - RW - 8 bits - DPCD_VGA:0x504			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_CHIPID1 (R)	7:0	0x6E	Byte 1 of Chip iD

Byte 1 of Chip ID

DPCD_BRANCH_CHIPID2 - RW - 8 bits - DPCD_VGA:0x505			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_CHIPID2 (R)	7:0	0x6F	Byte 2 of Chip ID

Byte 2 of Chip ID

DPCD_BRANCH_CHIPID3 - RW - 8 bits - DPCD_VGA:0x506			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_CHIPID3 (R)	7:0	0x6D	Byte 3 of Chip ID

Byte 3 of Chip ID

DPCD_BRANCH_CHIPID4 - RW - 8 bits - DPCD_VGA:0x507			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_CHIPID4 (R)	7:0	0x6C	Byte 4 of Chip ID

Byte 4 of Chip ID

DPCD_BRANCH_CHIPID5 - RW - 8 bits - DPCD_VGA:0x508			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_CHIPID5 (R)	7:0	0x41	Byte 5 of Chip ID

Byte 5 of Chip ID

DPCD_BRANCH_REV - RW - 8 bits - DPCD_VGA:0x509			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_MIN_REV (R)	3:0	0x0	Chip Minor Revision
DPCD_BRANCH_MAJ_REV (R)	7:4	0x0	Chip Major revision

Chip Revision

DPCD_BRANCH_SW_MAJ_REV - RW - 8 bits - DPCD_VGA:0x50A			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_SW_MAJ_REV (R)	7:0	0x0	Software Major revision Read as 0x00, no software in Nutmeg

Software Major revision

DPCD_BRANCH_SW_MIN_REV - RW - 8 bits - DPCD_VGA:0x50B			
Field Name	**Bits**	**Default**	**Description**
DPCD_BRANCH_SW_MIN_REV (R)	7:0	0x0	Software Minor revision Read as 0x00, no software in Nutmeg

Software Minor Revision

DPCD_DPRL_LANESETUP0 - RW - 8 bits - DPCD_VGA:0x510			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_LANE_MAP	7:0	0x0	Physical to logical lane mapping bit [1:0] - Logical lane number of physical lane 0 bit [3:2] - Logical lane number of physical lane 1 bit [5:4] - Logical lane number of physical lane 2 bit [7:6] - Logical lane number of physical lane 3

Nutmeg lane setup 0

DPCD_DPRL_LANESETUP1 - RW - 8 bits - DPCD_VGA:0x511			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_LANEINV	3:0	0x0	Lane inversion control bit 0 - Invert Lane 0 bit 1 - Invert Lane 1 bit 2 - Invert Lane 2 bit 3 - Invert Lane 3

Nutmeg lane setup 1

DPCD_DPRL_IRQ_SERVICE - RW - 8 bits - DPCD_VGA:0x512			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_IRQ_SVC (R)	7:0	0x0	For VGA: bit 0 - Display Controler Error bit 1 - Hw Timing Change Event bit 2 - DFIFO Error bit 3 - I2C SW DONE bit 4 - I2C HW DONE bit 7:5 - RESERVED

IRQ Service - Non DPRL

DPCD_DPRL_IRQ_EN - RW - 8 bits - DPCD_VGA:0x513			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_IRQ_EN	7:0	0x0	Bit-wise enable of Interrupts of IRQ SVC register

IRQ Enable for IRQ SVC

DPCD_DPRL_IRQ_GLOBEN - RW - 8 bits - DPCD_VGA:0x514			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_IRQ_GLOBEN	0	0x1	0x0 - Interrupts are not enabled 0x1 - Interrupts are enabled Bit will deassert when interrupt is active. Bit will reassert upon write or expiration of IRQ Timer as specified in IRQ_TIMEOUT
DPCD_DPRL_REQTRN_IRQ_EN	1	0x1	Enable for Training Request IRQ event. Default enabled
DPCD_DPRL_SINKEVENT_IRQ_EN	2	0x1	Enable for Sink Event IRQ event. Default enabled

Global IRQ enable

DPCD_DPRL_INTIRQ_SERVICE - RW - 16 bits - DPCD_VGA:0x516			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_INTIRQ_SVC	15:0	0x0	bit 0 - Symbol Framing error bit 1 - MSA Mismatch error bit 2 - VBID Mismatch error bit 6:3 - Lane elastic fifo overflow bit 7 - reserved bit 8 - Excessive Symbol Error bit 9 - Loss of Symbol Alignment bit 10 - Loss Interlane Alignment

IRQ Service - DPRL

DPCD_DPRL_INTIRQ_EN - RW - 16 bits - DPCD_VGA:0x518			
Field Name	**Bits**	**Default**	**Description**

DPCD_DPRL_INTIRQ_EN	15:0	0x0	Bit-wise enable of interrupts of INTIRQ register

IRQ Enable for INTIRQ SVC

DPCD_DPRL_IRQ_TIMEOUT - RW - 32 bits - DPCD_VGA:0x51C			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_IRQ_TIMEOUT	31:0	0x7d0	Duration of timeout in microsecond after HPD assertion and reenable of IRQs

IRQ Timeout

DPCD_DPRL_IRQ_HPDTIME - RW - 24 bits - DPCD_VGA:0x520			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_IRQ_HPDTIME	23:0	0x2ee	Duration of HPD Pulse in microsecond

HPD Time

DPCD_DPRL_DEBUG - RW - 8 bits - DPCD_VGA:0x523			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_DBG_LANESEL	1:0	0x0	Lane select for lane-specific debug signals
DPCD_DPRL_DBG_SEL	7:2	0x0	Main MUX select

DEBUG Mux control

DPCD_DPRL_PRBS23 - RW - 8 bits - DPCD_VGA:0x525			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_PRBS23_EN	0	0x0	Enable PRBS23 checking instead of PRBS7

PRBS23 Enable

DPCD_DPRL_DEBUG_OUT - RW - 32 bits - DPCD_VGA:0x528			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_DBG_OUT (R)	31:0	0x0	Out of debug mux

DEBUG Output

DPCD_DPRL_CR_THRESH - RW - 8 bits - DPCD_VGA:0x580			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_CR_THRESH	7:0	0x80	Number of consecutive, error-free TP1 symbols are seen before CR_DONE is reported.

Clock Recovery Done Threshold

DPCD_DPRL_EQ_THRESH - RW - 8 bits - DPCD_VGA:0x581			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_EQ_THRESH	7:0	0x10	Number of consecutive, error-free TP2 sequences are seen before EQ_DONE is reported

Equalization Done Threshold

DPCD_DPRL_LFSRADV - RW - 8 bits - DPCD_VGA:0x582			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_LFSRADV	0	0x0	Scrambler LFSR Advance mode 0x0 - LFSR is advanced only on Data symbols 0x1 - LFSR is advanced on every symbol

Scrambler LFSR Advance mode

DPCD_DPRL_RFCHAL - RW - 32 bits - DPCD_VGA:0x584			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_RFCHAL	31:0	0x0	Authentication block Challenge Value

Authentication Challenge

DPCD_DPRL_RFRESP - RW - 32 bits - DPCD_VGA:0x588			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_RFRESP (R)	31:0	0x0	Authentication block Response Value

Authentication Response

DPCD_DPRL_RFCTRL - RW - 8 bits - DPCD_VGA:0x58C			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_RFCTRL	3:0	0x0	Authentication block Control value

Authentication Control

DPCD_DPRL_RFSTAT - RW - 8 bits - DPCD_VGA:0x58D			
Field Name	**Bits**	**Default**	**Description**
DPCD_DPRL_RFSTAT (R)	2:0	0x0	Authentication block Status value

Authentication Status

DPCD_SET_POWER - RW - 8 bits - DPCD_VGA:0x600			
Field Name	**Bits**	**Default**	**Description**
DPCD_SET_POWER	1:0	0x2	Nutmeg Power Control 0x1 - Sets Nutmeg to normal operation 0x2 - Sets Nutmeg to Power Down mode

Nutmeg Power control

PCIERXVGAC_RX0_STATUS1 - RW - 32 bits - DPCD_VGA:0x80000			
Field Name	**Bits**	**Default**	**Description**
RX_SAOUT (R)	3:0	0x0	Rx retimed sampler outputs ([0] and [2] are data and [1] and [3] are edge)
RX_PRBS_ER (R)	4	0x0	Prbs10 checker error flag
RX_GEN2COMP (R)	5	0x0	Not used
RX_TOGGLE_ER (R)	6	0x0	Asserted if the toggle pattern is not received.
RX_CROUT (R)	13:7	0x0	Clock recovery debug output

PCIERXVGAC_RX1_STATUS1 - RW - 32 bits - DPCD_VGA:0x80100			
Field Name	**Bits**	**Default**	**Description**
RX_SAOUT (R)	3:0	0x0	Rx retimed sampler outputs ([0] and [2] are data and [1] and [3] are edge)
RX_PRBS_ER (R)	4	0x0	Prbs10 checker error flag
RX_GEN2COMP (R)	5	0x0	Not used
RX_TOGGLE_ER (R)	6	0x0	Asserted if the toggle pattern is not received.
RX_CROUT (R)	13:7	0x0	Clock recovery debug output

PCIERXVGAC_RX2_STATUS1 - RW - 32 bits - DPCD_VGA:0x80200			
Field Name	**Bits**	**Default**	**Description**
RX_SAOUT (R)	3:0	0x0	Rx retimed sampler outputs ([0] and [2] are data and [1] and [3] are edge)
RX_PRBS_ER (R)	4	0x0	Prbs10 checker error flag
RX_GEN2COMP (R)	5	0x0	Not used
RX_TOGGLE_ER (R)	6	0x0	Asserted if the toggle pattern is not received.
RX_CROUT (R)	13:7	0x0	Clock recovery debug output

PCIERXVGAC_RX3_STATUS1 - RW - 32 bits - DPCD_VGA:0x80300			
Field Name	**Bits**	**Default**	**Description**
RX_SAOUT (R)	3:0	0x0	Rx retimed sampler outputs ([0] and [2] are data and [1] and [3] are edge)
RX_PRBS_ER (R)	4	0x0	Prbs10 checker error flag
RX_GEN2COMP (R)	5	0x0	Not used
RX_TOGGLE_ER (R)	6	0x0	Asserted if the toggle pattern is not received.
RX_CROUT (R)	13:7	0x0	Clock recovery debug output

PCIERXVGAC_RX0_CONTROL1 - RW - 32 bits - DPCD_VGA:0x80004			
Field Name	**Bits**	**Default**	**Description**
RX_FRONTEND_EN	0	0x1	Rx frontend enable.
RX_DET_BLOCK	1	0x0	When asserted, sets P90_BRX_ELEC_IDLE_* low
RX_IDLEDET_EN	2	0x0	When deasserted, electrical idle detection is disabled
RX_EQ	4:3	0x0	Rx equalization setting 00 is minimum equalization and 11 is maximum equalization
RX_CR_EN	5	0x1	Clock recovery enable
RX_COMPSPD_EN	6	0x0	Not used
RX_CLK_DIV	8:7	0x0	Rx clock divider
RX_CLKG_EN	9	0x1	When de-asserted, disables clock gating in power saving modes
RX_INCAL_FORCE	10	0x0	When asserted, the anablog offset calibration is disabled
RX_EN	11	0x1	Rx enable

PCIERXVGAC_RX1_CONTROL1 - RW - 32 bits - DPCD_VGA:0x80104			
Field Name	**Bits**	**Default**	**Description**
RX_FRONTEND_EN	0	0x1	Rx frontend enable.
RX_DET_BLOCK	1	0x0	When asserted, sets P90_BRX_ELEC_IDLE_* low
RX_IDLEDET_EN	2	0x0	When deasserted, electrical idle detection is disabled
RX_EQ	4:3	0x0	Rx equalization setting 00 is minimum equalization and 11 is maximum equalization
RX_CR_EN	5	0x1	Clock recovery enable
RX_COMPSPD_EN	6	0x0	Not used
RX_CLK_DIV	8:7	0x0	Rx clock divider
RX_CLKG_EN	9	0x1	When de-asserted, disables clock gating in power saving modes
RX_INCAL_FORCE	10	0x0	When asserted, the anablog offset calibration is disabled
RX_EN	11	0x1	Rx enable

PCIERXVGAC_RX2_CONTROL1 - RW - 32 bits - DPCD_VGA:0x80204			
Field Name	**Bits**	**Default**	**Description**
RX_FRONTEND_EN	0	0x1	Rx frontend enable.
RX_DET_BLOCK	1	0x0	When asserted, sets P90_BRX_ELEC_IDLE_* low
RX_IDLEDET_EN	2	0x0	When deasserted, electrical idle detection is disabled
RX_EQ	4:3	0x0	Rx equalization setting 00 is minimum equalization and 11 is maximum equalization
RX_CR_EN	5	0x1	Clock recovery enable
RX_COMPSPD_EN	6	0x0	Not used
RX_CLK_DIV	8:7	0x0	Rx clock divider
RX_CLKG_EN	9	0x1	When de-asserted, disables clock gating in power saving modes
RX_INCAL_FORCE	10	0x0	When asserted, the anablog offset calibration is disabled
RX_EN	11	0x1	Rx enable

PCIERXVGAC_RX3_CONTROL1 - RW - 32 bits - DPCD_VGA:0x80304			
Field Name	**Bits**	**Default**	**Description**
RX_FRONTEND_EN	0	0x1	Rx frontend enable.
RX_DET_BLOCK	1	0x0	When asserted, sets P90_BRX_ELEC_IDLE_* low
RX_IDLEDET_EN	2	0x0	When deasserted, electrical idle detection is disabled
RX_EQ	4:3	0x0	Rx equalization setting 00 is minimum equalization and 11 is maximum equalization
RX_CR_EN	5	0x1	Clock recovery enable
RX_COMPSPD_EN	6	0x0	Not used
RX_CLK_DIV	8:7	0x0	Rx clock divider
RX_CLKG_EN	9	0x1	When de-asserted, disables clock gating in power saving modes
RX_INCAL_FORCE	10	0x0	When asserted, the anablog offset calibration is disabled
RX_EN	11	0x1	Rx enable

PCIERXVGAC_RX0_CONTROL2 - RW - 32 bits - DPCD_VGA:0x80008			
Field Name	**Bits**	**Default**	**Description**
RX_CRPHSIZE	1:0	0x1	Clock recovery phase filter size
RX_CROUT_SEL	2	0x1	Selects which registers are output to RX_CROUT
RX_CRFR_ON	3	0x0	When asserted clock recovery frequency loop enabled
RX_CRFR_BPASS	4	0x0	When asserted, bypasses the clock recovery freq estimator output with RX_CRFR
RX_CRFR	10:5	0x0	Bypass value for the clock reovery freq estimator output
RX_CRFRSIZE	12:11	0x1	clock recovery freq filter size
RX_CRCTRL_BPASS	13	0x0	When asserted, bypasses the clock recovery phase counter output with RX_CRCTL
RX_CRCTRL	20:14	0x0	Bypass value for the clock recovery phase counter output. Selected by asszerting RX_CRCTRL_BPASS
RX_TOGGLE_EN	21	0x0	Rx toggle pattern (1010101010 or 0101010101) recognition enable. RX_TOGGLE_ER is asserted if the toggle pattern is not received.
RX_PRBS_CLR	22	0x0	When asserted, clears the PRBS10 checker error flag.
RX_LBACK_EN	23	0x0	When asserted, the Rx receives its input from serial output of Tx
RX_NC_DATA_EN	24	0x0	Enable non-clocked data receiver circuit

PCIERXVGAC_RX0_CONTROL2 - RW - 32 bits - DPCD_VGA:0x80008			
Field Name	**Bits**	**Default**	**Description**
RX_TCLK_EN	25	0x0	When asserted, bypasses the recovered clock from teh clock recovery with test clock
RX_TEST_EN	26	0x0	Rx test data enable for scan mode

PCIERXVGAC_RX1_CONTROL2 - RW - 32 bits - DPCD_VGA:0x80108			
Field Name	**Bits**	**Default**	**Description**
RX_CRPHSIZE	1:0	0x1	Clock recovery phase filter size
RX_CROUT_SEL	2	0x1	Selects which registers are output to RX_CROUT
RX_CRFR_ON	3	0x0	When asserted clock recovery frequency loop enabled
RX_CRFR_BPASS	4	0x0	When asserted, bypasses the clock recovery freq estimator output with RX_CRFR
RX_CRFR	10:5	0x0	Bypass value for the clock reovery freq estimator output
RX_CRFRSIZE	12:11	0x1	clock recovery freq filter size
RX_CRCTRL_BPASS	13	0x0	When asserted, bypasses the clock recovery phase counter output with RX_CRCTL
RX_CRCTRL	20:14	0x0	Bypass value for the clock recovery phase counter output. Selected by asszerting RX_CRCTRL_BPASS
RX_TOGGLE_EN	21	0x0	Rx toggle pattern (1010101010 or 0101010101) recognition enable. RX_TOGGLE_ER is asserted if the toggle pattern is not received.
RX_PRBS_CLR	22	0x0	When asserted, clears the PRBS10 checker error flag.
RX_LBACK_EN	23	0x0	When asserted, the Rx receives its input from serial output of Tx
RX_NC_DATA_EN	24	0x0	Enable non-clocked data receiver circuit
RX_TCLK_EN	25	0x0	When asserted, bypasses the recovered clock from teh clock recovery with test clock
RX_TEST_EN	26	0x0	Rx test data enable for scan mode

PCIERXVGAC_RX2_CONTROL2 - RW - 32 bits - DPCD_VGA:0x80208			
Field Name	**Bits**	**Default**	**Description**
RX_CRPHSIZE	1:0	0x1	Clock recovery phase filter size
RX_CROUT_SEL	2	0x1	Selects which registers are output to RX_CROUT
RX_CRFR_ON	3	0x0	When asserted clock recovery frequency loop enabled
RX_CRFR_BPASS	4	0x0	When asserted, bypasses the clock recovery freq estimator output with RX_CRFR
RX_CRFR	10:5	0x0	Bypass value for the clock reovery freq estimator output
RX_CRFRSIZE	12:11	0x1	clock recovery freq filter size
RX_CRCTRL_BPASS	13	0x0	When asserted, bypasses the clock recovery phase counter output with RX_CRCTL
RX_CRCTRL	20:14	0x0	Bypass value for the clock recovery phase counter output. Selected by asszerting RX_CRCTRL_BPASS
RX_TOGGLE_EN	21	0x0	Rx toggle pattern (1010101010 or 0101010101) recognition enable. RX_TOGGLE_ER is asserted if the toggle pattern is not received.
RX_PRBS_CLR	22	0x0	When asserted, clears the PRBS10 checker error flag.
RX_LBACK_EN	23	0x0	When asserted, the Rx receives its input from serial output of Tx
RX_NC_DATA_EN	24	0x0	Enable non-clocked data receiver circuit
RX_TCLK_EN	25	0x0	When asserted, bypasses the recovered clock from teh clock recovery with test clock
RX_TEST_EN	26	0x0	Rx test data enable for scan mode

PCIERXVGAC_RX3_CONTROL2 - RW - 32 bits - DPCD_VGA:0x80308			
Field Name	**Bits**	**Default**	**Description**
RX_CRPHSIZE	1:0	0x1	Clock recovery phase filter size
RX_CROUT_SEL	2	0x1	Selects which registers are output to RX_CROUT
RX_CRFR_ON	3	0x0	When asserted clock recovery frequency loop enabled
RX_CRFR_BPASS	4	0x0	When asserted, bypasses the clock recovery freq estimator output with RX_CRFR
RX_CRFR	10:5	0x0	Bypass value for the clock reovery freq estimator output
RX_CRFRSIZE	12:11	0x1	clock recovery freq filter size
RX_CRCTRL_BPASS	13	0x0	When asserted, bypasses the clock recovery phase counter output with RX_CRCTL
RX_CRCTRL	20:14	0x0	Bypass value for the clock recovery phase counter output. Selected by asszerting RX_CRCTRL_BPASS
RX_TOGGLE_EN	21	0x0	Rx toggle pattern (1010101010 or 0101010101) recognition enable. RX_TOGGLE_ER is asserted if the toggle pattern is not received.
RX_PRBS_CLR	22	0x0	When asserted, clears the PRBS10 checker error flag.
RX_LBACK_EN	23	0x0	When asserted, the Rx receives its input from serial output of Tx
RX_NC_DATA_EN	24	0x0	Enable non-clocked data receiver circuit
RX_TCLK_EN	25	0x0	When asserted, bypasses the recovered clock from teh clock recovery with test clock
RX_TEST_EN	26	0x0	Rx test data enable for scan mode

PCIERXVGAC_RX0_ARESET - RW - 32 bits - DPCD_VGA:0x80010			
Field Name	**Bits**	**Default**	**Description**
ARESET	0	0x0	Asynchronous reset. Asserted at the beginning of slow-speed functional test to align RX_DATAOUT and RX_DATA_CLK accross all lanes

PCIERXVGAC_RX1_ARESET - RW - 32 bits - DPCD_VGA:0x80110			
Field Name	**Bits**	**Default**	**Description**
ARESET	0	0x0	Asynchronous reset. Asserted at the beginning of slow-speed functional test to align RX_DATAOUT and RX_DATA_CLK accross all lanes

PCIERXVGAC_RX2_ARESET - RW - 32 bits - DPCD_VGA:0x80210			
Field Name	**Bits**	**Default**	**Description**
ARESET	0	0x0	Asynchronous reset. Asserted at the beginning of slow-speed functional test to align RX_DATAOUT and RX_DATA_CLK accross all lanes

PCIERXVGAC_RX3_ARESET - RW - 32 bits - DPCD_VGA:0x80310			
Field Name	**Bits**	**Default**	**Description**
ARESET	0	0x0	Asynchronous reset. Asserted at the beginning of slow-speed functional test to align RX_DATAOUT and RX_DATA_CLK accross all lanes

PCIERXVGAC_RX_CLK_CONTROL - RW - 32 bits - DPCD_VGA:0x80400			
Field Name	**Bits**	**Default**	**Description**
use_sw_pcie_rx	0	0x0	sw override flag for PCIE_RX_CLK_DIV0~3 0=Use internal value 1=Use sw register value to override the setting

PCIERXPLL_MACRO_STATUS1 - RW - 32 bits - DPCD_VGA:0x81000			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_VCTRLADC (R)	3:0	0x0	PLL Control Voltage through adc
PCIERXPLL_FREQ_LOCK (R)	4	0x0	PLL Lock status 0=PLL not frequency locked 1=PLL frequency locked

PCIERXPLL_MACRO_CONTROL1 - RW - 32 bits - DPCD_VGA:0x81004			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_VCTRLADC_EN	0	0x1	PLL Voltage ADC enable 0=voltage ADC not enabled 1=voltage ADC enabled
PCIERXPLL_FREQ_LOCK_EN	3	0x1	Enable PLL Lock 0=Frequency lock detect not enabled 1=Frequency lock detect enabled
PCIERXPLL_CREN_MODE	4	0x0	Clock recovery enable mode 0=PLL is not in clock recovery mode 1=PLL is in clock recovery mode
PCIERXPLL_PBYPASS	5	0x0	Bypass 1x clock with PTCLK_1X 0=Normal operation 1=1x test clock passed to 1x functional clock output
PCIERXPLL_IDLEDET_TH	7:6	0x0	Electrical Idle detect threshold (not used in Nutmeg)
PCIERXPLL_PREFCLK_SEL	11	0x0	Reference Clock select (0x0 for Nutmeg) 0=REFCLK for PCIe 1=Disabled
PCIERXPLL_RESET_EN	13	0x0	External PLL reset enable. 0=PLL reset comes from internal counter (triggered by PLL_PDNB) 1=PLL reset comes from PLL_RESET
PCIERXPLL_FASTEN	14	0x0	Fast Lock enable (Not used in Nutmeg)
PCIERXPLL_ENSAT	15	0x0	Saturation behavior enable (Not used in Nutmeg)

PCIERXPLL_MACRO_CONTROL1 - RW - 32 bits - DPCD_VGA:0x81004			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_IBIAS	25:16	0xC6	Bandwidth control
PCIERXPLL_TCLK_10X_SRC	26	0x0	Source for 10X Test clock 0=clkpll_refclk 1=PLL_TCLK_10X

General PLL control

PCIERXPLL_MACRO_CONTROL2 - RW - 32 bits - DPCD_VGA:0x81008			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_BACKUP	15:0	0x0	Backup PLL control
PCIERXPLL_CLKF	22:16	0x0	Feedback Divider setting
PCIERXPLL_CLKR	27:23	0x0	Reference Divider setting
use_sw_pcierxpll	28	0x0	sw override flag for PCIERXPLL_CLKF and PCIERXPLL_IBIAS 0=Use internal value 1=Use sw register value to override the setting

PCIERXPLL_MACRO_CONTROL3 - RW - 32 bits - DPCD_VGA:0x8100C			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_PLL_TEST	13	0x0	PLL divdier counter test control 0=Normal Operation 1=Reference Divdier and Feedback Divider are cascaded and output on PLL_TESTOUT
PCIERXPLL_PTCLK_10X_EN	18	0x0	Enable 10x Test clock 0=Normal Operation 1=TX_CLK_10XP/N is bypassed with TCLK_10X

PCIERXPLL_PDNB_CONTROL - RW - 32 bits - DPCD_VGA:0x81104			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_PPLL_PDNB	0	0x1	Active low power down enable for PLL 0=PLL power down 1=PLL Power on
PCIERXPLL_BUF_PDNB	1	0x1	Active low power down enable for clock tree 0=10X Clock buffer power off 1=10X Clock buffer power on
PCIERXPLL_BIAS_GEN_PDNB	3	0x1	Active low power down enable for Bias generator 0=PLL Bias Generator power off 1=PLL Bias Generator power on

PCIERXPLL_RESET - RW - 32 bits - DPCD_VGA:0x81108			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_RESET	0	0x0	Pll reset 0=PLL is not reset 1=PLL is reset

PCIERXPLL_LOCK_CTRL - RW - 32 bits - DPCD_VGA:0x8110C			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_LOCK_TIME	7:0	0x80	number of microseconds that the pcie pll takes to lock
PCIERXPLL_LOCKED (R)	8	0x0	lock status

PCIERXPLL_DEBUG1 - RW - 32 bits - DPCD_VGA:0x81230			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_DBGBUS_SEL	4:0	0x0	Select which values are sent on PCIe Debug bus
PCIERXPLL_DBGBUS_LANESEL	7:5	0x0	Select which lane is sent to debug bus
PCIERXPLL_DBG1_DUMMY	31:8	0x0	Dummy register reserved for future use

Debug register 1

PCIERXPLL_DEBUG2 - RW - 32 bits - DPCD_VGA:0x81234			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_DBG2_DUMMY	31:0	0x0	Dummy register reserved for future use

Debug register 2

PCIERXPLL_BIST_CH_EN - RW - 8 bits - DPCD_VGA:0x81238			
Field Name	**Bits**	**Default**	**Description**
BIST_CH_EN	5:0	0x0	Channel enable for BIST test

PCIERXPLL_BIST_MODE - RW - 8 bits - DPCD_VGA:0x81239			
Field Name	**Bits**	**Default**	**Description**
BIST_MODE	1:0	0x0	Bist mode 0=Toggle pattern 1=PRBS10 2=PRBS7 (DisplayPort) 3=PRBS23

PCIERXPLL_BIST_OVERRIDE_CRCTRL - RW - 8 bits - DPCD_VGA:0x8123A			
Field Name	**Bits**	**Default**	**Description**
BIST_OVERRIDE_CRCTRL	0	0x0	Override CRCTRL from macro

PCIERXPLL_BIST_DEBUG_SEL - RW - 8 bits - DPCD_VGA:0x8123B			
Field Name	**Bits**	**Default**	**Description**
BIST_DEBUG_SEL	5:0	0x0	Selects lane to debug

PCIERXPLL_BIST_LOOPDBG_SEL - RW - 8 bits - DPCD_VGA:0x8123C			
Field Name	**Bits**	**Default**	**Description**
BIST_LOOPDBG_SEL	2:0	0x0	Selects loop infor debug

PCIERXPLL_BIST_CRCTRL_VAL - RW - 8 bits - DPCD_VGA:0x8123D			
Field Name	**Bits**	**Default**	**Description**
BIST_CRCTRL_VAL	6:0	0x0	CRCTRL override value

PCIERXPLL_BIST_PHASEOUT_SEL - RW - 8 bits - DPCD_VGA:0x8123E			
Field Name	**Bits**	**Default**	**Description**
BIST_PHASEOUT_SEL	4:0	0x0	Select lane to output oPHASE data

PCIERXPLL_BIST_NCYCLE - RW - 8 bits - DPCD_VGA:0x8123F			
Field Name	**Bits**	**Default**	**Description**
BIST_NCYCLE	7:0	0x0	Duration of Phase iteration

PCIERXPLL_BIST_DPHASE - RW - 8 bits - DPCD_VGA:0x81240			
Field Name	**Bits**	**Default**	**Description**
BIST_DPHASE	5:0	0x0	Eye width threshold for test pass

PCIERXPLL_BIST_TEST - RW - 8 bits - DPCD_VGA:0x81241			
Field Name	**Bits**	**Default**	**Description**
BIST_TEST	0	0x0	Select second widest eye open for measure

PCIERXPLL_BIST_ENABLE - RW - 8 bits - DPCD_VGA:0x81242			
Field Name	**Bits**	**Default**	**Description**
BIST_ENABLE	0	0x0	Enable test

PCIERXPLL_BIST_REGCTL - RW - 8 bits - DPCD_VGA:0x81243			
Field Name	**Bits**	**Default**	**Description**
BIST_REGCTL	0	0x0	Use Register based control for BIST instead of JTAG.

PCIERXPLL_BIST_DATA - RW - 16 bits - DPCD_VGA:0x81244			
Field Name	**Bits**	**Default**	**Description**
BIST_RESPONSE (R)	0	0x0	Debug output from pcie io bist
BIST_PASS (R)	1	0x0	Debug output from pcie io bist
BIST_TIMEOUT (R)	2	0x0	Debug output from pcie io bist
BIST_PHASEOUT1 (R)	8:3	0x0	Debug output from pcie io bist
BIST_PHASEOUT2 (R)	14:9	0x0	Debug output from pcie io bist
BIST_DUMMY15 (R)	15	0x0	Debug output from pcie io bist

PCIERXPLL_BIST_DBG - RW - 16 bits - DPCD_VGA:0x81246			
Field Name	**Bits**	**Default**	**Description**
BIST_DBG (R)	15:0	0x0	Debug output from pcie io bist

PCIERXPLL_P_B1X_CLK_DIV_CTRL - RW - 32 bits - DPCD_VGA:0x81254			
Field Name	**Bits**	**Default**	**Description**
DISABLE_P_B1X_CLK_DIV	0	0x0	Disables the divide by 2 clock divider in 1.7Gb/s mode 0=Enable Divide by 2 selection 1=Always select divide by 1

Core clock divider control

PCIERXPLL_IMPCTRL - RW - 32 bits - DPCD_VGA:0x81260			
Field Name	**Bits**	**Default**	**Description**
REG_RX_IMPVAL_OVERRIDE	12:0	0x7f	override impedance value
OVERRIDE_IMPVAL	13	0x0	override impedance value enable

PCIERXPLL_IMPVAL_STATUS - RW - 32 bits - DPCD_VGA:0x81264			
Field Name	**Bits**	**Default**	**Description**
RX_IMPVAL_READ (R)	12:0	0x7f	
RECAL_READ (R)	16	0x0	

PCIERXPLL_PM_DBG_SEL - RW - 8 bits - DPCD_VGA:0x81268			
Field Name	**Bits**	**Default**	**Description**
PCIERXPLL_PM_DBG_SEL	7	0x0	pcie rx pll debug bus selection

pcie rx pll debug bus selection

control - RW - 32 bits - DPCD_VGA:0x82000			
Field Name	**Bits**	**Default**	**Description**
enable	0	0x1	Enable the Display FIFO. When not enabled the FIFO ignores data from the link layer. 0=false 1=true
ppll_pwrup_done_bypass	4	0x0	By default, the DFIFO will not start until the Display PLL is locked and the clock is switched to the PLL clock; this bit bypasses this logic and starts the DFIFO whenever video data is present from the main-link 0=false 1=true
start_on_newline	8	0x1	Determines if the DFIFO starts at the newline or newframes 0=newframe 1=newline
average_on_active_lines_only	12	0x1	When set, the DFIFO only averages on active lines; if not set, the DFIFO averages the FIFO level during the VBLANK period, using the maximum FIFO level from the last active line 0=false 1=true
noadj_at_vblank	16	0x0	When set, DFIFO does not adjust while in v-blank period 0=false 1=true

Control Register

alpha_denom_exp - RW - 32 bits - DPCD_VGA:0x82004			
Field Name	**Bits**	**Default**	**Description**
alpha_denom_exp	2:0	0x4	range: 0-6 ; the average is determined by avg(t) = (1-alpha) * avg(t-1) + alpha * sample(t) where alpha = ((2^alpha_denom_exp)-1)/(2^alpha_denom_exp)

alpha denominator exponent

noadjust_line_threshold - RW - 32 bits - DPCD_VGA:0x82008			
Field Name	**Bits**	**Default**	**Description**
noadjust_line_threshold	16:0	0x10	This value determines how many lines must have processed before the RCA is free to make a frequency adjustment

No-adjust Line Threshold

getmaxlevel_cycles - RW - 32 bits - DPCD_VGA:0x8200C			
Field Name	**Bits**	**Default**	**Description**
getmaxlevel_cycles	7:0	0x40	This value is the number of cycles after startup the FIFO level is measured to determine the FIFO initial condition

Cycles to get estimate of inititial FIFO level

fifo_level - RW - 32 bits - DPCD_VGA:0x82014			
Field Name	**Bits**	**Default**	**Description**
trigger_level	7:0	0x7f	This is the level the FIFO must reach before the FIFO allows the display-controller to start draining it; this value is typically set to the middle of the FIFO
rail	23:16	0x4	This is the the amount the FIFO level is allowed to drift before an adjustment is made
course_rail	31:24	0xff	This is the the amount the FIFO level is allowed to drift before an adjustment is immediately made

FIFO Level Controls

adjust - RW - 32 bits - DPCD_VGA:0x8201C			
Field Name	**Bits**	**Default**	**Description**
adjust_fraction_exp	2:0	0x2	This value represents the fraction exponent, in 1/(2^n), of the calculated multiplier descrepency; the multiplier is adjusted by (1 + 1/(2^n2)) to over-correct the descrepency to move the display FIFO towards the target level

Reference clock adjustment control

locking_control - RW - 32 bits - DPCD_VGA:0x82020			
Field Name	**Bits**	**Default**	**Description**
lock_milestone	4:0	0xa	The lock count is incremented everytime a milstone less-than-or-equal-to this value is reached

Control for generating locked flag

lock_count - RW - 32 bits - DPCD_VGA:0x82024			
Field Name	**Bits**	**Default**	**Description**
lock_count (R)	27:0	0x0	This is the lock count value within the dfifo

Lock Count

overflow_count - RW - 32 bits - DPCD_VGA:0x82028			
Field Name	**Bits**	**Default**	**Description**
overflow_count	5:0	0x0	This counter keeps track of the number of overflows that have occurred in the DFIFO

Overflow Count

underflow_count - RW - 32 bits - DPCD_VGA:0x8202C			
Field Name	**Bits**	**Default**	**Description**
underflow_count	5:0	0x0	This counter keeps track of the number of underflows that have occurred in the DFIFO

Underflow Count

average_fifo_level - RW - 32 bits - DPCD_VGA:0x82030			
Field Name	**Bits**	**Default**	**Description**
average_fifo_level (R)	7:0	0x0	This value is the average FIFO level

FIFO's Average Level

lock_count_threshold - RW - 32 bits - DPCD_VGA:0x82034			
Field Name	**Bits**	**Default**	**Description**
lock_count_threshold	27:0	0x8	The locked flag is activated when the lock_count is greater-than-or-equal-to this value

Lock Count Threshold

irq_raw_status - RW - 32 bits - DPCD_VGA:0x82040			
Field Name	**Bits**	**Default**	**Description**
irq_overflow (R)	0	0x0	High if the DFIFO overflow counter is non-zero 0=inactive 1=active
irq_underflow (R)	1	0x0	High if the DFIFO underflow counter is non-zero 0=inactive 1=active
irq_locked (R)	2	0x0	High if the DFIFO has locked the Pixel and Link-Symbol clock frequencies 0=inactive 1=active

Interrupt Raw Status

irq_enable - RW - 32 bits - DPCD_VGA:0x82044			
Field Name	**Bits**	**Default**	**Description**
irq_enable_overflow	0	0x0	Enables overflow interrupt 0=disable 1=enable
irq_enable_underflow	1	0x0	Enables underflow interrupt 0=disable 1=enable
irq_enable_locked	2	0x0	Enables interrupt on DFIFO lock 0=disable 1=enable

Interrupt Enable

irq_status - RW - 32 bits - DPCD_VGA:0x82048			
Field Name	**Bits**	**Default**	**Description**
irq_status_overflow (R)	0	0x0	High if the overflow interrupt is active and enabled 0=inactive 1=active
irq_status_underflow (R)	1	0x0	High if the underflow interrupt is active and enabled 0=inactive 1=active
irq_status_locked (R)	2	0x0	High if the locked interrupt is active and enabled 0=inactive 1=active

Interrupt Status of Enabled Interrupts

sca_offset - RW - 32 bits - DPCD_VGA:0x82050			
Field Name	**Bits**	**Default**	**Description**
sca_offset (R)	31:0	0x0	the DFIFO calculated stream clock adjust offset value; this is the value the DFIFO is adding to the specified clock_multiplier to match the input and output stream clocks of the DFIFO

Stream Clock Adjust Offset

dfifo_debug - RW - 32 bits - DPCD_VGA:0x82054			
Field Name	**Bits**	**Default**	**Description**
dbgmux_sel	3:0	0xf	Select the output to the debug mux
sparebits	31:4	0xfff0000	ECO bits

Debug Register

dfifo_mem_read_margin - RW - 32 bits - DPCD_VGA:0x82074			
Field Name	**Bits**	**Default**	**Description**
mem_read_margin	3:0	0x0	Read margin setting
mem_read_margin_enable	4	0x0	Enable read margin control

Read margin control

EXTx_PPLL_REF_DIV_SRC - RW - 32 bits - DPCD_VGA:0x83000			
Field Name	**Bits**	**Default**	**Description**
EXTx_PPLL_REF_DIV_SRC	2:0	0x1	Determines clock source of reference divider 0=PCIE_REFCLK 1=XTALIN 2=GENERICA 3=GENERICB 4=HSYNCA 5=HSYNCB 6=VPCLK 7=DVOCLK0

Determines clock sources for the reference divider of primary pixel clock PLL in extended timing mode

EXTx_PPLL_REF_DIV - RW - 32 bits - DPCD_VGA:0x83004			
Field Name	**Bits**	**Default**	**Description**
EXTx_PPLL_REF_DIV	9:0	0x1	Determines the pixel clock reference divider, 0x0 = reserved(bypass divider) 0x1 = bypass divider 0x2 = divide by 2 ... 0x3ff = divide by 1023
EXTx_PPLL_CALIBRATION_REF_DIV	15:12	0x4	reference divider value during calibration

Reference divider value for primary pixel clock PLL in extended timing mode

EXTx_DIFF_POST_DIV_CNTL - RW - 32 bits - DPCD_VGA:0x83010			
Field Name	**Bits**	**Default**	**Description**
EXTx_DIFF_DRIVER_ENABLE	10:8	0x0	Enables the driver for the differential direct clock for LVTM and UNIPHY link B. 0=both disabled 1=differential clock for LVTM is disabled, differential clock for UNIPHY link B enabled when the DIGB block is enabled 2=differential clock for LVTM is enabled when DIGB is enabled, differential clock for UNIPHY link B is disabled 3=both enabled when DIGB is enabled

Controls the P2PLL new differential post divider for the direct clock

EXTx_PPLL_FB_DIV - RW - 32 bits - DPCD_VGA:0x83014			
Field Name	**Bits**	**Default**	**Description**
EXTx_PPLL_FB_DIV_FRACTION_CNTL	5:4	0x1	Fractional feedback divider slip request control 0=00 - Slip_req/Slip_ack handshake 1=01 - Slip once every 1 clocks (ignore slip_ack) 2=10 - Slip once every 2 clocks (ignore slip_ack) 3=11 - Slip once every 4 clocks (ignore slip_ack)

Feedback divider values for secondary pixel clock PLL in extended timing mode

EXTx_PPLL_FB_DIVIDER - RW - 32 bits - DPCD_VGA:0x83018			
Field Name	**Bits**	**Default**	**Description**
EXTx_PPLL_FB_DIVIDER_FRACTION	19:0	0x0	The fractional part of the divider: fraction/2^20
EXTx_PPLL_FB_DIVIDER_INTEGER	31:20	0x80	The integer part of the divider

Feedback divider values for secondary pixel clock PLL

EXTx_PPLL_POST_DIV - RW - 32 bits - DPCD_VGA:0x8301C			
Field Name	**Bits**	**Default**	**Description**
EXTx_PPLL_POST_DIV	6:0	0x6	Post divider value of display PLL. 0x0 - 0x1 = reserved (divide PLL output by 2) 0x2 = divide PLL output by 2 0x3 = divide PLL output by 3 0x4 = divide PLL output by 4 0x5 = divide PLL output by 5 ... 0x7f = divide PLL output by 127

Post divider value of secondary pixel clock PLL in extended timing mode

EXTx_PPLL_CNTL - RW - 32 bits - DPCD_VGA:0x83020			
Field Name	**Bits**	**Default**	**Description**
EXTx_PPLL_CTL	4:0	0x4	Used to program VCO gain settings. PPLL_CTL[4] = 0 - the four calibration bits are set by the calibration loop. PPLL_CTL[4] = 1 - The four calibration bits are set by CTL[3:0]
EXTx_PPLL_LF_MODE	15:7	0xe8	PLL loop filter mode settings
EXTx_PPLL_CP	23:16	0x7	PLL charge pump current adjustment.
EXTx_PPLL_IBIAS	31:24	0x15	PLL current bias adjustment

Controls the secondary pixel clock PLL

PxPLL_CNTL - RW - 32 bits - DPCD_VGA:0x83024			
Field Name	**Bits**	**Default**	**Description**
PxPLL_RESET	0	0x0	Reset digital logic inside PLL 0=no reset 1=PLL reset
PxPLL_SLEEP	1	0x0	Power down analog logic inside PLL 0=PLL runs 1=PLL powerdown
PxPLL_BYPASS_CAL	2	0x0	Bypass PLL calibration phase 0=do not bypass calibration 1=bypass calibration. Causes PxPLL_CALIB_DONE & PxPLL_LOCKED signals to go high after reset is asserted low
PxPLL_ITMONEN	3	0x0	Turns on transmission gates that lead to various internal critical nodes 0=transmission gates are off 1=turn on transmission gates
PxPLL_VCOREF	5:4	0x0	PLL VCO input reference voltage setting
PxPLL_FB_CLK_DIV_2	6	0x0	FB clock is pll/2
PxPLL_POST_CLK_DIV_2	7	0x0	PostDiv clock is pll/2
PxPLL_CALREF	9:8	0x0	PLL's 2nd VCO input reference voltage setting
PxPLL_CAL_BYPASS_REFDIV	10	0x0	Determines which clock will go to the calibration logic and VCO during calibration 0=do not bypass reference divider (XTALIN/2 during calibration) 1=bypass reference divider (XTALIN during calibration)
PxPLL_CORE_REFCLK_DISABLE	11	0x0	Gates off core_refclk supplied to post,feedback and reference divider 0=CORE_REFCLK to fb_divider and post_divider enabled 1=CORE_REFCLK to fb_divider and post_divider gated off
PxPLL_ANTI_GLITCH_RESET	13	0x0	Anti-Glitch Reset Control 0=No reset 1=Anti-glitch logic reset
PxPLL_POWERUP_DONE (R)	15	0x0	Indicates if pll power down sequence is complete 0=PLL power down sequence is not done 1=PLL power down sequence is done
PxPLL_PDIVCLK_SEL	18:17	0x0	
PxPLL_LOCK_FREQ_SEL	19	0x0	Selects pll lock frequency range 0=600-1200MHz 1=?Lower Lock Range

PxPLL_CNTL - RW - 32 bits - DPCD_VGA:0x83024			
Field Name	**Bits**	**Default**	**Description**
PxPLL_CALIB_DONE (R)	20	0x0	Indicates that the PLL has completed its calibration 0=PLL calibration is not done 1=PLL calibration is done
PxPLL_LOCKED (R)	21	0x0	Indicates that the PLL has locked. This signal reuses the calibration logic counter to count to 100us, the period it takes the PLL to lock 0=PLL is not locked 1=PLL is locked
PxPLL_LVTMCLK_PDIVSEL	23:22	0x0	Source of lvtmclk
PxPLL_PDIV2_SRC	25:24	0x1	Source of divide by 2 block
PxPLL_DBGCLK_SEL	28:26	0x0	Debug clock selector
PxPLL_PIXCLK_PDIVSEL	30:29	0x0	Source of the pixlk

Controls primary pixel clock PLL

PxPLL_INT_SS_DELAY - RW - 32 bits - DPCD_VGA:0x8302C			
Field Name	**Bits**	**Default**	**Description**
PxPLL_SS_DELAY	7:0	0x0	This is the PLL feedback update delay; This should be left at zero

Cntrols the delay between updates in the Pll

PxPLL_DS_CNTL - RW - 32 bits - DPCD_VGA:0x83034			
Field Name	**Bits**	**Default**	**Description**
PxPLL_DS_ORDER	17:16	0x1	Delta-Sigma modulator order
PxPLL_DS_MODE	18	0x0	Delta-Sigma mode: 0 - fractional, 1 - integer
PxPLL_DS_PRBS_EN	19	0x0	Delta-Sigma PRBS enable: 0 - no PRBS, 1 - apply PRBS on delta-sigma input

P2PLL Delta-Sigma modulator control

PxPLL_VREG_CNTL - RW - 32 bits - DPCD_VGA:0x83038			
Field Name	**Bits**	**Default**	**Description**
PxPLL_VREG_LPF_C	3:0	0x0	Voltage regulator bandwidth capacitor control
PxPLL_VREG_LPF_R	7:4	0x0	Voltage regulator bandwidth resistor control
PxPLL_VREG_PG_BIT	12:8	0x0	Voltage regulator pass-gate control
PxPLL_VREG_TRIM	16:13	0x0	Voltage regulator output voltage fine control
PxPLL_VREG_FILTER	21:20	0x0	Control bits for regulator's output filter
PxPLL_VREG_BIAS	27:24	0x0	Control bits for regulator's bias circuit
PxPLL_VREG_RESET	28	0x0	Reset bit for regulator
PxPLL_VREG_POWER_DOWN	29	0x0	Power down bit for regulator

Pixel PLL voltage regulator control

PxPLL_DEBUG - RW - 32 bits - DPCD_VGA:0x8303C			
Field Name	**Bits**	**Default**	**Description**
PxPLL_DEBUG_MUX_SELECT (W)	1:0	0x0	Select which signals go to core debug mux.
PxPLL_DEBUG_MUXOUT (R)	31:16	0x0	debug output from pll.

PxPLL_MISC_CNTL - RW - 32 bits - DPCD_VGA:0x83040			
Field Name	**Bits**	**Default**	**Description**
PxPLL_DIRECT_RUNCLOCK	0	0x0	Gater for PCLK DIRECT
PxPLL_DIRECT_SRCSEL	1	0x0	Source Selection for PCLK DIRECT
PxPLL_DISP_CLK_PDIV	8:2	0x0	Pst Divider
PxPLL_DISP_CLK_PDIVSEL	10:9	0x0	Source of DISPCLK
PxPLL_DVOCLK_PDIVSEL	12:11	0x0	Source of DVOCLK
PxPLL_PDIV_HSYNC	19:13	0x0	Post Divider
PxPLL_REFCLK_SELECT	20	0x1	Choose source for PPLL_REFCLK output
PxPLL_SYMCLK_PDIV	27:21	0x0	Post Divider
PxPLL_SYMCLK_PDIVSEL	29:28	0x0	Source of PDIVSEL
PxPLL_HSYNC	30	0x0	HSYNC to pixel clock divider (Post divider)
PxPLL_FB_SLIPREQ_WAIT	31	0x0	Reserved

Misc control registers

PxPLL_MISC2_CNTL - RW - 32 bits - DPCD_VGA:0x83044			
Field Name	**Bits**	**Default**	**Description**
PxPLL_SEL_SPARE	3:0	0x0	Reserved
PxPLL_VCO_GAIN	5:4	0x0	Reserved for VCO gain control
PxPLL_CNTL	15:6	0x0	Reserved
PxPLL_HALFGM_EN	16	0x0	Enable Half-GM Gain option for Input2 OTA
DCCG_DEBUG_MUX_SELECT	20:17	0x0	DPLL Debug signal MUXOUT[15:0] source selection
DCCG_DEBUG_SIGNAL_EN	21	0x0	Enable DPLL Debug signal output
PxPLL_CAL_MODE	27:23	0x0	Reserved

Misc. Control

PxPLL_DTO_UNLOCK_CNTL - RW - 32 bits - DPCD_VGA:0x83048			
Field Name	**Bits**	**Default**	**Description**
PxPLL_DTO	8:0	0x0	DTO block control
PxPLL_DTO_DIS	9	0x1	DTO block disable: 1'b0 = Enable DISPCLK DTO 1'b1 = Disable DISPCLK DTO
PxPLL_DTO_UPDATE_REQ	10	0x0	DTO block setting update request: 1'b0 = no DTO update 1'b1 = DTO update request pending
PxPLL_UNLOCK_DET_COUNT	14:12	0x0	Unlock detector control
PxPLL_UNLOCK_DET_EN	15	0x0	Unlock detector enable
PxPLL_UNLOCK_DET_RES100	16	0x0	Unlock detector resolution control

DTO Control

PxPLL_SS_CTRL1 - RW - 32 bits - DPCD_VGA:0x8304C			
Field Name	**Bits**	**Default**	**Description**
PxPLL_SS_EN	0	0x0	Spread spectrum mode enable: 1'b0 = disable spread spectrum 1'b1 = enable spread spectrum
PxPLL_SS_SINGLE_STEP_SEL	1	0x0	Single step test clock selection (DTV feature): 1'b0 = Select GENERICA 1'b1 = Select PCIE_REFCLK
PxPLL_SS_MODE	2	0x0	Spread spectrum mode select: 1'b0 = centre spread 1'b1 = down spread

PxPLL_SS_CTRL1 - RW - 32 bits - DPCD_VGA:0x8304C			
Field Name	**Bits**	**Default**	**Description**
PxPLL_SS_AMOUNT_NFRAC_SLIP	7:4	0x0	Spread spectrum amount fractional setting
PxPLL_SS_AMOUNT_FBDIV	15:8	0x0	Spread spectrum amount setting
PxPLL_SS_STEP_SIZE_DSFRAC	31:16	0x0	Spread spectrum step size DS control

Spread Spectrum Control

PxPLL_SS_CTRL2 - RW - 32 bits - DPCD_VGA:0x83050			
Field Name	**Bits**	**Default**	**Description**
PxPLL_SS_AMOUNT_DSFRAC	15:0	0x0	Spread spectrum amount DS setting

Spread Spectrum Control

PxPLL_FB_FORCE1 - RW - 32 bits - DPCD_VGA:0x83054			
Field Name	**Bits**	**Default**	**Description**
PxPLL_ENABLE_FB_FORCE	0	0x0	enable force mode
PxPLL_FORCE_ATOMIC_UPDATE_W	1	0x0	update request
PxPLL_FORCE_ATOMIC_UPDATE_R (R)	2	0x0	update ack

Force the FB divder values from registers

PxPLL_FB_FORCE2 - RW - 32 bits - DPCD_VGA:0x83058			
Field Name	**Bits**	**Default**	**Description**
PxPLL_FORCE_DS_FRAC	15:0	0x0	force value for ds frac
PxPLL_FORCE_FBDIV	27:16	0x0	force value for fbdiv
PxPLL_FORCE_FBDIV_FRACTION	31:28	0x0	force value for fbdiv_fraction

Force the FB divider values from registers

DISPC_TEST_PATTERN_CONTROL - RW - 32 bits - DPCD_VGA:0x84000			
Field Name	**Bits**	**Default**	**Description**
DISPC_TEST_PATTERN_EN	0	0x0	Set to 1 to enable the test pattern 0=selects scaler output 1=selects test pattern output
DISPC_TEST_PATTERN_MODE	10:8	0x0	Selects the type of test pattern 0=color blocks RGB 1=color blocks YCbCr-601 2=color blocks YCbCr-709 3=vertical bars 4=horizontal bars 5=single ramp RGB 6=dual ramp RGB 7=reserved
DISPC_TEST_PATTERN_DYNAMIC_RANGE	16	0x0	Selects the dynamic range, only in RGB color blocks mode 0=VESA range 1=CEA range

DISPC_TEST_PATTERN_CONTROL - RW - 32 bits - DPCD_VGA:0x84000			
Field Name	**Bits**	**Default**	**Description**
DISPC_TEST_PATTERN_COLOR_FORMAT	31:24	0x0	Selects the color format in modes 0,1,2 (color blocks) 0=6 BPC (not valid for YCbCr) 1=8 BPC 2=10 BPC 3=reserved

Test Pattern Controls

DISPC_TEST_PATTERN_PARAMETERS - RW - 32 bits - DPCD_VGA:0x84004			
Field Name	**Bits**	**Default**	**Description**
DISPC_TEST_PATTERN_INC0	3:0	0x0	Used in mode 5 and 6 (single and dual ramp) to determine the step in the first ramp, the step is exp(2, CRTCx_TEST_PATTERN_INC0) LSBs in 16 bit per component, so for example a 6 should be programmed to have a 1 LSB in 10 bpc
DISPC_TEST_PATTERN_INC1	7:4	0x0	Used in mode 6 (dual ramp) to determine the step in the second ramp, the step is exp(2, CRTCx_TEST_PATTERN_INC0) LSBs in 16 bit per component, so for example a 6 should be programmed to have a 1 LSB in 10 bpc
DISPC_TEST_PATTERN_VRES	11:8	0x0	Used to determine the dimentions of the ramp and color block test patterns. Height is exp (2, CRTCx_TEST_PATTERN_VRES)
DISPC_TEST_PATTERN_HRES	15:12	0x0	Used to determine the dimentions of the ramp and color block test patterns. width is exp (2, CRTCx_TEST_PATTERN_HRES)
DISPC_TEST_PATTERN_RAMP0_OFFSET	31:16	0x0	Used in mode 5 and 6 (single and dual ramp) to determine the starting offset in the first ramp (the starting offset in the second ramp is zero)ed in mode 5 and 6 (single and dual ramp) to determine the starting offset in the first ramp (the starting offset in the second ramp is zero). Uses a 16 bit -MSB aligned- representation of the color. NOTE: Bits 0:5 of this field are hardwired to ZERO.

Test Pattern Parameters

DISPC_TEST_PATTERN_COLOR_MASK - RW - 32 bits - DPCD_VGA:0x84008			
Field Name	**Bits**	**Default**	**Description**
DISPC_TEST_PATTERN_MASK	5:0	0x0	Used to select which colors are loaded with DxCRTC_TEST_PATTERN_DATA. mask is: B1, G1, R1, B0, G0, R0

Test Pattern Color Mask

DISPC_SW_TOTAL_H_TIME - RW - 32 bits - DPCD_VGA:0x8400C			
Field Name	**Bits**	**Default**	**Description**
DISPC_SW_TOTAL_H_TIME	15:0	0x0	Total Pixels in a line including blank pixels

User Specified Total Pixels in a Line

DISPC_SW_TOTAL_V_TIME - RW - 32 bits - DPCD_VGA:0x84010			
Field Name	**Bits**	**Default**	**Description**
DISPC_SW_TOTAL_V_TIME	15:0	0x0	Total lines in a frame including blank lines

User Specified Total Lines in a Frame

DISPC_SW_ACTIVE_H_TIME - RW - 32 bits - DPCD_VGA:0x84014			
Field Name	**Bits**	**Default**	**Description**
DISPC_SW_ACTIVE_H_TIME	15:0	0x0	Active Video Width in pixels

User Specified Active Video Width

DISPC_SW_ACTIVE_V_TIME - RW - 32 bits - DPCD_VGA:0x84018			
Field Name	**Bits**	**Default**	**Description**
DISPC_SW_ACTIVE_V_TIME	15:0	0x0	Active Video Height in lines

User Specified Active Video Height

DISPC_SW_ACTIVE_H_START_TIME - RW - 32 bits - DPCD_VGA:0x8401C			
Field Name	**Bits**	**Default**	**Description**
DISPC_SW_ACTIVE_H_START_TIME	15:0	0x0	Horizontal start time of active video from the leading edge of Hsync in pixels

User Specified Horizontal Start Time of Active Video

DISPC_SW_ACTIVE_V_START_TIME - RW - 32 bits - DPCD_VGA:0x84020			
Field Name	**Bits**	**Default**	**Description**
DISPC_SW_ACTIVE_V_START_TIME	15:0	0x0	Vertical start time of active video from the leading edge of Vsync in lines

User Specified Vertical Start Time of Active Video

DISPC_SW_HSYNC_TIME - RW - 32 bits - DPCD_VGA:0x84024			
Field Name	**Bits**	**Default**	**Description**
DISPC_SW_HSYNC_TIME	14:0	0x0	Hsync width in pixels
DISPC_SW_HSYNC_POLARITY	15	0x0	Sync signal active edge 0=Active High 1=Active Low

User Specified Hsync Width and Polarity

DISPC_SW_VSYNC_TIME - RW - 32 bits - DPCD_VGA:0x84028			
Field Name	**Bits**	**Default**	**Description**
DISPC_SW_VSYNC_TIME	14:0	0x0	Vsync width in lines
DISPC_SW_VSYNC_POLARITY	15	0x0	Sync signal active edge 0=Active High 1=Active Low

User Specified Vsync Width and Polarity

DISPC_CONTROL - RW - 32 bits - DPCD_VGA:0x8402C			
Field Name	**Bits**	**Default**	**Description**
DISPC_BLANK_ACTIVE_DISPLAY_ENABLE	0	0x0	Active Display blanks screen with DISPC_BLACK_PIXEL 0=Disable 1=Enable
DISPC_FORCE_ENABLE	4	0x0	Forces Enable Fsm into the Enable State 0=Disable 1=Enable
DISPC_FORCE_DISABLE	5	0x0	Forces Enable Fsm into the Disable State 0=Disable 1=Enable
DISPC_HW_TIMING_PARAMS_UNCHANGED_TIME	11:8	0x0	The Display Port MSA Timing Parameters must remain the same DISPC_HW_TIMING_PARAMS_UNCHANGED_TIME times in a row before being loaded into the Hardware timing parameters. Load a zero to update instantly.
DISPC_SW_TIMING_PARAMS_UPDATE_INSTANTLY	12	0x0	Instantly updates Software Timing Parameters

DISPC_HW_TOTAL_H_TIME - R - 32 bits - DPCD_VGA:0x84030			
Field Name	**Bits**	**Default**	**Description**
DISPC_HW_TOTAL_H_TIME	15:0	0x0	Total Pixels in a line including blank pixels

Display Port MSA Total Pixels in a Line

DISPC_HW_TOTAL_V_TIME - R - 32 bits - DPCD_VGA:0x84034			
Field Name	**Bits**	**Default**	**Description**
DISPC_HW_TOTAL_V_TIME	15:0	0x0	Total lines in a frame including blank lines

Display Port MSA Total Lines in a Frame

DISPC_HW_ACTIVE_H_TIME - R - 32 bits - DPCD_VGA:0x84038			
Field Name	**Bits**	**Default**	**Description**
DISPC_HW_ACTIVE_H_TIME	15:0	0x0	Active Video Width in pixels

Display Port MSA Active Video Width

DISPC_HW_ACTIVE_V_TIME - R - 32 bits - DPCD_VGA:0x8403C			
Field Name	**Bits**	**Default**	**Description**
DISPC_HW_ACTIVE_V_TIME	15:0	0x0	Active Video Height in lines

Display Port MSA Active Video Height

DISPC_HW_ACTIVE_H_START_TIME - R - 32 bits - DPCD_VGA:0x84040			
Field Name	**Bits**	**Default**	**Description**
DISPC_HW_ACTIVE_H_START_TIME	15:0	0x0	Horizontal start time of active video from the leading edge of Hsync in pixels

Display Port MSA Horizontal Start Time of Active Video

DISPC_HW_ACTIVE_V_START_TIME - R - 32 bits - DPCD_VGA:0x84044			
Field Name	**Bits**	**Default**	**Description**
DISPC_HW_ACTIVE_V_START_TIME	15:0	0x0	Vertical start time of active video from the leading edge of Vsync in lines

Display Port MSA Vertical Start Time of Active Video

DISPC_HW_HSYNC_TIME - R - 32 bits - DPCD_VGA:0x84048			
Field Name	**Bits**	**Default**	**Description**
DISPC_HW_HSYNC_TIME	14:0	0x0	Hsync width in pixels
DISPC_HW_HSYNC_POLARITY	15	0x0	Sync signal active edge 0=Active High 1=Active Low

Display Port MSA Hsync Width and Polarity

DISPC_HW_VSYNC_TIME - R - 32 bits - DPCD_VGA:0x8404C			
Field Name	**Bits**	**Default**	**Description**
DISPC_HW_VSYNC_TIME	14:0	0x0	Vsync width in lines
DISPC_HW_VSYNC_POLARITY	15	0x0	Sync signal active edge 0=Active High 1=Active Low

Display Port MSA Vsync Width and Polarity

DISPC_SYNC_CONTROL - RW - 32 bits - DPCD_VGA:0x84050			
Field Name	**Bits**	**Default**	**Description**
DISPC_HSYNC_SET	0	0x0	Hsync value is driven high 0=Normal Operation 1=HSYNC Pin driven high
DISPC_HSYNC_CLEAR	1	0x0	Hsync value is driven low 0=Normal Operation 1=HSYNC Pin driven low
DISPC_HSYNC_INVERT	2	0x0	Hsync value is inverted. 0=Normal Operation 1=Invert the Vsync Value
DISPC_COMPOSITE_HSYNC_ENABLE	3	0x0	Enable Composite Hsync 0=Disable 1=Enable
DISPC_VSYNC_SET	8	0x0	Vsync value is driven high 0=Normal Operation 1=VSYNC Pin driven high
DISPC_VSYNC_CLEAR	9	0x0	Vsync value is driven low 0=Normal Operation 1=VSYNC Pin driven low
DISPC_VSYNC_INVERT	10	0x0	Vsync value is inverted. 0=Normal Operation 1=Invert the Vsync Value
DISPC_COUNT_SNAPSHOT (W)	12	0x0	Take a snapshot of the current count value
DISPC_RESET_FRAME_COUNT (W)	13	0x0	Reset the number of frames
DISPC_FORCE_HCOUNT	14	0x0	Loads the DISPC_FORCE_HCOUNT_DATA into Hcount
DISPC_FORCE_VCOUNT	15	0x0	Loads the DISPC_FORCE_VCOUNT_DATA into Vcount
DISPC_FORCE_INTERLACED_FIELD_ID_ENABLE	16	0x0	Forces the Interlaced Field Id to switch 0=Disable 1=Enable
DISPC_FORCE_INTERLACED_FIELD_ID	17	0x0	Interlace Field to force. 0=BOTTOM 1=TOP
DISPC_INTERLACED_FIELD_ID_POLARITY	18	0x0	Field Polarity for external interlace fields 0=Normal polariyt 1=Inverted Polarity
DISPC_SYNC_DELAY	27:24	0x3	Delays Hsync and Vsync by DISPC_SYNC_DELAY clock cycles. Used to match internal DAC delay.

Control for the generation of the sync signals

DISPC_BLANK_PIXEL - RW - 32 bits - DPCD_VGA:0x84054			
Field Name	**Bits**	**Default**	**Description**
DISPC_BLANK_PIXEL_B	9:0	0x0	Blue data
DISPC_BLANK_PIXEL_G	19:10	0x0	Green data
DISPC_BLANK_PIXEL_R	29:20	0x0	Red data

Pixle Value for Blank Data

DISPC_BLACK_PIXEL - RW - 32 bits - DPCD_VGA:0x84058			
Field Name	**Bits**	**Default**	**Description**
DISPC_BLACK_PIXEL_B	9:0	0x0	Blue data
DISPC_BLACK_PIXEL_G	19:10	0x0	Green data
DISPC_BLACK_PIXEL_R	29:20	0x0	Red data

Pixel Value for Black Data

DISPC_LAST_PIXEL - R - 32 bits - DPCD_VGA:0x8405C			
Field Name	**Bits**	**Default**	**Description**
DISPC_LAST_PIXEL_B	9:0	0x0	Blue data
DISPC_LAST_PIXEL_G	19:10	0x0	Green data
DISPC_LAST_PIXEL_R	29:20	0x0	Red data

Last Pixel Value Displayed

DISPC_VCOUNT_STATUS - R - 32 bits - DPCD_VGA:0x84060			
Field Name	**Bits**	**Default**	**Description**
DISPC_VCOUNT	16:0	0x0	Current line being disiplayed

Current Vcount

DISPC_HCOUNT_STATUS - R - 32 bits - DPCD_VGA:0x84064			
Field Name	**Bits**	**Default**	**Description**
DISPC_HCOUNT	15:0	0x0	Current Pixel being displayed

Current Hcount

DISPC_STATUS - R - 32 bits - DPCD_VGA:0x84068			
Field Name	**Bits**	**Default**	**Description**
DISPC_INTERLACED_ENABLE	0	0x0	Display Port MSA interlaced enable signal 0=Disable 1=Enable
DISPC_INTERLACED_EVEN_LINES	1	0x0	Display Port MSA even lines signal. 0=Odd Lines 1=Even Lines
DISPC_INTELACED_FIELD_ID	2	0x0	Display Port MSA field id 0=Bottom 1=Top
DISPC_INTERNAL_INTERLACED_FIELD_ID	3	0x0	Internally generated field id 0=Bottom 1=Top
DISPC_STATE	6:4	0x0	State of the Enable Fsm 0=DISABLED 1=ENABLED 2=WAIT_FOR_DISABLE
DISPC_HW_TIMING_PARAMS_UPDATE	12	0x0	Display Port MSA values are going to change. Read Clears bit

Status of the Display Controller

DISPC_SW_TIMING_CONTROL - RW - 32 bits - DPCD_VGA:0x8406C			
Field Name	**Bits**	**Default**	**Description**
DISPC_LOAD_SW_TIMING (W)	0	0x0	Loads the DISPC_SW timing registers into internal timing registers 0=No Load 1=Load SW Timing Parameters
DISPC_USE_SW_TIMING	1	0x0	Display Controller uses the DISPC_SW timing parameters 0=Use timing paramters from DP link 1=Use timing parameters from registers
DISPC_SW_INTERLACE_ENABLE	4	0x0	User controlled Interlace enable 0=Disable 1=Enable
DISPC_SW_INTERLACED_EVEN_LINES	5	0x0	User controlled Interlace even lines
DISPC_SW_INTERLACED_FIELD_ID	6	0x0	User Controlled Interlaced field
DISPC_USE_SW_INTERLACED_FIELD_ID	7	0x0	Determine which field ID to use during disable state. 0=Use Field Id from DP link as start up Field ID 1=Use DISPC_SW_INTERLACED_FIELD_ID as start up Field ID

User Control for SW timing

DISPC_ERROR_STATUS - R - 32 bits - DPCD_VGA:0x84070			
Field Name	**Bits**	**Default**	**Description**
DISPC_UNDERFLOW_ERROR	0	0x0	No valid data available
DISPC_INTERLACED_FIELD_ID_ERROR	1	0x0	Field Ids did not toggle or do not match
DISPC_UNEXPECTED_DATA_ERROR	2	0x0	Reached end of line and next pixel was not to a new line pixel
DISPC_HW_TIMING_PARAMS_ERROR	3	0x0	Display Port Timing Parameters changed while block was enabled

Error Status of the Display Controller

DISPC_ERROR_HCOUNT_STATUS - R - 32 bits - DPCD_VGA:0x84074			
Field Name	**Bits**	**Default**	**Description**
DISPC_ERROR_HCOUNT	15:0	0x0	Value of Hcount when the error occured.

Hcount Value of Error Occurance

DISPC_ERROR_VCOUNT_STATUS - R - 32 bits - DPCD_VGA:0x84078			
Field Name	**Bits**	**Default**	**Description**
DISPC_ERROR_VCOUNT	16:0	0x0	Value of Vcount when the error occured.

Vcount Value of Error Occurance

DISPC_ERROR_CONTROL - RW - 32 bits - DPCD_VGA:0x8407C			
Field Name	**Bits**	**Default**	**Description**
DISPC_USE_LAST_PIXEL_ENABLE	0	0x0	DISPC_LAST_PIXEL is used if error occurs 0=Disable 1=Enable
DISPC_CLEAR_ERRORS	1	0x0	Clears all error bits 0=Do not clear errors 1=Clear all errors

Error Control Bits

DISPC_INTERRUPT_CONTROL - RW - 32 bits - DPCD_VGA:0x84080			
Field Name	**Bits**	**Default**	**Description**
DISPC_ERRORS_INT (R)	0	0x0	One of the Display Controller Errors has occured
DISPC_ERRORS_ACK (W)	1	0x0	A write clears the interrupt
DISPC_HW_TIMING_PARAMS_ERROR_INT (R)	2	0x0	Display Port Timing Parameters are changing
DISPC_HW_TIMING_PARAMS_ERROR_ACK (W)	3	0x0	A write clears the interrupt

Interrupt Control

DISPC_FORCE_HCOUNT_DATA - RW - 32 bits - DPCD_VGA:0x84084			
Field Name	**Bits**	**Default**	**Description**
DISPC_FORCE_HCOUNT_DATA	15:0	0x0	Value forced into the Hcount Register

Force Pixel Count

DISPC_FORCE_VCOUNT_DATA - RW - 32 bits - DPCD_VGA:0x84088			
Field Name	**Bits**	**Default**	**Description**
DISPC_FORCE_VCOUNT_DATA	16:0	0x0	Value forced into the Vcount Register

Force Line Count

DISPC_FRAME_COUNT - R - 32 bits - DPCD_VGA:0x8408C			
Field Name	**Bits**	**Default**	**Description**
DISPC_FRAME_COUNT	15:0	0x0	Number of frames

Number of frames

DISPC_DISABLE_POINT_CONTROL - RW - 32 bits - DPCD_VGA:0x84090			
Field Name	**Bits**	**Default**	**Description**
DISPC_DISABLE_POINT	2:0	0x0	Point where the display controller is disabled once enabled. 0=Immidieatly 1=end of hblank 2=end of vsync 3=display blank 4=start of blank 5=h blank 6=v blank

Disable Point of Sync Signals

DISPC_ERROR_MASK - RW - 32 bits - DPCD_VGA:0x84094			
Field Name	**Bits**	**Default**	**Description**
DISPC_UNDERFLOW_ERROR_MASK	0	0x1	Mask DISPC_UNDERFLOW_ERROR 0=UnMask 1=Mask
DISPC_INTERLACED_FIELD_ID_ERROR_MASK	1	0x1	Mask DISPC_INTERLACED_FIELD_ID_ERROR 0=UnMask 1=Mask
DISPC_UNEXPECTED_ERROR_MASK	2	0x1	Mask DISPC_UNEXPECTED_ERROR 0=UnMask 1=Mask
DISPC_HW_TIMING_PARAMS_ERROR_MASK	3	0x1	Mask HW_TIMING_PARAMS_ERROR 0=UnMask 1=Mask

Masks errors from generating an interrupt

DISPC_TEST_PATTERN_COLOR - RW - 32 bits - DPCD_VGA:0x84098			
Field Name	**Bits**	**Default**	**Description**
DISPC_TEST_PATTERN_DATA	15:0	0x0	Used to load the RGB0 and RGB1 colors for the vertical and horizontal test patterns, also using a MSB aligned 16 bit representation of the color NOTE: Bits 0:5 of this field are hardwired to ZERO.

Test Pattern Color

DISPC_DEBUG_MUX_CONTROL - RW - 32 bits - DPCD_VGA:0x841F8			
Field Name	**Bits**	**Default**	**Description**
DISPC_DEBUG_MUX_SELECT	2:0	0x0	Selects different signals to be sent to the core debug mux.

Selects which signals are driven on the debug bus

DISPC_DEBUG - RW - 32 bits - DPCD_VGA:0x841FC			
Field Name	**Bits**	**Default**	**Description**
DISPC_DEBUG	31:0	0x0	Extra bits used for future modes or chicken bits

Spare Registers for chicken bits and future features or ECOs

DAC_ENABLE - RW - 32 bits - DPCD_VGA:0x85000			
Field Name	**Bits**	**Default**	**Description**
DAC_ENABLE	0	0x1	Power On Dac and Enable Sync output 0=Disable 1=Enable

Turn on/off DAC

DAC_CRC_EN - RW - 32 bits - DPCD_VGA:0x85008			
Field Name	**Bits**	**Default**	**Description**
DAC_CRC_EN	0	0x0	Enable signal for DAC CRC 0=Disable 1=Enable
DAC_CRC_CONT_EN	16	0x0	Determines whether CRC is calculated continuously or for one frame (one shot) 0=CRC is calculated over 1 frame 1=CRC is continuously calculated for every frame

DAC CRC enable signals

DAC_CRC_CONTROL - RW - 32 bits - DPCD_VGA:0x8500C			
Field Name	**Bits**	**Default**	**Description**
DAC_CRC_FIELD	0	0x0	Controls which field polarity starts the DAC CRC block after DAC_CRC_EN is set high. Used only for interlaced mode CRCs 0=Odd field begins CRC calculation 1=Even field begins CRC calculation
DAC_CRC_ONLY_BLANKb	8	0x0	Determines whether CRC is calculated for the whole frame or only during non-blank period for DAC 0=CRC calculated over entire field 1=CRC calculated only during BLANKb

DAC CRC controls signals

DAC_CRC_SIG_RGB_MASK - RW - 32 bits - DPCD_VGA:0x85010			
Field Name	**Bits**	**Default**	**Description**
DAC_CRC_SIG_BLUE_MASK	9:0	0x3ff	Mask bits for DAC B channel CRC
DAC_CRC_SIG_GREEN_MASK	19:10	0x3ff	Mask bits for DAC G channel CRC
DAC_CRC_SIG_RED_MASK	29:20	0x3ff	Mask bits for DAC R channel CRC

Mask bits for R, G & B CRC calculations

DAC_CRC_SIG_CONTROL_MASK - RW - 32 bits - DPCD_VGA:0x85014			
Field Name	**Bits**	**Default**	**Description**
DAC_CRC_SIG_CONTROL_MASK	5:0	0x3f	Mask bits for DAC control signal CRC

Mask bits for DAC control signal CRC

DAC_CRC_SIG_RGB - RW - 32 bits - DPCD_VGA:0x85018			
Field Name	**Bits**	**Default**	**Description**
DAC_CRC_SIG_BLUE (R)	9:0	0x3ff	CRC signature value for DAC blue component
DAC_CRC_SIG_GREEN (R)	19:10	0x3ff	CRC signature value for DAC green component
DAC_CRC_SIG_RED (R)	29:20	0x3ff	CRC signature value for DAC red component

DAC CRC R, G & B results

DAC_CRC_SIG_CONTROL - RW - 32 bits - DPCD_VGA:0x8501C			
Field Name	**Bits**	**Default**	**Description**
DAC_CRC_SIG_CONTROL (R)	5:0	0x3f	CRC signature value for DAC control signals

CRC signature value for DAC control signals

DAC_SYNC_TRISTATE_CONTROL - RW - 32 bits - DPCD_VGA:0x85020			
Field Name	**Bits**	**Default**	**Description**
DAC_HSYNC_TRISTATE	0	0x0	DAC hsync tristate. Used to determine hsync enable
DAC_VSYNC_TRISTATE	8	0x0	DAC vsync tristate. Used to determine vsync enable
DAC_SYNC_TRISTATE	16	0x0	DAC sync tristate. Used to determine sync enables

DAC SYNC Tristate control

DAC_AUTODETECT_CONTROL - RW - 32 bits - DPCD_VGA:0x85028			
Field Name	**Bits**	**Default**	**Description**
DAC_AUTODETECT_MODE	1:0	0x0	Operation control of DAC Autodetect logic: 0: No checking 1: Connection checking 2: Disconnection checking
DAC_AUTODETECT_FRAME_TIME_COUNTER	15:8	0x0	If an enabled display pipe is connected to DAC, autodetect logic will count number of frames before DAC comparator enabled.Otherwise, the autodetect logic will count number of 0.1-second units.
DAC_AUTODETECT_CHECK_MASK	18:16	0x7	Mask to select which of the 3 RGB channels will be checked for connection or disconnection. Bit 18: Check R/C channel if bit set to 1. Bit 17: Check G/Y channel if bit set to 1. Bit 16: Check B/Comp channel if bit set to 1.

DAC_AUTODETECT_CONTROL2 - RW - 32 bits - DPCD_VGA:0x8502C			
Field Name	**Bits**	**Default**	**Description**
DAC_AUTODETECT_POWERUP_COUNTER	7:0	0xb	DAC macro Bandgap voltage reference power up time. Default = 11 microseconds.
DAC_AUTODETECT_TESTMODE	8	0x0	0: Normal operation 1: Test mode - count in 1us units

DAC_AUTODETECT_CONTROL3 - RW - 32 bits - DPCD_VGA:0x85030			
Field Name	**Bits**	**Default**	**Description**
DAC_AUTODET_COMPARATOR_IN_DELAY	7:0	0x19	DAC comparator delay for inputs to settle in autodetect mode. Default = 25us
DAC_AUTODET_COMPARATOR_OUT_DELAY	15:8	0x20	DAC comparator delay for outputs to settle in autodetect mode. Default = 5us

DAC_AUTODETECT_STATUS - RW - 32 bits - DPCD_VGA:0x85034			
Field Name	**Bits**	**Default**	**Description**
DAC_AUTODETECT_STATUS (R)	0	0x0	Result from autodetect logic sequence: 0: DAC was looking for a connection and has yet found a connection 1: DAC was looking for a connection and found a connection
DAC_AUTOUNDETECT_STATUS (R)	1	0x0	Result from autodetect logic sequence: 0: DAC was looking for a disconnection has not yet found a disconnection 1: DAC was looking for a disconnection and found a disconnection
DAC_AUTODETECT_CONNECT (R)	4	0x0	1: At least one channel has a properly terminated device connected. 0: No devices are connected
DAC_AUTODETECT_RED_SENSE (R)	9:8	0x0	Two bit result from last Red/C compare: 0: Channel is disconnected 1: Channel is connected 2: Channel is not checked 3: Reserved
DAC_AUTODETECT_GREEN_SENSE (R)	17:16	0x0	Two bit result from last Green/Y compare: 0: Channel is disconnected 1: Channel is connected 2: Channel is not checked 3: Reserved
DAC_AUTODETECT_BLUE_SENSE (R)	25:24	0x0	Two bit result from last Blue/Comp compare: 0: Channel is disconnected 1: Channel is connected 2: Channel is not checked 3: Reserved

DAC_FORCE_OUTPUT_CNTL - RW - 32 bits - DPCD_VGA:0x8503C			
Field Name	**Bits**	**Default**	**Description**
DAC_FORCE_DATA_EN	0	0x0	Enable synchronous force option on DAC. 0=Disable 1=Enable
DAC_FORCE_DATA_SEL	10:8	0x0	Select which DAC channels have data forced 0=Don't Force, 1=ForceBit 0: Blue channelBit 1: Green channelBit 2: Red channel
DAC_FORCE_DATA_ON_BLANKb_ONLY	24	0x0	Data is force only during active region. 0=Disable 1=Enable

Data Force Control

DAC_FORCE_DATA - RW - 32 bits - DPCD_VGA:0x85040			
Field Name	**Bits**	**Default**	**Description**
DAC_FORCE_DATA	9:0	0x0	Data to be forced on R, G & B channels. When auto detect logic is enabled, this must be programmed to 0x000 (Default).

DAC_POWERDOWN - RW - 32 bits - DPCD_VGA:0x85050			
Field Name	**Bits**	**Default**	**Description**
DAC_POWERDOWN	0	0x0	Bandgap Voltage Reference Power down enable (BGSLEEP)
DAC_POWERDOWN_BLUE	8	0x0	Blue channel power down enable (BDACPD)
DAC_POWERDOWN_GREEN	16	0x0	Green channel power down enable (GDACPD)
DAC_POWERDOWN_RED	24	0x0	Red channel power down enable (RDACPD)

Controls for DAC Start-Up & Power-Down sequences

DAC_CONTROL - RW - 32 bits - DPCD_VGA:0x85058			
Field Name	**Bits**	**Default**	**Description**
DAC_DFORCE_EN	0	0x0	DAC asynchronous data force enable. Can be used for sync force as well but DAC_FORCE_OUTPUT_CNTL achieves the same goal with a more complete feature set. Asynchronous force requires DAC_x_ASYNC_ENABLE in DAC_COMPARATOR_ENABLE to be set as well. Drives DFORCE_EN pin on macro. Forces all DAC channels to DAC_FORCE_DATA value. Overrides DAC_FORCE_OUTPUT_CNTL/DAC_FORCE_DATA_EN control.
DAC_ZSCALE_SHIFT	16	0x0	DAC zero scale shift enable. Causes DAC to add a small offset to the levels of all outputs. Drives DAC ZSCALE_SHIFT pin.

DAC_COMPARATOR_ENABLE - RW - 32 bits - DPCD_VGA:0x8505C			
Field Name	**Bits**	**Default**	**Description**
DAC_COMP_DDET_REF_EN	0	0x0	Enables DAC comparators for analog termination checking with DDETECT_REF as the reference. The DDETECT reference level is lower than SDETECT_REF to allow termination checking on an active channel while the data being driven is the ZSCALE_SHIFT offset.Must be used in conjunction with ZSCALE_SHIFT=1 and with some forced data on the DAC inputs. Only one of COMP_DDET_REF_EN and COMP_SDET_REF_EN should be active at a time.Used in conjunction with core logic to drive the DAC DDETECT pin. 0=Disable 1=Enable
DAC_COMP_SDET_REF_EN	8	0x0	Enables DAC comparators for analog termination checking with SDETECT_REF as the reference. The data must be forced to a sufficiently high value using one of the DAC force features. Only one of COMP_DDET_REF_EN and COMP_SDET_REF_EN should be active at a time.Goes directly to the DAC SDETECT pin. 0=Disable 1=Enable
DAC_R_ASYNC_ENABLE	16	0x0	DAC red channel asynchronous mode enable.Allows DAC outputs to be updated without a clock.Used in conjunction with core logic to drive the DAC R_ASYNC_EN pin. 0=Disable 1=Enable
DAC_G_ASYNC_ENABLE	17	0x0	DAC green channel asynchronous mode enable.Used in conjunction with core logic to drive the DAC G_ASYNC_EN pin. 0=Disable 1=Enable
DAC_B_ASYNC_ENABLE	18	0x0	DAC blue channel asynchronous mode enable.Used in conjunction with core logic to drive the DAC B_ASYNC_EN pin. 0=Disable 1=Enable

DAC_COMPARATOR_OUTPUT - RW - 32 bits - DPCD_VGA:0x85060			
Field Name	**Bits**	**Default**	**Description**
DAC_COMPARATOR_OUTPUT (R)	0	0x0	Monitor Detect Output. This signal is an AND of 3 DAC macro signals: R_CDET, G_YDET & B_COMPDET.
DAC_COMPARATOR_OUTPUT_BLUE (R)	1	0x0	DAC blue channel comparator output ? value comes from DAC R_CDET pin
DAC_COMPARATOR_OUTPUT_GREEN (R)	2	0x0	DAC green channel comparator output ? value comes from DAC G_YDET pin
DAC_COMPARATOR_OUTPUT_RED (R)	3	0x0	DAC red channel comparator output ? value comes from DAC B_COMPDET pin

DAC_PWR_CNTL - RW - 32 bits - DPCD_VGA:0x85068			
Field Name	**Bits**	**Default**	**Description**
DAC_BG_MODE	1:0	0x0	Bandgap macro configuration - BGMODE(1:0)

DAC_DFT_CONFIG - RW - 32 bits - DPCD_VGA:0x8506C			
Field Name	**Bits**	**Default**	**Description**
DAC_DFT_CONFIG	31:0	0x0	Configuration for DAC DFT block

DAC_MACRO_CNTL - RW - 32 bits - DPCD_VGA:0x85074			
Field Name	**Bits**	**Default**	**Description**
DAC_WHITE_LEVEL	1:0	0x2	Video Standard Select bits - STD(1:0) 0x0: PAL 0x1: NTSC PS2 (VGA) 0x3 HDTV (Component Video)
DAC_WHITE_FINE_CONTROL	13:8	0x20	Full-scale Output Adjustment - DACADJ(5:0)
DAC_ANALOG_MONITOR	27:24	0x0	Analog test mux select - MON(3:0)
DAC_CAL_EN	28	0x0	Starts the DACA full-scale calibration if set to 1.Default = 0.

DAC_TEST_ENABLE - RW - 32 bits - DPCD_VGA:0x8507C			
Field Name	**Bits**	**Default**	**Description**
DAC_TEST_ENABLE	0	0x0	DACATEST Enable configures DAC data to come from GPIOs 0=Disable 1=Enable

DAC_MANUAL_DETECTION_CNTL - RW - 32 bits - DPCD_VGA:0x85080			
Field Name	**Bits**	**Default**	**Description**
DAC_MANUAL_DETECT (W)	0	0x0	Forces the Display Port regsiter 0x200 sink count to 1. Set if DAC is manually detected.
DAC_MANUAL_UNDETECT (W)	8	0x0	Forces the Display Port regsiter 0x200 sink count to 0. Set if DAC is manually undetected.

DAC_DEBUG_MUX_CNTL - RW - 32 bits - DPCD_VGA:0x85084			
Field Name	**Bits**	**Default**	**Description**
DAC_DEBUG_MUX_SELECT	2:0	0x0	Selects different signals to be sent out to core debug mux.

DAC_BANDGAP_ADJUSTMENT - RW - 32 bits - DPCD_VGA:0x85088			
Field Name	**Bits**	**Default**	**Description**
DAC_BANDGAP_ADJUSTMENT	5:0	0x20	Bandgap Reference Voltage Adjustment - BGADJ(5:0)

Bandgap Adjust Control

DAC_PIXEL_COMPARE_CONTROL - RW - 32 bits - DPCD_VGA:0x8508C			
Field Name	**Bits**	**Default**	**Description**
DAC_PIXEL_COMPARE_ENABLE	0	0x0	Enable pixel comparison 0=Disable 1=Enable
DAC_PIXEL_COMPARE_CONTINOUS	1	0x0	Continously compare pixels 0=Compare Only One Frame 1=Compare Every Frame
DAC_PIXEL_COMPARE_PER_FRAME	2	0x0	Compare results registered per frame 0=Carry over results to next frame 1=Reset Results Every Frame
DAC_PIXEL_COMPARE_ACTIVE_ONLY	3	0x0	Compare active video section of the frame 0=Compare entire frame 1=Compare only active video
DAC_PIXEL_COMPARE_FIELD	4	0x0	Interlaced field to compare 0=Compare Top Field 1=Compare Bottom Field

Dac Pixel Compare Control

DAC_PIXEL_COMPARE_ERROR_HCOUNT - RW - 32 bits - DPCD_VGA:0x85090			
Field Name	**Bits**	**Default**	**Description**
DAC_PIXEL_COMPARE_ERROR_HCOUNT (R)	15:0	0x0	Pixel Number when first error occured

Pixel Number when first error occured

DAC_PIXEL_COMPARE_ERROR_VCOUNT - RW - 32 bits - DPCD_VGA:0x85094			
Field Name	**Bits**	**Default**	**Description**
DAC_PIXEL_COMPARE_ERROR_VCOUNT (R)	16:0	0x0	Pixel Number when first error occured

Line Number when fist error occured

DAC_PIXEL_COMPARE_ERROR_EXPECTED_PIXEL - RW - 32 bits - DPCD_VGA:0x85098			
Field Name	**Bits**	**Default**	**Description**
DAC_PIXEL_COMPARE_ERROR_EXPECTED_PIXEL_B (R)	9:0	0x0	Blue
DAC_PIXEL_COMPARE_ERROR_EXPECTED_PIXEL_G (R)	19:10	0x0	Green
DAC_PIXEL_COMPARE_ERROR_EXPECTED_PIXEL_R (R)	29:20	0x0	Red

Expected Pixel when first error occured

DAC_PIXEL_COMPARE_ERROR_COMPUTED_PIXEL - RW - 32 bits - DPCD_VGA:0x8509C			
Field Name	**Bits**	**Default**	**Description**
DAC_PIXEL_COMPARE_ERROR_COMPUTED_PIXEL_B (R)	9:0	0x0	Blue
DAC_PIXEL_COMPARE_ERROR_COMPUTED_PIXEL_G (R)	19:10	0x0	Green
DAC_PIXEL_COMPARE_ERROR_COMPUTED_PIXEL_R (R)	29:20	0x0	Red

Computed Pixel when frist error occured

DAC_PIXEL_COMPARE_ERROR_STATUS - RW - 32 bits - DPCD_VGA:0x850A0			
Field Name	**Bits**	**Default**	**Description**
DAC_PIXEL_COMPARE_ERRORS (R)	15:0	0x0	Total Errors accumulated
DAC_PIXEL_COMPARE_ERRORS_WRAPPED (R)	16	0x0	Total Errors wrapped the counter
DAC_PIXEL_COMPARE_ERROR_OCCURED (R)	17	0x0	Error values are valid

Pixel Errors

DAC_LDO_CONTROL - RW - 32 bits - DPCD_VGA:0x850A4			
Field Name	**Bits**	**Default**	**Description**
DAC_LDO_PDN	0	0x0	Power Down Signal 0=Power On 1=Power Off
DAC_LDO_ADJ	7:4	0x8	Adjust value for LDO

Low Dropout Regulator Control

EFUS_DAC_ADJUSTMENT_CONTROL - RW - 32 bits - DPCD_VGA:0x850A8			
Field Name	**Bits**	**Default**	**Description**
EFUS_DAC_BANDGAP_ADJUSTMENT (R)	5:0	0x0	EFUS Value of Bandgap Reference Voltage Adjustment - BGADJ(5:0)
EFUS_DAC_WHITE_FINE_CONTROL (R)	13:8	0x0	EFUS Value of Full-scale Output Adjustment - DACADJ (5:0)
EFUS_OVERRIDE	16	0x0	0= override BGADJ DACADJ by software programming 1=use value of EFUS

DAC EFUS Usage Control

AUX_DPHY_TX_REF_CONTROL - RW - 32 bits - DPCD_VGA:0x86000			
Field Name	**Bits**	**Default**	**Description**
AUX_TX_REF_SEL	0	0x0	Use to select source of half symbol referece. 0=Divided sym_clk 1=Reconstructed from microsecond ref
AUX_TX_RATE	5:4	0x0	Use to select aux channel symbol rate. 0=1 MHz 1=2 MHz 2=4 MHz 3=8 MHz
AUX_TX_REF_DIV	24:16	0x32	Divider to generate 2 MHz reference from sym_clk.

Allows you to control the half-symbol reference signal.

AUX_DPHY_TX_CONTROL - RW - 32 bits - DPCD_VGA:0x86004			
Field Name	**Bits**	**Default**	**Description**
AUX_TX_PRECHARGE_LEN	2:0	0x0	Passive Precharge duraion. When AUX_DPHY_TX_REF_CONTROL.AUX_TX_REF_SEL=1, AUX_TX_PRECHARGE_LEN must be 2 or higher to allow TX sm 10 ns to compute the tx half symbol period. The total precharge time, defined by 8 * AUX_TX_PRECHARGE_LEN + AUX_SYM_PERIOD * AUX_TX_PRECHARGE_SYMBOLS, must be between 10 and 50 ns. 0=0us 1=8us 2=16us 3=24us 4=32us 5=40us 6=48us 7=56us
AUX_TX_PRECHARGE_FORMAT	3	0x0	control precharge pattern format. 1: constant patten, no toggle. 0: 0101 toggle pattern just as preamble
AUX_TX_PRECHARGE_SYMBOLS	13:8	0x10	Active Precharge duration. Number of '0' symbols to transmit as part of precharge in addition to 16 '0' symbols sent as part of sync pattern.

Control for programming precharge duration

AUX_DPHY_RX_CONTROL0 - RW - 32 bits - DPCD_VGA:0x86008			
Field Name	**Bits**	**Default**	**Description**
AUX_RX_IGNORE_RECV_NO_DET	0	0x0	Consider a receive valid even if a symbol is below threshold.
AUX_RX_START_WINDOW	6:4	0x1	Sets size of window in which transitions will be considered valid before lock. (is relative to detected period) 0=1/2 period 1=1/4 period 2=1/8 period 3=1/16 period 4=1/32 period 5=1/64 period 6=1/128 period 7=1/256 period
AUX_RX_RECEIVE_WINDOW	10:8	0x2	Sets size of window in which transitions will be considered valid once locked. (is relative to detected period) 0=1/2 period 1=1/4 period 2=1/8 period 3=1/16 period 4=1/32 period 5=1/64 period 6=1/128 period 7=1/256 period
AUX_RX_HALF_SYM_DETECT_LEN	13:12	0x1	Number of transitions to use to accumulate aux half symbol clock period. 0=6 edges 1=10 edges 2=18 edges 3=Reserved
AUX_RX_TRANSITION_FILTER_EN	16	0x1	Enable to restart half symbol detect when transition is outside window. 0=Disable 1=Enable
AUX_RX_ALLOW_BELOW_THRESHOLD_PHASE_DETECT	17	0x0	Determine whether to allow symbols below detection threshold when detecting symbol phase during the sync preamble. 0=Don't Allow 1=Allow
AUX_RX_ALLOW_BELOW_THRESHOLD_START	18	0x1	Determine whether to allow symbols below detection threshold when detecting START pattern. 0=Don't Allow 1=Allow
AUX_RX_ALLOW_BELOW_THRESHOLD_STOP	19	0x1	Determine whether to allow symbols below detection threshold when detecting STOP pattern. 0=Don't Allow 1=Allow
AUX_RX_PHASE_DETECT_LEN	21:20	0x3	Number of sync symbols to use for phase reset. 0=2 half symbols 1=4 half symbols 2=6 half symbols 3=8 half symbols

AUX_DPHY_RX_CONTROL0 - RW - 32 bits - DPCD_VGA:0x86008			
Field Name	**Bits**	**Default**	**Description**
AUX_RX_DETECTION_THRESHOLD	30:28	0x1	Sets correlation threshold level (relative to number of samples per symbol) required to consider a symbol valid. 0=1/2 1=3/4 2=7/8 3=15/16 4=31/32 5=63/64 6=127/128 7=255/256
AUX_RX_SAMPLING_ECO_EN	31	0x0	(Active Low) Improve glitch rejection 0=Enabled 1=Disabled

Allows you to fine tune various parameters of the recieve transaction.

AUX_DPHY_TIMEOUTS - RW - 32 bits - DPCD_VGA:0x8600C			
Field Name	**Bits**	**Default**	**Description**
AUX_RX_PHASE_SYNC_TIMEOUT_LEN	9:0	0x14	Phase Sync Timeout length (us)
AUX_RX_WAIT_START_TIMEOUT_LEN	19:10	0xc8	Wait Start Timeout length (us)
AUX_RX_RECEIVE_TIMEOUT_LEN	29:20	0xc8	Receive Timeout length (us)

Timeouts for the different portions of a receive transaction.

AUX_DPHY_RX_CONTROL1 - RW - 32 bits - DPCD_VGA:0x86010			
Field Name	**Bits**	**Default**	**Description**
AUX_RX_PRECHARGE_SKIP	7:0	0xa	Number of transitions to skip before starting to lock, defaulted to 0
FRACT_COUNT_SEL	16	0x0	1: conventional coding style, backup usage; 0:Jacobinical style
BUF_STYLE_SEL	17	0x0	1: conventional coding style, backup usage; 0:Jacobinical style

Control for skipping/programming precharge state for receive transaction.

AUX_DPHY_STATUS - RW - 32 bits - DPCD_VGA:0x86014			
Field Name	**Bits**	**Default**	**Description**
AUX_TX_HALF_SYM_PERIOD (R)	8:0	0x0	Half symbol clock period based on on used fr TX and as initial guess for TS.
AUX_RX_SYNC_VALID_COUNT (R)	14:10	0x0	Indicates the number of consecutive valid transitions detected during the sync preamble. This is the maximum count- it is cleared on 'go'.
AUX_RX_HALF_SYM_PERIOD_FRACT (R)	20:16	0x0	Fractional bits of half symbol period detected during FREQ_SYNC state.
AUX_RX_HALF_SYM_PERIOD (R)	29:21	0x0	Half symbol period detected during the FREQ_SYNC state in symbol clocks.

Allows you to view recieve status information.

AUX_ERROR_STATUS - RW - 32 bits - DPCD_VGA:0x86018			
Field Name	**Bits**	**Default**	**Description**
AUX_RECV_TIMEOUT (R)	0	0x0	rx timeout during receive state
AUX_PHASE_SYNC_TIMEOUT (R)	1	0x0	rx timeout during phase-sync state
AUX_WAIT_START_TIMEOUT (R)	2	0x0	rx timeout during wait-start state
AUX_XACT_TIMEOUT (R)	3	0x0	receive transaction timeout
AUX_RX_PARTIAL_BYTE (R)	4	0x0	rx partial byte detected
AUX_RX_MIN_COUNT_VIOL (R)	5	0x0	rx min count violation detected
AUX_RX_SYNC_INVALID_L (R)	6	0x0	rx sync invalid l detected
AUX_RX_SYNC_INVALID_H (R)	7	0x0	rx sync invalid h detected
AUX_RX_INVALID_START (R)	8	0x0	rx invalid start detected
AUX_RX_INVALID_STOP (R)	9	0x0	rx invalid stop detected
AUX_RX_RECV_NO_DET (R)	10	0x0	rx recv no det detected
AUX_RX_RECV_INVALID_H (R)	11	0x0	rx recv invalid H detected
AUX_RX_RECV_INVALID_L (R)	12	0x0	rx recv invalid L detected
AUX_RX_INVALID_CMD (R)	13	0x0	rx recv an invalid command field or an invalid length field

Error Status

AUX_XACT_TIMEOUT_LEN - RW - 32 bits - DPCD_VGA:0x8601C			
Field Name	**Bits**	**Default**	**Description**
AUX_XACT_TIMEOUT_LEN	9:0	0x12c	Transaction Timeout limit

Transaction Timeout limit

AUX_TEST_MODE - RW - 32 bits - DPCD_VGA:0x86020			
Field Name	**Bits**	**Default**	**Description**
AUX_FORCE_SYNC_TX	0	0x0	When set, generate continous sync pattern.
AUX_FORCE_RX_MODE	1	0x0	When set, force aux block into receive mode.
AUX_FORCE_TX_HIGH	2	0x0	When set, generate transmit high output.
AUX_FORCE_TX_LOW	3	0x0	When set, generate transmit low output.
AUX_DBGMUX_SEL_LOW	15:8	0x0	Mux select for debug bus

Aux channel Test Mode Control

AUX_SCRATCH0 - RW - 32 bits - DPCD_VGA:0x86024			
Field Name	**Bits**	**Default**	**Description**
AUX_SCRATCH0	31:0	0x0	Scratch Register

Scratch Register

AUX_SCRATCH1 - RW - 32 bits - DPCD_VGA:0x86028			
Field Name	**Bits**	**Default**	**Description**
AUX_SCRATCH1	31:0	0x0	Scratch Register

Scratch Register

AUX_SCRATCH2 - RW - 32 bits - DPCD_VGA:0x8602C			
Field Name	**Bits**	**Default**	**Description**
AUX_SCRATCH2	31:0	0x0	Scratch Register

Scratch Register

AUX_SCRATCH3 - RW - 32 bits - DPCD_VGA:0x86030			
Field Name	**Bits**	**Default**	**Description**
AUX_SCRATCH3	31:0	0x0	Scratch Register

Scratch Register

AUX_SCRATCH4 - RW - 32 bits - DPCD_VGA:0x86034			
Field Name	**Bits**	**Default**	**Description**
AUX_SCRATCH4	31:0	0x0	Scratch Register

Scratch Register

AUX_PAD_CTRL - RW - 32 bits - DPCD_VGA:0x86038			
Field Name	**Bits**	**Default**	**Description**
AUX_PAD_DGEN	0	0x0	Enable glitch rejection
AUX_PAD_DETEN	1	0x1	Enable detection circuit
AUX_PAD_TERM0	2	0x0	Term0
AUX_PAD_TERM1	3	0x0	Term1
AUX_PAD_DETSEL	4	0x0	Detection level (5 edges or 9 edges)
AUX_PAD_SPARE0	5	0x0	spare0
AUX_PAD_SPARE1	6	0x0	spare1

Pad controls

AUX_DETECT_TIMEOUT - RW - 32 bits - DPCD_VGA:0x8603C			
Field Name	**Bits**	**Default**	**Description**
AUX_DETECT_TIMEOUT	19:0	0x7d00	detection timeout length

Detection timeout length

IMPCAL_AUXN - RW - 32 bits - DPCD_VGA:0x86044			
Field Name	**Bits**	**Default**	**Description**
AUXN_IMPCAL_ENABLE	0	0x1	Indicates that the impedance calibration state machine should cary out impedance calibration for the AUXN pad
AUXN_IMPCAL_CALOUT (R)	8	0x0	Readback value of IO_DC_auxn_calout
AUXN_CALOUT_ERROR (R)	9	0x0	Error Flag if calibration reaches min/max without calout toggle
AUXN_CALOUT_ERROR_AK (W)	10	0x0	Acknowledge for the error flag
AUXN_IMPCAL_VALUE (R)	19:16	0x0	Readback value of DC_IO_auxn_cal_impval

IMPCAL_AUXN - RW - 32 bits - DPCD_VGA:0x86044			
Field Name	**Bits**	**Default**	**Description**
AUXN_IMPCAL_STEP_DELAY	23:20	0x1	Defines the number of MICROSEC_REF pulses between increases/decreases of DC_IO_auxn_cal_impval. 0: 1 usec_ref pulse, 1: 2 usec_ref pulse, ..., 15: 16 usec_ref pulse
AUXN_IMPCAL_OVERRIDE	27:24	0x5	Specifes value for software override
AUXN_IMPCAL_OVERRIDE_ENABLE	28	0x0	Enables software override.

aux cal n control

IMPCAL_PERIOD - RW - 32 bits - DPCD_VGA:0x86048			
Field Name	**Bits**	**Default**	**Description**
CAL_PERIOD	23:0	0x9c40	Number of microseconds between recalibrations.

aux cal period

IMPCAL_CTRL - RW - 32 bits - DPCD_VGA:0x8604C			
Field Name	**Bits**	**Default**	**Description**
CAL_PERIOD_EN	0	0x1	Enable periodic recalibrations.
CAL_RECAL_REQ (W)	1	0x0	Request an immediate recalibration
CALR_CNTL_OVERRIDE	3:2	0x0	
IMPCAL_STATE (R)	6:4	0x0	Readback value of the calibration state machine
CAL_DONE (R)	7	0x0	Calibration done status flag

aux cal control

IMPCAL_PAD_TEST - RW - 32 bits - DPCD_VGA:0x86050			
Field Name	**Bits**	**Default**	**Description**
PAD_TEST_MODE_EN	0	0x0	Enable pad test mode. All pad inputs and outputs are mapped to register bits
AUXCAL_PAD_BIASEN	1	0x0	BIASEN
AUXCAL_PAD_EN_N	2	0x0	EN_N
AUXCAL_PAD_NG0	4	0x0	NG0
AUXCAL_PAD_NG1	5	0x0	NG1
AUXCAL_PAD_NG2	6	0x0	NG2
AUXCAL_PAD_NG3	7	0x0	NG3
AUXCAL_PAD_CALOUTN (R)	12	0x0	CALOUTN

aux cal pad test

DC_I2C_CONTROL - RW - 32 bits - DPCD_VGA:0x87000			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_GO (W)	0	0x0	Write 1 to start I2C transfer.
DC_I2C_SOFT_RESET	1	0x0	Write 1 to reset I2C controller
DC_I2C_SEND_RESET	2	0x0	Set to 1 to send reset sequence (9 clocks with no data) at start of transfer. This sequence is sent after DC_I2C_GO is written to 1, before the first transaction only.
DC_I2C_SW_STATUS_RESET	3	0x0	Write 1 to reset DC_I2C_SW_STATUS flags, will reset SW_DONE, ABORTED, TIMEOUT, SW_INTERRUPTED, BUFFER_OVERFLOW, STOPPED_ON_NACK, NACK0, NACK1, NACK2, NACK3
DC_I2C_SDVO_EN	4	0x0	Set to 1 to send two transactions to configure SDVO bus for DDC before main transaction. The SDVO transaction is as follows: S-AAw-a-07-a-02-a-P-S-AAw-a-08-a-7A-a-P where AA is the address and is selected by DC_I2C_SDVO_ADDR_SEL. The SDVO transactions take place after the RESET transaction (if enabled) and before the remaining transactions. 0=Disable 1=Enable
DC_I2C_SDVO_ADDR_SEL	6	0x0	Use to select address for SDVO I2C bus configuration 0=0x70 1=0x72
DC_I2C_TRANSACTION_COUNT	21:20	0x0	Number of transactions to be done in current transfer. 0=transaction0 only 1=transaction0, transaction1 2=transaction0, transaction1, transaction2 3=transaction0, transaction1, transaction2, transaction3 (DC_I2C_REPEAT=0 only)

DC_I2C_ARBITRATION - RW - 32 bits - DPCD_VGA:0x87004			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_SW_PRIORITY	1:0	0x1	Sets priority for software I2C requests. This setting applies only when HDCP is using I2C bus and software also wants to use the same I2C bus 0=Normal - If DC_I2C_NO_QUEUED_SW_GO = 0, software I2C transaction will be queued after HW I2C. If DC_I2C_NO_QUEUED_SW_GO = 1, software I2C transaction is not queued, in this case, software have to poll for DC_I2C_DDCx_HW_DONE doing any I2C transaction 1=High - Software always interrupts HW I2C if HDCP is using the same I2C bus, HW I2C will automatically resume once software I2C is completed 2=Reserved 3=Reserved

DC_I2C_ARBITRATION - RW - 32 bits - DPCD_VGA:0x87004			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_REG_RW_CNTL_STATUS (R)	3:2	0x0	Specifies whether host(software) or embedded microcontroller have control of the DC_I2C group of registers. The unit in control is the only one permitted to read/write the DC_I2C registers and use the I2C controller. 0=No Read/Write of I2C registers permitted 1=Only software can read/write I2C Registers 2=Only DMCU can read/write I2C Registers 3=Reserved
DC_I2C_NO_QUEUED_SW_GO	4	0x0	Set to 1 to disable queuing of software I2C GO. If this bit is set, then if software writes DC_I2C_GO while I2C is in use by hardware, the GO request will be ignored and the DC_I2C_SW_INTERRUPTED bit set.
DC_I2C_ABORT_HW_XFER (W)	8	0x0	Write 1 to abort current HW transfer (send stop if transfer has started)
DC_I2C_ABORT_SW_XFER (W)	12	0x0	Write 1 to abort current SW transfer (send stop if transfer has started)
DC_I2C_SW_USE_I2C_REG_REQ	20	0x0	Software should write this register to 1 when they want to read/write the I2C DDC registers. Reading this register indicates if there is a pending request from software for read/write control of the I2C registers
DC_I2C_SW_DONE_USING_I2C_REG (W)	21	0x0	When software has control of the I2C DDC registers, it should write this bit to 1 when it has completed using the I2C DDC registers and interface after each transaction.
DC_I2C_DMCU_USE_I2C_REG_REQ	24	0x0	The embedded microcontroller will write this register to 1 when it wants to use the I2C DDC interface and read/write the I2C DDC registers. Reading this register indicates if there is a pending request already from DMCU for read/write control of the I2C registers
DC_I2C_DMCU_DONE_USING_I2C_REG (W)	25	0x0	The embedded microcontroller will write this register to 1 when it currently has control of the I2C DDC interface and it has completed its transaction and read/write usage of the I2C DDC registers.

Configure arbitration between hardware, software and embedded microcontroller use of the DC_I2C engine

DC_I2C_INTERRUPT_CONTROL - RW - 32 bits - DPCD_VGA:0x87008			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_SW_DONE_INT (R)	0	0x0	SW_DONE interrupt status
DC_I2C_SW_DONE_ACK (W)	1	0x0	Acknowledge bit for DC_I2C_SW_DONE_INT. Write 1 to clear interrupt.
DC_I2C_SW_DONE_MASK	2	0x0	Mask bit for DC_I2C_SW_DONE_INT. Set to 1 to enable interrupt.
DC_I2C_DDC1_HW_DONE_INT (R)	4	0x0	DDC1 HW_DONE interrupt status
DC_I2C_DDC1_HW_DONE_ACK (W)	5	0x0	DDC1 Acknowledge bit for DC_I2C_HW_DDC1_DONE_INT. Write 1 to clear interrupt.
DC_I2C_DDC1_HW_DONE_MASK	6	0x0	DDC1 Mask bit for DC_I2C_HW_DDC1_DONE_INT. Set to 1 to enable interrupt.

DC_I2C_SW_STATUS - RW - 32 bits - DPCD_VGA:0x8700C			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_SW_STATUS (R)	1:0	0x0	Current SW status of DC_I2C 0=Idle 1=In use by SW 2=In use by HW 3=In use by DMCU
DC_I2C_SW_DONE (R)	2	0x0	Set on completion of SW transfer. Cleared by writing DC_I2C_SW_DONE_ACK to 1
DC_I2C_SW_ABORTED (R)	4	0x0	Indicates that abort request ccurred during SW transfer, stopping transfer. Cleared on GO.
DC_I2C_SW_TIMEOUT (R)	5	0x0	Indicates that timeout condition occurred during SW transfer, stopping transfer. Cleared on GO.
DC_I2C_SW_INTERRUPTED (R)	6	0x0	Indicates that SW transfer was interrupted by hardware request. Cleared on GO.
DC_I2C_SW_BUFFER_OVERFLOW (R)	7	0x0	Indicates that buffer overflow occurred during SW transfer, stopping transfer. Cleared on GO.
DC_I2C_SW_STOPPED_ON_NACK (R)	8	0x0	Indicates that SW transfer was interrpted due to NACK when STOP_ON_NACK=1. Cleared on GO.
DC_I2C_SW_SDVO_NACK (R)	10	0x0	
DC_I2C_SW_NACK0 (R)	12	0x0	Indicates that I2C slave did not issue an acknowledge during the first SW transaction. Cleared on GO.
DC_I2C_SW_NACK1 (R)	13	0x0	Indicates that I2C slave did not issue an acknowledge during the second SW transaction. Cleared on GO.
DC_I2C_SW_NACK2 (R)	14	0x0	Indicates that I2C slave did not issue an acknowledge during the third SW transaction. Cleared on GO.
DC_I2C_SW_NACK3 (R)	15	0x0	Indicates that I2C slave did not issue an acknowledge during the fourth SW transaction. Cleared on GO.
DC_I2C_SW_REQ (R)	18	0x0	Software requests use of DC_I2C interface (indicates that request is pending - i.e. queued). Cleared when request becomes active or by DC_I2C_ABORT_SW_XFER.

Status fields for DC_I2C engine

DC_I2C_DDC1_HW_STATUS - RW - 32 bits - DPCD_VGA:0x87010			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_DDC1_HW_STATUS (R)	1:0	0x0	Current HW status of DC_I2C 0=Idle 1=In use by SW 2=In use by HW 3=In use by DMCU
DC_I2C_DDC1_HW_DONE (R)	3	0x0	Set on completion of HW transfer. Cleared by writing DC_I2C_HW_DONE_ACK to 1
DC_I2C_DDC1_HW_REQ (R)	16	0x0	Hardware requests use of DC_I2C interface (indicates that request is pending - i.e. queued). Cleared when request becomes active or by DC_I2C_ABORT_HW_XFER.
DC_I2C_DDC1_HW_URG (R)	17	0x0	Indicates that hardware I2C request is urgent (used by arbitration logic).

Status fields for DC_I2C engine

DC_I2C_DDC1_SPEED - RW - 32 bits - DPCD_VGA:0x87014			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_DDC1_THRESHOLD	1:0	0x2	Select threshold to use to determine whether value sampled on SDA is 1 or 0. Specified in terms of the ratio between the number of sampled ones and the total number of times SDA is sampled. 0=>0 1=1/4 of total samples 2=1/2 of total samples 3=3/4 of total samples
DC_I2C_DDC1_DISABLE_FILTER_DURING_STALL	4	0x0	Determines whether dout_filter will be disabled when receiver is clock stalling. 0=Disable 1=Do not Disable
DC_I2C_DDC1_PRESCALE	31:16	0x0	prescale = 1Mhz / (desired_i2c_speed) Note: In rev A12, DC_I2C_DDC1_PRESCALE[0] was used for selection of old and new i2c timing prescale[0]=0: new i2c timing (default value) prescale[0]=1: old i2c timing

DDC1 speed setting

DC_I2C_DDC1_SETUP - RW - 32 bits - DPCD_VGA:0x87018			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_DDC1_DATA_DRIVE_EN	0	0x0	Select whether SDA pad is pulled up or driven high 0=Pullup by external resistor 1=I2C pads drive SDA
DC_I2C_DDC1_DATA_DRIVE_SEL	1	0x0	Select number of clocks to drive SDA high 0=Drive for 10MCLKs 1=20MCLKS
DC_I2C_DDC1_CLK_DRIVE_EN	7	0x0	Select whether SCL pad is pulled up or driven high 0=Pullup by external resistor 1=I2C pads drive SCL
DC_I2C_DDC1_INTRA_BYTE_DELAY	15:8	0x0	Use to specify delay between bytes in units of I2C reference.
DC_I2C_DDC1_INTRA_TRANSACTION_DELAY	23:16	0x0	Use to specify delay between transactions in units of I2C reference.
DC_I2C_DDC1_TIME_LIMIT	31:24	0x0	Time limit, in units of 256 I2C fast reference (TOCLK) pulses, to wait before timeout when clock is stalled by external device.

DDC1 SETUP

DC_I2C_TRANSACTION0 - RW - 32 bits - DPCD_VGA:0x8701C			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_RW0	0	0x0	Read/write indicator for first transaction - set to 0 for write, 1 for read. This bit only controls DC_I2C behaviour - the R/W bit in the transaction is programmed into the I2C buffer as the LSB of the address byte. 0=WRITE 1=READ
DC_I2C_STOP_ON_NACK0	8	0x0	Determines whether the current transfer will stop if a NACK is received during the first transaction (current transaction always stops). 0=STOP CURRENT TRANSACTION, GO TO NEXT TRANSACTION 1=STOP ALL TRANSACTIONS, SEND STOP BIT
DC_I2C_START0	12	0x0	Determines whether a start bit will be sent before the first transaction 0=NO START 1=START
DC_I2C_STOP0	13	0x0	Determines whether a stop bit will be sent after the first transaction 0=NO STOP 1=STOP
DC_I2C_STRETCH0	14	0x0	0=DO NOT STRETCH SCL 1=STRETCH SCL
DC_I2C_NOADDR0	15	0x0	0=SEND ADDRESS 1=NO ADDRESS SENT
DC_I2C_COUNT0	24:16	0x0	Byte count for first transaction (excluding the first byte, which is usually the address).

Configuration for first transaction

DC_I2C_TRANSACTION1 - RW - 32 bits - DPCD_VGA:0x87020			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_RW1	0	0x0	Read/write indicator for second transaction - set to 0 for write, 1 for read. This bit only controls DC_I2C behaviour - the R/W bit in the transaction is programmed into the I2C buffer as the LSB of the address byte. 0=WRITE 1=READ
DC_I2C_STOP_ON_NACK1	8	0x0	Determines whether the current transfer will stop if a NACK is received during the second transaction (current transaction always stops). 0=STOP CURRENT TRANSACTION, GO TO NEXT TRANSACTION 1=STOP ALL TRANSACTIONS, SEND STOP BIT
DC_I2C_START1	12	0x0	Determines whether a start bit will be sent before the second transaction 0=NO START 1=START
DC_I2C_STOP1	13	0x0	Determines whether a stop bit will be sent after the second transaction 0=NO STOP 1=STOP
DC_I2C_STRETCH1	14	0x0	0=DO NOT STRETCH SCL 1=STRETCH SCL

DC_I2C_TRANSACTION1 - RW - 32 bits - DPCD_VGA:0x87020			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_NOADDR1	15	0x0	0=SEND ADDRESS 1=NO ADDRESS SENT
DC_I2C_COUNT1	24:16	0x0	Byte count for second transaction (excluding the first byte, which is usually the address).

Configuration for second transaction

DC_I2C_TRANSACTION2 - RW - 32 bits - DPCD_VGA:0x87024			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_RW2	0	0x0	Read/write indicator for third transaction - set to 0 for write, 1 for read. This bit only controls DC_I2C behaviour - the R/W bit in the transaction is programmed into the I2C buffer as the LSB of the address byte. 0=WRITE 1=READ
DC_I2C_STOP_ON_NACK2	8	0x0	Determines whether the current transfer will stop if a NACK is received during the third transaction (current transaction always stops). 0=STOP CURRENT TRANSACTION, GO TO NEXT TRANSACTION 1=STOP ALL TRANSACTIONS, SEND STOP BIT
DC_I2C_START2	12	0x0	Determines whether a start bit will be sent before the third transaction 0=NO START 1=START
DC_I2C_STOP2	13	0x0	Determines whether a stop bit will be sent after the third transaction 0=NO STOP 1=STOP
DC_I2C_STRETCH2	14	0x0	0=DO NOT STRETCH SCL 1=STRETCH SCL
DC_I2C_NOADDR2	15	0x0	0=SEND ADDRESS 1=NO ADDRESS SENT
DC_I2C_COUNT2	24:16	0x0	Byte count for third transaction (excluding the first byte, which is usually the address).

Configuration for third transaction

DC_I2C_TRANSACTION3 - RW - 32 bits - DPCD_VGA:0x87028			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_RW3	0	0x0	Read/write indicator for fourth transaction - set to 0 for write, 1 for read. This bit only controls DC_I2C behaviour - the R/W bit in the transaction is programmed into the I2C buffer as the LSB of the address byte. 0=WRITE 1=READ
DC_I2C_STOP_ON_NACK3	8	0x0	Determines whether the current transfer will stop if a NACK is received during the fourth transaction (current transaction always stops). 0=STOP CURRENT TRANSACTION, GO TO NEXT TRANSACTION 1=STOP ALL TRANSACTIONS, SEND STOP BIT

DC_I2C_TRANSACTION3 - RW - 32 bits - DPCD_VGA:0x87028			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_START3	12	0x0	Determines whether a start bit will be sent before the fourth transaction 0=NO START 1=START
DC_I2C_STOP3	13	0x0	Determines whether a stop bit will be sent after the fourth transaction 0=NO STOP 1=STOP
DC_I2C_STRETCH3	14	0x0	0=DO NOT STRETCH SCL 1=STRETCH SCL
DC_I2C_NOADDR3	15	0x0	0=SEND ADDRESS 1=NO ADDRESS SENT
DC_I2C_COUNT3	24:16	0x0	Byte count for fourth transaction (excluding the first byte, which is usually the address).

Configuration for fourth transaction

DC_I2C_DATA - RW - 32 bits - DPCD_VGA:0x8702C			
Field Name	**Bits**	**Default**	**Description**
DC_I2C_DATA_RW	0	0x0	Select whether buffer access will be a read or write. For writes, address auto-increments on write to DC_I2C_DATA. For reads, address auto-increments on reads to DC_I2C_DATA. 0=Write 1=Read
DC_I2C_DATA	15:8	0x0	Use to fill or read the I2C buffer
DC_I2C_INDEX	24:16	0x0	Use to set index into I2C buffer for next read or current write, or to read index of current read or next write. Writable only when DC_I2C_INDEX_WRITE=1.
DC_I2C_INDEX_WRITE (W)	31	0x0	To write index field, set this bit to 1 while writing DC_I2C_DATA.

This register is used to read or write the I2C buffer

DC_I2C_EDID_DETECT_CONTROL - RW - 32 bits - DPCD_VGA:0x87030			
Field Name	**Bits**	**Default**	**Description**
I2C_EDID_DETECT_ENABLE	0	0x0	Enables automatic detection of an EDID
I2C_EDID_DETECT_MODE	1	0x0	0=Detection Polling 1=Undetection Polling
I2C_EDID_DETECT_SEND_RESET	2	0x0	Send a reset over i2c
I2C_EDID_DETECT_TRY_UNTIL_VALID	11:8	0x4	Number of times the result must be the same before an actual detection is determined.
I2C_EDID_MANUAL_DETECT (W)	16	0x0	Forces the Display Port regsiter 0x200 sink count to 1. Set if EDID is manually detected.
I2C_EDID_MANUAL_UNDETECT (W)	24	0x0	Forces the Display Port regsiter 0x200 sink count to 0. Set if EDID is manually undetected.
HW_AUTO_PLUG_UNPLUG_SWITCH	25	0x0	Enable hardware FSM to auto plug(detect) and unplug (undetect) switch 0=Use software to set plug or unplug mode 1=Use hardware FSM to auto switch between plug(detect) and unplug (undetect) state
CURRENT_I2C_EDID_DETECT_MODE (R)	26	0x0	Current i2c edid detect 0=Current state is plug detection 1=Current state is unplug detection

DC_I2C_EDID_DETECT_READ_ADDRESS - RW - 32 bits - DPCD_VGA:0x87034			
Field Name	**Bits**	**Default**	**Description**
I2C_EDID_DETECT_READ_ADDRESS	7:0	0xa0	Adress to read EDID
I2C_EDID_DETECT_READ_RESULT (R)	23:16	0x0	Result from the EDID read

DC_I2C_EDID_DETECT_WAIT_TIME - RW - 32 bits - DPCD_VGA:0x87038			
Field Name	**Bits**	**Default**	**Description**
I2C_EDID_DETECT_WAIT_TIME	15:0	0x1f4	Time to wait before next EDID detection transaction begins.

DC_I2C_EDID_DETECT_STATUS - R - 32 bits - DPCD_VGA:0x8703C			
Field Name	**Bits**	**Default**	**Description**
I2C_EDID_DETECT_STATUS	1:0	0x0	0=Detected 1=Undetect. Only valid if block is enabled
I2C_EDID_DETECT_VALID_TRYS	11:8	0x0	Number of detection transactions that were the same
I2C_EDID_DETECT_STATE	22:16	0x0	State of the EDID detect machine.

I2C_DEBUG_BUS - RW - 32 bits - DPCD_VGA:0x87FFC			
Field Name	**Bits**	**Default**	**Description**
I2C_DEBUG_MUX_SELECT	0	0x0	Select between the EDID undetect and DC_I2C debug buses.
DOUT_I2C_DEBUG_BUS (R)	31:24	0x0	

I2C Debug Control

EC_SHARED_CLK_ENABLE - RW - 32 bits - DPCD_VGA:0x88000			
Field Name	**Bits**	**Default**	**Description**
NONSPREAD_REF_REG_IO_CLK_ENABLE	0	0x1	0=nonspread_ref_reg_io_gated_clk disabled 1=nonspread_ref_reg_io_gated_clk enabled
SPREAD_REF_JTAG_CLK_ENABLE	1	0x1	0=spread_ref_jtag_gated_clk disabled 1=spread_ref_jtag_gated_clk enabled
SPREAD_REF_REG_PCIEPLL_CLK_ENABLE	4	0x1	0=spread_ref_reg_pciepll_gated_clk disabled 1=spread_ref_reg_pciepll_gated_clk enabled

Clock Enables for the domains shared between LVDS and VGA

EC_EXT_VREG_OFF - RW - 32 bits - DPCD_VGA:0x88004			
Field Name	**Bits**	**Default**	**Description**
EXT_VREG_OFF	0	0x0	external voltage regulator gating control 0=external voltage regulator is turned on 1=external voltage regulator is turned off

EC_VGA_CLK_ENABLE - RW - 32 bits - DPCD_VGA:0x88008			
Field Name	**Bits**	**Default**	**Description**
VGAC_CLK_ENABLE	0	0x1	0=vgac_gated_clk disabled 1=vgac_gated_clk enabled
VGAC_REG_DAC_CLK_ENABLE	1	0x1	0=vgac_gated_reg_dac_clk disabled 1=vgac_gated_reg_dac_clk enabled
VGAC_REG_DISPC_CLK_ENABLE	2	0x1	0=vgac_gated_reg_dispc_clk disabled 1=vgac_gated_reg_dispc_clk enabled
VGAC_REG_DFIFO_CLK_ENABLE	3	0x1	0=vgac_gated_reg_dfifo_clk disabled 1=vgac_gated_reg_dfifo_clk enabled
LS_VGA_CLK_ENABLE	4	0x1	0=ls_vga_gated_clk disabled 1=ls_vga_gated_clk enabled
LS_VGA_REG_PCIERX_CLK_ENABLE	5	0x1	0=ls_vga_gated_reg_pcierx_clk disabled 1=ls_vga_gated_reg_pcierx_clk enabled
LS_VGA_REG_DPRL_CLK_ENABLE	6	0x1	0=ls_vga_gated_reg_dprl_clk disabled 1=ls_vga_gated_reg_dprl_clk enabled
NONSPREAD_REF_VGA_CLK_ENABLE	8	0x1	0=nonspread_ref_vga_gated_clk disabled 1=nonspread_ref_vga_gated_clk enabled
NONSPREAD_REF_VGA_REG_I2C_CLK_ENABLE	9	0x1	0=nonspread_ref_vga_gated_reg_i2c_clk disabled 1=nonspread_ref_vga_gated_reg_i2c_clk enabled
NONSPREAD_REF_VGA_REG_PLL_CLK_ENABLE	10	0x1	0=nonspread_ref_vga_gated_reg_pll_clk disabled 1=nonspread_ref_vga_gated_reg_pll_clk enabled
LS_VGA_HPD_DPRL_CLK_ENABLE	11	0x1	0=ls_vga_gated_hpd_dprl_clk disabled 1=ls_vga_gated_hpd_dprl_clk enabled

Clock Enables for the VGA domains

EC_SHARED_SOFT_RESET - RW - 32 bits - DPCD_VGA:0x8800C			
Field Name	**Bits**	**Default**	**Description**
NONSPREAD_REF_IO_SOFT_RESET	0	0x0	0=nonspread_ref_io_rst soft reset disabled 1=nonspread_ref_io_rst soft reset enabled
SPREAD_REF_JTAG_SOFT_RESET	1	0x0	0=spread_ref_jtag_rst soft reset disabled 1=spread_ref_jtag_rst soft reset enabled
SPREAD_REF_PCIEPLL_SOFT_RESET	2	0x0	0=spread_ref_pciepll_rst soft reset disabled 1=spread_ref_pciepll_rst soft reset enabled

Soft reset bits for the domains shared between LVDS and VGA

EC_VGA_SOFT_RESET - RW - 32 bits - DPCD_VGA:0x88014			
Field Name	**Bits**	**Default**	**Description**
VGAC_VGAC_SOFT_RESET	0	0x0	0=vgac_vgac_rst soft reset disabled 1=vgac_vgac_rst soft reset enabled
VGAC_DFIFO_SOFT_RESET	1	0x0	0=vgac_dfifo_rst soft reset disabled 1=vgac_dfifo_rst soft reset enabled
LS_VGA_DPRL_SOFT_RESET	4	0x0	0=ls_vga_dprl_rst soft reset disabled 1=ls_vga_dprl_rst soft reset enabled
LS_VGA_DFIFO_SOFT_RESET	5	0x0	0=ls_vga_dfifo_rst soft reset disabled 1=ls_vga_dfifo_rst soft reset enabled
LS_VGA_VGAC_SOFT_RESET	6	0x0	0=ls_vga_vgac_rst soft reset disabled 1=ls_vga_vgac_rst soft reset enabled
LS_VGA_PCIERX_SOFT_RESET	7	0x0	0=ls_vga_pcierx_rst soft reset disabled 1=ls_vga_pcierx_rst soft reset enabled
NONSPREAD_REF_VGA_DFIFO_SOFT_RESET	8	0x0	0=nonspread_ref_vga_dfifo_rst soft reset disabled 1=nonspread_ref_vga_dfifo_rst soft reset enabled
NONSPREAD_REF_VGA_VGAC_SOFT_RESET	9	0x0	0=nonspread_ref_vga_vgac_rst soft reset disabled 1=nonspread_ref_vga_vgac_rst soft reset enabled
NONSPREAD_REF_VGA_I2C_SOFT_RESET	10	0x0	0=nonspread_ref_vga_i2c_rst soft reset disabled 1=nonspread_ref_vga_i2c_rst soft reset enabled

Soft reset bits for the VGA domains

EC_CLK_MUX_CNTL - RW - 32 bits - DPCD_VGA:0x88018			
Field Name	**Bits**	**Default**	**Description**
VGAC_CLK_MUX_USE_SW	4	0x0	0=hardware will control vgac_clk mux 1=hardware will control vgac_clk mux
VGAC_CLK_MUX_CLKSEL_SW	5	0x0	0=value of vgac_clk mux select 1=value of vgac_clk mux select
LS_CLK_MUX_USE_SW	8	0x0	0=hardware will control ls_clk mux 1=hardware will control ls_clk mux
LS_CLK_MUX_CLKSEL_SW	9	0x0	0=value of ls_clk mux select 1=value of ls_clk mux select
SPREAD_REF_CLK_SEL_SW	11	0x0	0=select alwayson 100MHz clock 1=select phy 100MHz clok

EC Clock Mux Control

EC_DEBUG_CLKMUX_SEL - RW - 32 bits - DPCD_VGA:0x8801C			
Field Name	**Bits**	**Default**	**Description**
DEBUG_CLKMUX_SEL	3:0	0x0	0=Select which clock goes to the LVDS PHY IPIXCLK port for debug purposes

Debug Clock Selection

EC_DACPM_CONTROL - RW - 32 bits - DPCD_VGA:0x88020			
Field Name	**Bits**	**Default**	**Description**
DAC_DISABLE_HARDWARE_SEQUENCER	0	0x0	Disable DAC hardware power sequence. 1: software power sequence 0:hardware power sequence

DAC PM Control

EC_DACPM_DAC_WAIT_COUNT - RW - 32 bits - DPCD_VGA:0x88024			
Field Name	**Bits**	**Default**	**Description**
DAC_WAIT_COUNT	11:0	0x0	This counter controls the delay between off state and wait state of DAC power on FSM, for DAC analog macro power on sequence

DAC PM WAIT Count

EC_DACPM_DAC_BANDGAP_ON_COUNT - RW - 32 bits - DPCD_VGA:0x88028			
Field Name	**Bits**	**Default**	**Description**
DAC_BANDGAP_ON_COUNT	11:0	0x64	This counter controls the delay between wait state and falling edge of BGSLEEP for DAC analog macro power on sequence

DAC PM Bandgap On Count

EC_DPLLPM_CONTROL - RW - 32 bits - DPCD_VGA:0x88030			
Field Name	**Bits**	**Default**	**Description**
DPLL_DISABLE_HARDWARE_SEQUENCER	0	0x0	Disable DPLL hardware power sequence. 1: software power sequence 0: hardware power sequence
DPLL_USE_REGISTER_VALUES	1	0x0	Override DPLL parameters setting by register flag 1: set DPLL parameters by programmable register 0: set DPLL parameters by internal calculating
DPLL_REPROGRAM_ON_DFIFO_RESET	2	0x0	Indicates whether DFIFO reset reprograms DPLL or not 1: DFIFO reset reprograms DPLL 0: DFIFO reset does not reprogram DPLL
DPLL_FORCE_REPROGRAM	3	0x0	DPLL software force reprogram bit
DPLL_USE_LOCK_COUNT	4	0x0	Flag indicates which counter is used to count DPLL lock period in HW sequence mode 1: using EC internal counter 0: using counter inside DPLL core
DPLL_FORCE_DPLL_ON	5	0x0	Force to turn on clock mux to select DPLL outputs in HW sequence mode 1: force to select DPLL output clock 0: auto select internal clock, when DPLL unlocked uses default clock, after DPLL locked switches to DPLL output clock
DPLL_HW_SEQ_PLL_OFF	6	0x0	Bit to turn off DPLL in HW sequence mode

DPLL PM Control

EC_DPLLPM_DPLL_REGULATOR_SETTLING_COUNT - RW - 32 bits - DPCD_VGA:0x88034			
Field Name	**Bits**	**Default**	**Description**
DPLL_REGULATOR_SETTLING_COUNT	11:0	0x33	DPLL PM Regulator Settling Count in micro-second

DPLL PM Regulator Settling Count

EC_DPLLPM_DPLL_LOCK_COUNT - RW - 32 bits - DPCD_VGA:0x88038			
Field Name	**Bits**	**Default**	**Description**
DPLL_LOCK_COUNT	11:0	0x64	DPLL PM Lock Count in micro-second

DPLL PM Lock Count

EC_DPLLPM_MEASURE_COUNT - RW - 32 bits - DPCD_VGA:0x8803C			
Field Name	**Bits**	**Default**	**Description**
MEASURE_COUNT	11:0	0x20	HW mode MA measuring clock count in micro-second

DPLL PM Clock Measure Count

EC_DPLLPM_SOF_COUNT - RW - 32 bits - DPCD_VGA:0x88040			
Field Name	**Bits**	**Default**	**Description**
SOF_COUNT	2:0	0x2	Frame count before start in HW mode
SOF_US_COUNT	27:16	0x0	Micro-second count before start in HW mode

DPLL PM Start of Frame Count

EC_DPLLPM_MULTIPLIER_OFFSET - RW - 32 bits - DPCD_VGA:0x88044			
Field Name	**Bits**	**Default**	**Description**
MULTIPLIER_OFFSET	15:0	0x0	Adds an offset error to the PLL calculation (for debug)

Adds an offset error to the PLL calculation (for debug)

EC_REF_CLK_RATE - RW - 32 bits - DPCD_VGA:0x88048			
Field Name	**Bits**	**Default**	**Description**
REF_CLK_RATE	26:0	0x17d7840	Reference Clock Frequency in Hz

Reference Clock Frequency in Hz

EC_REF_CLK_RATE_MHZ - RW - 32 bits - DPCD_VGA:0x8804C			
Field Name	**Bits**	**Default**	**Description**
REF_CLK_RATE_MHZ	6:0	0x19	Reference Clock Frequency in MHz

Reference Clock Frequency in MHz

EC_PIXEL_RATE - RW - 32 bits - DPCD_VGA:0x88050			
Field Name	**Bits**	**Default**	**Description**
PIXEL_RATE (R)	28:0	0x0	Pixel clock rate, calculated pixel rate in Hz

Calculated pixel rate in Hz

EC_LS_CLK_RATE - RW - 32 bits - DPCD_VGA:0x88054			
Field Name	**Bits**	**Default**	**Description**
LS_CLK_RATE (R)	28:0	0x0	LS clock rate, calculated LS_CLK rate in Hz

Calculated ls_clk rate in Hz

EC_DPLL_POST_DIV - RW - 32 bits - DPCD_VGA:0x88058			
Field Name	**Bits**	**Default**	**Description**
DPLL_POST_DIV (R)	6:0	0x0	Calculated display PLL post divider by internal measuring logics

Calculated display PLL post divider

EC_DPLL_FB_DIVIDER - RW - 32 bits - DPCD_VGA:0x8805C			
Field Name	**Bits**	**Default**	**Description**
DPLL_FB_DIVIDER_FRACTION (R)	19:0	0x0	Calculated fraction part of display PLL feedback divider by internal measuring logics
DPLL_FB_DIVIDER_INTEGER (R)	31:20	0x0	Calculated integer part of display PLL feedback divider by internal measuring logics

Calculated display PLL feedback divider

EC_DPLL_VCO_TARGET - RW - 32 bits - DPCD_VGA:0x88060			
Field Name	**Bits**	**Default**	**Description**
DPLL_VCO_TARGET	29:0	0x3e95ba80	Target frequency for the VCO (should center in PLL range), set by programmable register

Target frequency for the VCO (should center in PLL range)

EC_PCIEPM_CONTROL - RW - 32 bits - DPCD_VGA:0x88070			
Field Name	**Bits**	**Default**	**Description**
PCIE_DISABLE_HARDWARE_SEQUENCER	0	0x0	Disable PCIe hardware power sequence. 0: hardware power sequence 1: software power sequence

PCIE PM Control

EC_PCIEPM_PCIE_WAIT_COUNT - RW - 32 bits - DPCD_VGA:0x88074			
Field Name	**Bits**	**Default**	**Description**
PCIE_WAIT_COUNT	11:0	0x0	When hardware sequencer is enabled, there will be a time delay that is equal to this value * 40 ns, between completely off and the turning on of the frontend. (The counter is based on a 25MHz reference clock)

PCIE PM WAIT Count

EC_PCIEPM_PCIE_FRONTEND_ON_COUNT - RW - 32 bits - DPCD_VGA:0x88078			
Field Name	**Bits**	**Default**	**Description**
PCIE_FRONTEND_ON_COUNT	11:0	0x1f	When in hardware sequencer mode, provides the last time of rx_frontend_en = 1. (Tthe counter is based on a 25MHz reference clock)

PCIE PM FRONTEND On Count

EC_PCIEPLLPM_CONTROL - RW - 32 bits - DPCD_VGA:0x88080			
Field Name	**Bits**	**Default**	**Description**
PCIEPLLPM_DISABLE_HARDWARE_SEQUENCER	0	0x0	Disable PCIEPLL hardware power sequencer. 0: Hardware power sequencer 1: Software power sequencer

PCIE PLL PM Control

EC_DPLLPM_DPLL_WAIT_VREG_RESET_COUNT - RW - 32 bits - DPCD_VGA:0x88084			
Field Name	**Bits**	**Default**	**Description**
DPLL_WAIT_VREG_RESET_COUNT	11:0	0x2	DPLL PM Wait Vreg Reset Count in micro-seconds

DPLL PM Wait Vreg Reset Count

EC_DPLLPM_DPLL_VREG_RESET_COUNT - RW - 32 bits - DPCD_VGA:0x88088			
Field Name	**Bits**	**Default**	**Description**
DPLL_VREG_RESET_COUNT	11:0	0x2	DPLL PM Vreg Reset Count in micro-seconds

DPLL PM vreg reset count

EC_DPLLPM_DPLL_BIAS_POWERUP_COUNT - RW - 32 bits - DPCD_VGA:0x8808C			
Field Name	**Bits**	**Default**	**Description**
DPLL_BIAS_POWERUP_COUNT	11:0	0x1f5	DPLL PM bias power up count in micro-seconds

DPLL PM bias powerup count

EC_DACPM_DAC_LDO_ON_COUNT - RW - 32 bits - DPCD_VGA:0x88090			
Field Name	**Bits**	**Default**	**Description**
DAC_LDO_ON_COUNT	11:0	0x3e8	This counter controls the delay between the falling edge of BGSLEEP and the falling edge of LDO_PDN for DAC analog macro power on sequence

DAC PM LDO On Count

EC_DACPM_DAC_RGBDAC_ON_COUNT - RW - 32 bits - DPCD_VGA:0x88094			
Field Name	**Bits**	**Default**	**Description**
DAC_RGBDAC_ON_COUNT	11:0	0x3e8	This counter controls the delay between the falling edge of LDO_PDN and the falling edge of RGBDAC_on for DAC analog macro power on sequence

DAC macro RGB channel On Count

dbgmux_control - RW - 32 bits - DPCD_VGA:0x88180			
Field Name	**Bits**	**Default**	**Description**
muxsel	3:0	0xf	Specify which block's debug outputs go to the debug multiplexer outputs 0=PCIE_BUS 1=PCIE_RX_PLL_PM 2=dfifo_vga 3=PCIE_RX_VGA_PM 4=dprl_bus 5=reserved05 6=reserved06 7=auxSlvVga 8=reserved08 9=vgac_dispc 10=ec_dbg_bus 11=reserved11 12=vgai2c_bus 13=vgac_dacc 14=dpll_debug 15=reserved15
clksel	5:4	0x3	Specify which clock source go to clock spread outputs 0=NonSpread REF clock 1=PPLL_CORE_DBGCLK 2=PPLL_CORE_PIXCLK 3=reserved

Control Register for the Debug Multiplexer

dbgmux_zoomcontrol - RW - 32 bits - DPCD_VGA:0x88184			
Field Name	**Bits**	**Default**	**Description**
decimation_rate	3:0	0x0	Specify the zoomer decimation rate, 0 bypass; 1 decimation rate = 2; 3 decimation rate = 4; 7 decimation rate = 8
decimation_phase	7:4	0x0	Specify the sample phase of decimation
zoom_mode	11:8	0x0	Specify the zoomer mode: 0 bypass; 1 signal bandwidth x 2; 2 signal bandwidth x 4; 3 signal bandwidth x 8
zoom_base	16:12	0x0	Specify the begin point of zoom window
ec_clk_sel	20	0x0	Specify the selection of debug bus and EC clock group,0 debug bus; 1 EC clock group
ec_clk_phs	23:21	0x0	Specify the phase of EC clock group, from phase 0 ~ 7
zoom_disable	24	0x1	When set disable zoomer

Control Register for the Zoomer in Debug Multiplexer

dbgmux_gpiocontrol - RW - 32 bits - DPCD_VGA:0x88188			
Field Name	**Bits**	**Default**	**Description**
dbg_gpio_mode	1:0	0x0	specity the GPIO usage mode 0=function_mode 1=slow_speed_mode 2=dbgclk_out_mode 3=reserved

Control Register for Nutmeg tile GPIO mode

The IMC message registers are designed as a logical device in the FCH that complies with the Plug and Play ISA Specification. The device number of the message device is 9 and it is set up through the following global and local configuration registers.

7.1 Global Configuration Registers

Address	Type	Port Name
0x02	Write Only	Config Control Set bit[0] to cause Soft Reset. No need to clear. Deactivates the devices and resets the global and device registers to their default values.
0x07	Read/Write	Logical Device Number This register is for selecting the current logical device.
0x20	Read Only	Device ID
0x21	Read Only	Revison ID

7.2 Local Configuration Registers

Address	Register Name	Type	Register Description
0x30	Activate	R/W	Set bit[0] to activate this logical device
0x60	MSG9 Base Addr High Byte	R/W	MESSAGE9_BASE (high byte)
0x61	MSG9 Base Addr Low Byte	R/W	MESSAGE9_BASE (low byte) - Bit[0] is read-only 0.
0x70	MSG Interrupt Type Byte	R/W	Type of interrupt sent to host when IMC firmware writes the MSG_IMC_TO_SYS register: 00b: SMI (default) 01b: No Interrupt 10b: IRQ – the specific IRQ is programmed in ACPI register space. 11b: No interrupt

The configuration registers are accessed through the 8-bit Config port using an index and data register mechanism. The I/O address of the Config port can be read from the IMC_PortActive field in the FCH LPC ISA bridge PCI configuration register A4h.

Note that the IMC firmware will set IMC_PortActive to 0x6E once the IMC is enabled because the power-up default value of 0x2E is usually used by most super IO controllers. Therefore, an I/O conflict may occur when IMC and the super IO controller are used together. If the value picked by the IMC firmware is still not suitable for the design, platform BIOS developers can change it by programming the IMC_PortActive field of the FCH LPC ISA bridge PCI configuration register A4h to the desired address.

IMC_PortAddress- R/W - 16 bits - [PCI_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
IMC_PortActive	0	1b	When sets it to 1, LPC can decode the address specified in IMC_PortAddress otherwise LPC ignores it.
Addr15_1	15:1	0017h	When Addr15_1 is non-zero, and if an IO cycle from host has address[15:1] = Addr15_1, the cycle will be routed to IMC instead of to LPC bus. By default, address[15:0] = 002Eh or 002Fh will be routed. Read-only to host if IMC_PortHostAccessEn = 0.

Per the PnP ISA specification, the logical device must be placed in the Config state before accessing any configuration registers (achieved by writing the value 0x5A to the Config port). Once the logical device has entered the Config state, all the configuration registers can be accessed through the Config Port using an index and data register addressing mechanism. After the configuration register access is completed, write 0xA5 to the Config port to transit the logical device out of the Config state.

7.3 IMC Message Registers

Since the activation of Logical Device Number 9 and the address assignment of the Message Registers are handled by CIMx during the IMC enabling process, the host software needs only to read the value of MESSAGE9_BASE register (local configuration register 0x60 & 0x61) in order to access the IMC Message Registers.

There are 16 message registers available in the message register device, each with a unique index value for access through the Message Base register using the index and data register addressing mechanism. These message registers are the backbone of the IMC Message Function Software Interface.

Index	**Register Name**	**Type**	**Register Description**
0x80	MSG_SYS_TO_IMC	R/W	System to IMC Message data
0x81	MSG_IMC_TO_SYS	RO	IMC to System Message data
0x82	MSG_REG0	R/W	IMC Message storage 82
0x83	MSG_REG1	R/W	IMC Message storage 83
0x84	MSG_REG2	R/W	IMC Message storage 84
0x85	MSG_REG3	R/W	IMC Message storage 85
0x86	MSG_REG4	R/W	IMC Message storage 86
0x87	MSG_REG5	R/W	IMC Message storage 87
0x88	MSG_REG6	R/W	IMC Message storage 88
0x89	MSG_REG7	R/W	IMC Message storage 89
0x8A	MSG_REG8	R/W	IMC Message storage 8A
0x8B	MSG_REG9	R/W	IMC Message storage 8B
0x8C	MSG_REGA	R/W	IMC Message storage 8C
0x8D	MSG_REGB	R/W	IMC Message storage 8D
0x8E	MSG_REGC	R/W	IMC Message storage 8E
0x8F	MSG_REGD	R/W	IMC Message storage 8F

7.4 IMC Message Register Software Interface

The IMC Message Register Software interface is defined below. The host software is required to check for IMC presence before calling the interface functions; otherwise the caller will have to rely on the 50-ms time-out in receiving the function acknowledge returning in Msg_Reg0 to determine whether the call is serviced or not.

7.4.1 IMC Enable Options

The IMC enable information can be obtained by utilizing one of the following three options:

1) IMCEnableStrap Bit of the StrapStatus Register (Misc_Reg 80h)

The IMCEnableStrap bit, which represents the hardware IMC enable status, is the recommended approach. The register is accessed at the memory mapped location AcpiMMioAddr (PMIO_24) + 0E80h. The power-up default value of AcpiMMioAddr is 0FED80000h. It usually remains unmodified by CIMx; therefore, a segment selector with 4 GB access limit is needed to access the StrapStatus register which may not be available in some software environments.

StrapStatus – R 8/16/32 bits - [Misc_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
FWHDisableStrap	0	0b	EcPwm3 pad
UseLpcRomStrap	1	1b	Inverted version from EcPwm2 pad Note: Both EcPwm3 and EcPwm2 straps pins are used to select boot ROM type.
IMCEnableStrap	**2**	**0b**	**IMC is enabled if this bit is 1**
BootFailTmrEnStrap	3	0b	Enable Watchdog function
ClkGenStrap	4	0b	Select 25Mhz crystal clock or 100Mhz PCI-E clock
DefaultModeStrap	5	1b	Select default debug straps
Reserved	6	-	Reserved
I2CRomStrap	7	0b	Getting A-Link Express-II core strap from I2C ROM or using default value
ILAAutorunEnBStrap	8	1b	Enable trace memory auto run feature
FcPllBypStrap	9	1b	Bypass FC clock
PciPllBypStrap	10	0b	Bypass PCI PLL (used in functional test at tester)
ShortResetStrap	11	1b	Genearate short reset
Reserved	12	1b	PCI_ROM_BOOT strap
FastBif2cClkStrap	13	0b	Select fast BIF EPROM clocks
Reserved	14	-	Reserved
BlinkSlowModestrap	15	0b	Blink slow mode (100Mhz blink clock) strap
BIF_GEN2_COMPLIANCE_Strap	16	0b	BIF gen 2 compliance strap
Reserved	31:17	4'h0000	Reserved

2) Message Register Logical Device Activation Bit

Since CIMx will not initialize the Message Register logical device if the IMC is not enabled, the activation bit should stay at the power-up default value of 0 (i.e., disabled). As a result, this bit can be used as an indirect method for checking IMC presence. This method may be easier since only I/O instructions are involved, but it is less accurate than the IMCEnableStrap method because it is essentially an indirect approach relying on CIMx handling.

3) Message Register Index Register Base Address

This approach is similar to the logical device activation bit in option 2 above, however, only the Message Register Index Register is checked for the power on default value (0, disabled). This relies on CIMx not initializing the base address of the Message Register index register if the IMC is not enabled (with the same limitation as option 2).

7.4.2 IMC Message Functions Description

Function 0x80: Get IMC Thermal Zone Information

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x80 – Get IMC Thermal Zone Information
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	Bit[2:0]: Zone Number, only 0 to 4 is valid.

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Bit[2:0]: Zone number is preserved. Bit[5-3] : Current Decimal Temperature Value This field returns the decimal portion of the temperature in the units of 0.125 degree Celsius Other bits are reserved.
MSG_REG2	BYTE	Thermal zone control byte 1. Bit 0: Set to 1 if this thermal zone is enabled. Bit 1: Reserved. Bit 2: Set to 1 if the fan is controlled by IMC Bit 3: Reserved. Bit 4: Set to 1 if the fan speed is in linear mode, 0 for step mode Bit[7:5]: FANOUT signal used by this zone 0 - No fan is used by this zone 1 - Fan is driven by FANOUT0 output. 2 - Fan is driven by FANOUT1 output. 3 - Fan is driven by FANOUT2 output. 4 - Fan is driven by FANOUT3 output. 5 - Fan is driven by FANOUT4 output Other values are reserved. Note: 1. The fan speed can be controlled through function 0x86 manually if bit 2 is equal to 0

Field	Format	Description
MSG_REG3	BYTE	Thermal zone control byte 2 Bit[2:0]: Temperature sensor used by this zone 0 - No temperature sensor is used 1 - AMD FCH TEMPIN0 2 - AMD FCH TEMPIN1 3 - AMD FCH TEMPIN2 4 - AMD FCH TEMPIN3 5 - AMD FCH IntTEMP 6 - AMD sideband temperature sensor interface (SB-TSI), or ADM1032 remote temperature channel , or MAX6642 remote temperature channel, or ADT7461 remote temperature channel, or ADT7475 remote 1 sensor 7 - ADM1032 local temperature channel , or MAX6642 local temperature channel, or ADT7461 local temperature channel, or ADT7475 remote 2 sensor Bit[5:3]: Fan tachometer used by this zone 0 - No fan tachometer is used 1 - AMD FCH FANIN0 2 - AMD FCH FANIN1 3 - AMD FCH FANIN2 4 - AMD FCH FANIN3 5 - AMD FCH FANIN4 Other values are reserved Bit 6: Set to 1 to enable temperature averaging for the temperature sensor. Bit 7: Reserved.
MSG_REG4	BYTE	Thermal diode offset adjustment in degrees Celsius. This is a signed value (+127 to -127) for adjusting the raw temperature read from the temperature sensor to compensate for any inherent system offset such as PCB trace resistance.
MSG_REG5	BYTE	Hysteresis information (See note 2) Bit[3:0]: Active cooling hysteresis temperature in degree Celsius Bit[7:4]: Reserved Hysteresis is disabled if the value equal to 0.
MSG_REG6	BYTE	SMBUS Address for SMBus based temperature sensor such as SB-TSI and ADM1032. This parameter is not needed if the sensor is not a SMBus device. (See note 1)
MSG_REG7	BYTE	Bit[1:0]: The SMBus clock and data signal where the SMBUS based temperature sensor is connected. This parameter is not needed if the sensor is not a SMBus device. (See note 1) 0 = SCL0/SDA0 1 = SCL2/SDA2 2 = SCL3/SDA3 3 = SCL4/SDA4 Bit[7:3]: Reserved
MSG_REG8	BYTE	Fan PWM stepping rate in unit of PWM level percentage (0 to 100%) (See note 2)
MSG_REG9	BYTE	Fan PWM ramping rate in 5ms unit (See note 2) Ramping rate =0 to disable Fan PWM ramping and stepping
MSG_REGA	BYTE	Current Integer Temperature value. This field returns the integer portion of the temperature in degrees Celsius.
MSG_REGB	BYTE	Current PWM level in percentage (0 - 100%) (See note 2)
MSG_REGC	BYTE	Current Fan Speed in RPM (LSB) (See note 2)
MSG_REGD	BYTE	Current Fan Speed in RPM (MSB) (See note 2)

Note:

- The parameter returned in this register is only valid if SMBus based temperature sensor is used for the zone.
- The parameter returned in this register is only valid if FANOUT is assigned for the zone.

Function 0x81: Set IMC Thermal Zone Information

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x81 – Set IMC Thermal Zone Information
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	Bit[2:0]: Zone Number, only 0 to 4 is valid. (This call is effective only to the zones that is returned supported from function 0x80)
MSG_REG2	BYTE	Thermal zone control byte 1. Bit 0: Set to 1 to enable this thermal zone. Bit 1: Reserved, set to zero. Bit 2: Set to 1 if the fan is controlled automatically by IMC Bit 3: Reserved. Bit 4: Set to 1 if the fan speed is in linear mode, 0 for step mode Bit[7:5]: FANOUT signal used by this zone 0 - No fan is used by this zone 1 - Fan is driven by FANOUT0 output. 2 - Fan is driven by FANOUT1 output. 3 - Fan is driven by FANOUT2 output. 4 - Fan is driven by FANOUT3 output. 5 - Fan is driven by FANOUT4 output Other values are reserved. Note: 1. The fan speed can be controlled manually through function 0x86 if bit 2 is set to 0.

Field	Format	Description
MSG_REG3	BYTE	Thermal zone control byte 2 Bit[2:0]: Temperature sensor used by this zone 0 - No temperature sensor is used 1 - AMD FCH TEMPIN0 2 - AMD FCH TEMPIN1 3 - AMD FCH TEMPIN2 4 - AMD FCH TEMPIN3 5 - AMD FCH IntTEMP 6 - AMD sideband temperature sensor interface (SB-TSI), or ADM1032 remote temperature channel , or MAX6642 remote temperature channel, or ADT7461 remote temperature channel, or ADT7475 remote 1 sensor 7 - ADM1032 local temperature channel , or MAX6642 local temperature channel, or ADT7461 local temperature channel, or ADT7475 remote 2 sensor Bit[5:3]: Fan tachometer used by this zone 0 - No fan tachometer is used 1 - AMD FCH FANIN0 2 - AMD FCH FANIN1 3 - AMD FCH FANIN2 4 - AMD FCH FANIN3 5 - AMD FCH FANIN4 Other values are reserved Bit 6: Set to 1 to enable temperature averaging for the temperature sensor. Bit 7: Reserved.
MSG_REG4	BYTE	Bit[3:0] - Thermal diode offset adjustment in degrees Celsius. Bit[7-4] – Reserved
MSG_REG5	BYTE	Hysteresis information (see note 3) Bit[3:0]: Active cooling hysteresis temperature in degree Celsius Bit[7:4]: Reserved. Hysteresis is disabled if the value equal to 0.
MSG_REG6	BYTE	SMBUS Address for SMBus based temperature sensor such as SB-TSI and ADM1032. This parameter is not needed if the sensor is not a SMBus device. (see note 3)
MSG_REG7	BYTE	Bit[1:0]: The SMBus clock and data signal where the SMBUS based temperature sensor is connected. This parameter is not needed if the sensor is not a SMBus device. (see note 3) 0 = SCL0/SDA0 1 = SCL2/SDA2 2 = SCL3/SDA3 3 = SCL4/SDA4 Bit[7:3]: Reserved
MSG_REG8	BYTE	Fan PWM stepping rate in unit of PWM level percentage (0 to 100%) (see note 4)
MSG_REG9	BYTE	Fan PWM ramping rate in 5ms unit (see note 4) Ramping rate =0 to disable Fan PWM ramping and stepping

Note:

- The parameter is only needed if SMBus based temperature sensor is used for the zone.

- The parameter is only needed if FANOUT is assigned for the zone.

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged
MSG_REG2	BYTE	Unchanged
MSG_REG3	BYTE	Unchanged
MSG_REG4	BYTE	Unchanged
MSG_REG5	BYTE	Unchanged
MSG_REG6	BYTE	Unchanged
MSG_REG7	BYTE	Unchanged
MSG_REG8	BYTE	Unchanged
MSG_REG9	BYTE	Unchanged

Function 0x82: Read IMC Fan Policy Temperature Thresholds

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x82 – Read IMC fan policy temperature thresholds The function returns the temperature trip points at which different level of fan speeds are applied.
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	Bit[2:0]: Zone Number, only 0 to 4 is valid. (This call is effective only to the zones that is returned supported from function 0x80)

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged
MSG_REG2	BYTE	_AC0, the highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG3	BYTE	_AC1, the 2nd highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG4	BYTE	_AC2, the 3rd highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG5	BYTE	_AC3, the 4th highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG6	BYTE	_AC4, the 5th highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG7	BYTE	_AC5, the 6th highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG8	BYTE	_AC6, the 7th highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG9	BYTE	_AC7, the 8th or lowest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REGA	BYTE	_CRT, the critical threshold in degrees of Celsius.
MSG_REGB	BYTE	Reserved

Function 0x83: Set IMC Fan Policy Temperature Thresholds

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x83 – Set IMC fan policy temperature thresholds The function sets the temperature trip points at which different level of fan speed are applied.
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	Bit[2:0]: Zone Number, only 0 to 4 is valid. (This call is effective only to the zones that is returned supported from function 0x80)
MSG_REG2	BYTE	_AC0, the highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG3	BYTE	_AC1, the 2nd highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG4	BYTE	_AC2, the 3rd highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG5	BYTE	_AC3, the 4th highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG6	BYTE	_AC4, the 5th highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG7	BYTE	_AC5, the 6th highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG8	BYTE	_AC6, the 7th highest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REG9	BYTE	_AC7, the 8th or lowest temperature threshold in degrees of Celsius. This threshold is not defined if the value is equal to 0xFF
MSG_REGA	BYTE	_CRT, the critical threshold in degrees of Celsius.
MSG_REGB	BYTE	Reserved, set to 00h

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged
MSG_REG2	BYTE	Unchanged
MSG_REG3	BYTE	Unchanged
MSG_REG4	BYTE	Unchanged
MSG_REG5	BYTE	Unchanged
MSG_REG6	BYTE	Unchanged
MSG_REG7	BYTE	Unchanged
MSG_REG8	BYTE	Unchanged
MSG_REG9	BYTE	Unchanged

Function 0x84: Read IMC Fan Policy PWM Settings

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x84 – Read IMC fan policy PWM settings This function returns the FanOut PWM levels configured for the temperature trip points defined in function 0x83. The values are ranged from 0 to 100%, 0% PWM level means the fan is turned off and 100% means the fan is driven to full speed.
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	Bit[2:0]: Zone Number, only 0 to 4 is valid. (This call is effective only to the zones that is returned supported from function 0x80)

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged
MSG_REG2	BYTE	_AL0 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC0 temperature is reached.
MSG_REG3	BYTE	_AL1 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC1 temperature is reached.
MSG_REG4	BYTE	_AL2 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC2 temperature is reached.
MSG_REG5	BYTE	_AL3 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC3 temperature is reached.
MSG_REG6	BYTE	_AL4 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC4 temperature is reached.
MSG_REG7	BYTE	_AL5 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC5 temperature is reached.
MSG_REG8	BYTE	_AL6 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC6 temperature is reached.
MSG_REG9	BYTE	_AL7 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC7 temperature is reached.

Note: The PWM information is only meaningful for the temperature trip points defined in function 0x83.

Function 0x85: Set IMC Fan Policy PWM Settings

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x85 – Set IMC fan policy PWM settings This function sets the FanOut PWM levels for the temperature trip points defined in function 0x83. The values are ranged from 0 to 100%, 0% PWM level means the fan is turned off and 100% means the fan is driven to full speed.
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	Bit[2:0]: Zone Number, only 0 to 4 is valid. (This call is effective only to the zones that is returned supported from function 0x80)
MSG_REG2	BYTE	_AL0 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC0 temperature is reached.
MSG_REG3	BYTE	_AL1 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC1 temperature is reached.
MSG_REG4	BYTE	_AL2 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC2 temperature is reached.
MSG_REG5	BYTE	_AL3 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC3 temperature is reached.
MSG_REG6	BYTE	_AL4 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC4 temperature is reached.
MSG_REG7	BYTE	_AL5 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC5 temperature is reached.
MSG_REG8	BYTE	_AL6 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC6 temperature is reached.
MSG_REG9	BYTE	_AL7 PWM level in percentage (0 – 100%) This the fan speed to be applied when _AC7 temperature is reached.

Note: The PWM value should be set for every valid temperature trip points defined in function 0x83, the rest of the PWM values can be set to 0.

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged
MSG_REG2	BYTE	Unchanged
MSG_REG3	BYTE	Unchanged
MSG_REG4	BYTE	Unchanged
MSG_REG5	BYTE	Unchanged
MSG_REG6	BYTE	Unchanged
MSG_REG7	BYTE	Unchanged
MSG_REG8	BYTE	Unchanged
MSG_REG9	BYTE	Unchanged

Function 0x86: Set Fan Speed

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x86 – Set fan speed This function is for setting fan to a specified speed, but it only works for the zones which the fan is not configured to be controlled automatically by IMC. (i.e. Bit 2 of thermal control byte 1 is equal to 0)
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	Bit[2:0]: Zone Number, only 0 to 4 is valid. (This call is effective only to the zones that is returned supported from function 0x80)
MSG_REG2	BYTE	When fan is control manually ((Thermal control byte 1[2:1] = 00b) Bit[7:0] = 0 – 100, fan PWM level in percentage This function is not effective when the fan is controlled by IMC (Thermal control byte 1[2:1] = 10b)

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged
MSG_REG2	BYTE	Unchanged

Function 0x89: Set HWM TEMPIN Calculation Parameters

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x89 – Set HWM TEMPIN Calculation Parameters This function provides the critical parameters of the HWM TempIn sensors, IMC would not perform temperature measurement using those sensors until the parameters are provided.
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	TEMPIN channel Number
MSG_REG2-5	DWORD	At (original value in BIOS multiply by 65536)
MSG_REG6-9	DWORD	Ct (original value in BIOS multiply by 256)
MSG_REGA	BYTE	TEMPIN tuning parameter (i.e. PMIO2_FF[7:6] setting) Bit[1:0] = 0 – Default mode = 1 – High current ratio = 2 – High current Bit[2] = Set to 1 to disable filtering in TEMPIN calculation Other bits are reserved.

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged
MSG_REG2-5	DWORD	Unchanged
MSG_REG6-9	DWORD	Unchanged
MSG_REGA	BYTE	Unchanged

Function 0x8A: Get HWM TEMPIN Calculation Parameters

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x8A – Get HWM TEMPIN Calculation Parameters This function reads the HWM TEMPIN parameters submitted by the last function 0x89 call.
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	TEMPIN channel Number

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged
MSG_REG2-5	DWORD	At (original value in BIOS multiply by 65536)
MSG_REG6-9	DWORD	Ct (original value in BIOS multiply by 256)
MSG_REGA	BYTE	Bit[1:0] = 0 – Default mode = 1 – High current ratio = 2 – High current Bit[2] = Set to 1 to disable filtering in TEMPIN calculation Other bits are reserved.

Function 0x96: IMC Enter/Exit Scratch RAM (ROM Ownership Semaphore)

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x96 – Enter/Exit Scratch RAM This function instructs the IMC to stop or resume fetching from the BIOS ROM, it should be called by the host software before and after the BIOS ROM writing operation.
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	Sub-function value 0xB4 – Enter Scratch RAM This sub-function should be called before a BIOS ROM writing operation. 0xB5 – Exit Scratch RAM without RESET system This sub-function should be called after a BIOS ROM writing operation. 0xB6 – Exit Scratch RAM and RESET system This sub-function should be called after a BIOS ROM writing operation and a system reset is desired

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged.

Function 0x98: IMC Enter IDLE State

Arguments:

Field	Format	Description
MSG_SYS_TO_IMC	BYTE	0x98 – Enter IDLE state This function instructs IMC to prepare itself for the system to enter ACPI S3, S4 or S5 state.
MSG_REG0	BYTE	0x00
MSG_REG1	BYTE	Sub-function value 0x01 – Enter IDLE whenever system go to S3/S4/S5

Output:

Field	Format	Description
MSG_REG0	BYTE	Function status. 0x00: Function not supported 0xFA: Function completed, firmware may take up to 50ms to return the status.
MSG_REG1	BYTE	Unchanged.