AMD A45/A50M/A55E
Fusion Controller Hub
Register Programming Requirements

Technical Reference Manual
Rev. 3.00

P/N: 47778_ A45_A50M_A55E _rpr_pub_3.00

.

Trademarks

Disclaimer

Table of Contents

1 Introduction

1.1 About This Manual

This document lists the register settings required for the proper operation of the AMD family of Fusion Controller Hub (FCH) codenamed Hudson-1.

Note: The term Hudson-1 is used throughout this document to refer to the following Hudson-1 family members:

Marketing Name	Codename
A45	Hudson-D1
A50M	Hudson-M1
A55E	Hudson-E1

The information in this document applies to all members of the Hudson-1 family unless otherwise indicated. For feature differences distinguishing these variants, please refer to their respective databooks.

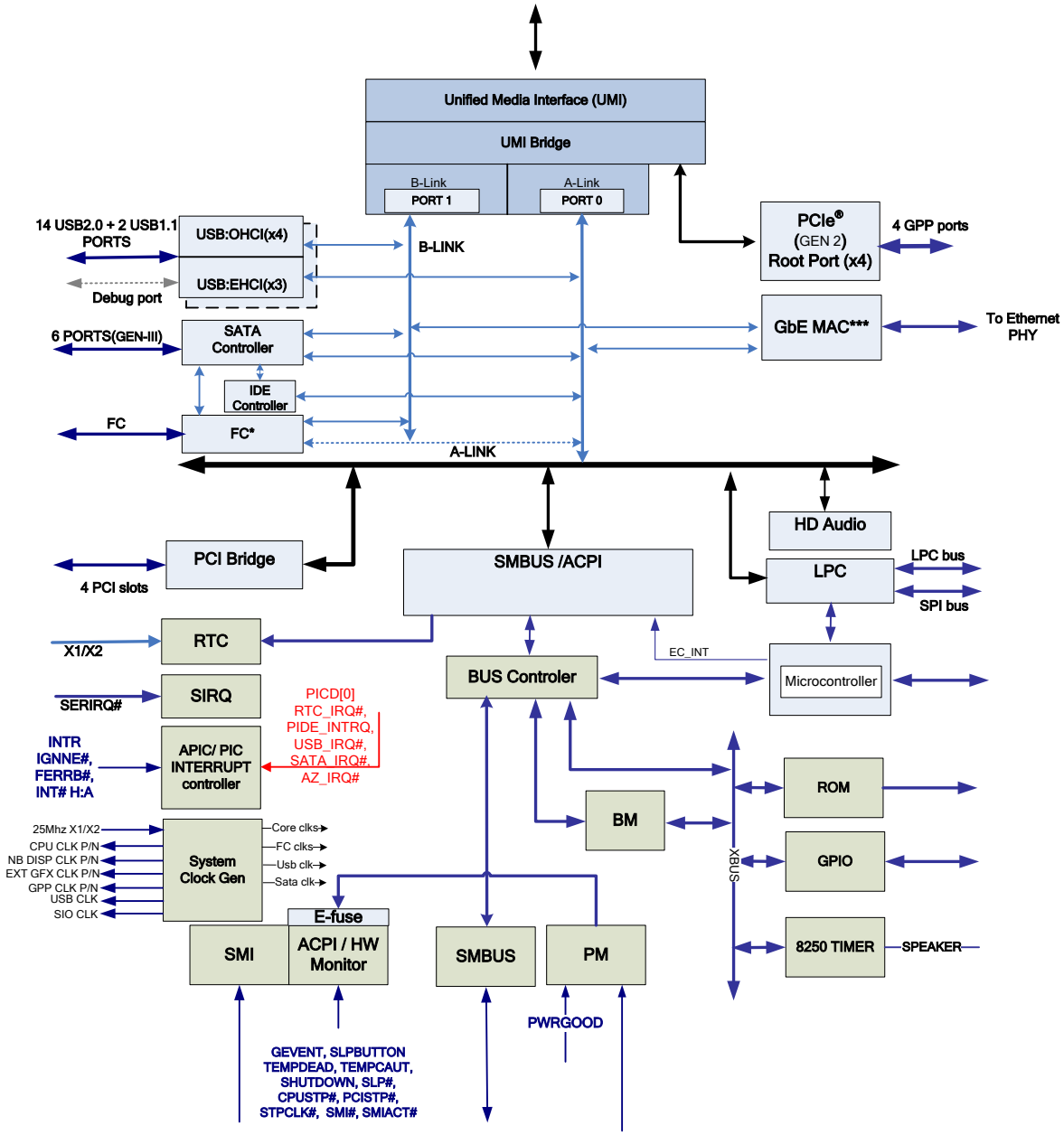
Most of the register settings are mandatory and should be implemented as described in this document. The document will be updated periodically with new or revised settings that are determined during the qualification of the Hudson-1 FCH. Please refer to the latest updated document on the AMD NDA site.

This document should be used in conjunction with the related *AMD A45/A50M/A55E Fusion Controller Hub BIOS Developer's Guide* and the *AMD A45/A50M/A55E Fusion Controller Hub Register Reference Guide.*

Note: In this document, changes/additions from the previous release are highlighted in red. Refer to the *Appendix: Revision History* at the end of this document for a detailed revision history.

1.2 AMD Hudson-1 Block Diagram

Figure 1 below shows the Hudson-1 internal PCI devices and major functional blocks.



Notes:
* Flash controller function is not supported on Hudson-1 platforms.
** PCI controller function is not supported on Hudson-M1 platforms.
*** GbE MAC is not supported

Figure 1 Hudson-1 Internal PCI Devices and Major Functional Blocks

1.3 How to Read the Information in this Document

Tables within this document contain information showing the applicable revision(s), recommended settings, and comments associated with the register. Consider the following example:

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_IO 0x52 [5:0] = 0x08	Recommended delay for S3/S4/S5 resume sequence

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide.
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		X						

- ASIC Rev → Hudson-1 All Revs = Applicable to all revisions of the Hudson-1.
- Register Settings → Recommended register settings with the register address and controlling bits.

For more detailed information about the registers found within this document, refer to the *AMD A45/A50/A55M Register Reference Guide*. The applicable sections in the register reference guide where the information can be found are marked with "x" in the tables in this document.

2 ACPI/SMBUS Controller (bus-0, dev-20, fun-0)

2.1 Revision ID

ASIC Rev	Register Settings	Function/Comment
Hudson-1 A11	Smbus_pci_config 0x08 = 0x40	Revision ID for Hudson-1 revision A11
Hudson-1 A12	Smbus_pci_config 0x08 = 0x41	Revision ID for Hudson-1 revision A12
Hudson-1 A13	Smbus_pci_config 0x08 = 0x42	Revision ID for Hudson-1 revision A13

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
		x						
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

2.2 ACPI Memory Mapped I/O Enable

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_reg 0x24 [0] = 1	Enable ACPI Memory mapped I/O space. In Hudson-1, PM_reg can be accessed through the indirect I/O space (CD6/CD7) or memory mapped I/O. The default is indirect I/O. SBIOS needs to set the "AcpiMMioDecodeEn" bit for memory mapped I/O access.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

2.3 MMIO Programming for Legacy Devices

The legacy devices LPC, IOAPIC, ACPI, TPM and Watchdog Timer require the base address of the Memory Mapped I/O registers to be assigned before these logic blocks are accessed. The Memory Mapped I/O register base address and its entire range should be mapped to non-posted memory region by programming the CPU register. See Hudson-1 BIOS Developer's Guide for details.

2.4 Programming C-State Transition Message in FCH

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_Reg 0xA0[0] = 1	Enable AC/DC change message delivery.
	PM_Reg 0xA0[1] = 1	Enable TimerTick tracking.
	PM_Reg 0xA0[10] = 1	Enable tag on clock interrupt.
	PM_Reg 0x A0[15:12] = 1111b	Configure the handling of USB traffic. [13] exit C-state upon OHCI traffic [15] exit C-state upon EHCI traffic
	PM_Reg 0x A0[30:24] = 011_1111b	Configure the extended break event timer.
	PM_Reg 0x A0[11] = 1	
	PM_Reg 0xA0[23] to 1	Enable Fusion message C-state multi-core support.
	PM_Reg 0xA0[6] to 1	Enable Fusion message C-state.
	PM_Reg 0xA0[4] to 1	
	PM_Reg 0xA0[3] to 1	

	If EC is enabled {
	PM_Reg 0xA0[8] to 1
	PM_Reg 0xA0[9] to 1
	}	

	PM_Reg 0xA0[2] to 1	

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

2.5 Mt C1e Enable

ASIC Rev	Register Settings	Function/Comment
The programming below is required when Mt C1e is enabled on the CPU side.		
Hudson-1 All Revs	PM_Reg 0x7A [15] = 1 PM_Reg 0x7A [3:0] = xxxxb PM_Reg 0x80[13] = 1 PM_Reg 0x80[7] = 1	Set bit 15 to 1 to enable Mt C1e message decoding. Program bits[3:0] to reflect CPUs or CPU core pairs in the system. This is used to specify how core message contributes one Mt C1e transition. Typically it is set to 1 for supporting Mt C1e. Set to 1 to enable Mt C1e protocol.
The following registers should be programmed only if FIDVID is also enabled in conjunction with MTC1e.		
Hudson-1 All Revs	PM_Reg 0x7E [6] = 0 PM_Reg 0x80 [4] = 0	CpopUpEn Is disabled EnableBreak is disabled

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	A-LINK	I/O REG	XIOAPIC			
		x						

2.6 HPET MSI Setting

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_reg x50 [4:2] = 000b	Program these register bits ONLY if the following are true in the platform configuration: - Legacy Floppy Drive interface supported. - Legacy FIR device supported.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

2.7 CPU PwrGood Setting

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_reg xC1 [3] = 1b	Set this bit to 1 so CpuPwrGd (LdtPwrGd) will be deasserted when SLP_S3# is asserted.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

2.8 SMAF Matching Setting

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_reg x08[7] = 1b	This bit must be set to cover a corner case of concurrent throttling and C1e.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

2.9 Keyboard Reset Settings for Legacy Free Systems

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_reg xBE[1] = 1b	This bit must not be programmed by the BIOS. It should be left with the power up default value of 1.
	Depends on system configuration: Case 1: PM_reg xBE[4] = 0b Case 2: PM_reg xBE[4] -> Leave at power-up default setting.	Case 1 This bit must be cleared by the platform system BIOS if the KBRST#/ GEVENT1# I/O pin is not connected to system keyboard reset or is configured as GEvent1 function. (Note: CIM-x does not support call back function to clear this bit.) Case 2 For all other cases, the bit should not be programmed by the BIOS. It should remain at the power-up default setting.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

2.10 NB Power Good Control on System Reset

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_reg xC0[21] = 1b	This bit must be set if system configuration uses internal clock generator for normal operation. For external clock mode, BIOS does not need to program this bit.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

2.11 HWM Sensor Clk

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM2_reg xEF[3:0] = 1010'b PM2_reg xFF[1:0] = 10'b	These settings are required to make HWM work properly.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM2_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		X						

2.12 PCIe® Native Mode

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_reg x77[2:0] = 101'b	This setting is required to support PCIe® native mode. Otherwise it is set to 110'b for PCIe legacy mode.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		X						

2.13 PCIe® Wake Status and PME Wake Status

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	AcpiPmEvtBlk: x00[15:14] = 0	Clear PciExpWakeStatus and WakeStatus bits before entering sleep state. When PCIe wake is enabled, care must be taken to ensure both of the status bits are cleared before entering into sleep states. Not clearing these status bits could result in the system either waking up immediately or failing to wake up from sleep states.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM_REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
	X	X						

3 LPC Controller (bus-0, dev-20, fun-3)

3.1 SPI Controller MMIO Base Address

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	LPC_PCI_config 0xA0 [31:5]	Memory base address for SPI ROM control registers. SBIOS needs to program non-zero address value to enable the MMIO access.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
						X		
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

3.2 Enabling SPI ROM Prefetch

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	LPC_PCI_config 0xBB [0] = 1	Enable SPI ROM (64bytes) prefetch

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
						X		
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

3.3 Enabling LPC DMA Function

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	LPC_PCI_config 0x40 [2] = 1 LPC_PCI_config 0x78[0] = 0	Enable DMA transaction on the LPC bus.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
						X		
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

3.4 Spi Timing Enhancement

ASIC Rev	Register Settings	Function/Comment
Hudson-1 A12 and above	LPC cfg 0xBB[5:3] = 111	Set to 111 to improve Spi timing margin.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
						X		
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

3.5 Spi Prefetch Enhancement

ASIC Rev	Register Settings	Function/Comment
Hudson-1 A12 and above	LPC cfg 0xBA[6:5] = 11 SpiMmio 0x00[19] = 1 SpiMmio 0x0C[21:16] = 1	These settings are for increasing SpiCs margin when prefetch is enabled. LPC cfg 0xBA[6:5] should be programmed to 11 by IMC only.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
						X		
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

4 UMI Settings - Indirect I/O Access

4.1 Defining AB_REG_BAR

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_reg xE0 [31:0] = ABRegBar	Defines the AB I/O base address. Refer to *AMD A45/A50/A55M Register Reference Guide, chapter 4: UMI/A-Link Bridge Registers* for more information.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		X						

4.2 Upstream DMA Access

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	AXCFG_reg: 0x04 [2] = 1	Enable Hudson-1 to issue memory read/write requests in the upstream direction.

Programming Sequence:

```
OUT AB_INDX, 0x80000004    // Load AB_INDX with pointer to AXCFG_reg:0x04
IN  AB_DATA, TMP           // Read COMMAND register (AXCFG_reg:0x04)
OR  TMP,     0x00000004    // Set bit 4
OUT AB_DATA, TMP           // Set BUS_MASTER_EN
```

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.3 PCIB Prefetch Settings

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PCIB prefetch ABCFG_reg 0x10060 [20] = 1 ABCFG_reg 0x10064 [20] = 1	The settings on AB control the PCIB prefetch. For all revisions the prefetch needs to be enabled for performance enhancement.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.4 OHCI Prefetch Settings

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0x80 [0] = 1	This register in AB controls the USB OHCI controller prefetch used for enhancing performance of ISO out devices.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.5 B-Link Client's Credit Variable Settings for the Downstream Arbitration Equation

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0x9C [0] = 1	Disable the credit variable in the downstream arbitration equation.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.6 Setting B-Link Prefetch Mode

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0x80 [18:17] = 0x3	Set B-Link prefetch mode.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.7 Detection of Upstream Interrupts

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0x94 [20] = 1 ABCFG_reg 0x94 [19:0] = CPU interrupt delivery address [39:20].	Enable UMI logic to detect upstream interrupts for the purposes of system management.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.8 Downstream Posted Transactions to Pass Non-Posted Transactions

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0x10090 [8] = 1	Enable downstream posted transactions to pass non-posted transactions.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.9 AB Int_Arbiter Enhancement

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0x10054 [11:0] = 0x7FF	Enable the A-Link int_arbiter enhancement to allow the A-Link bandwidth to be used more efficiently.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.10 Requester ID

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0x98 [16] = 1 ABCFG_reg 0x98 [17] = 1	Enable the requester ID for upstream traffic. [16]: for UMI link [17]: for GPP

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.11 A-Link L1 (ASPM)

ASIC Rev	Step	Register Settings	Function/Comment
Hudson-1 All Rev.	1	AXINDP_Reg 0xA0 [15:12] = 0x6	Setting LC_L1_Inactivity timer to 0x6 corresponds to 40us of idle time before link enters L1.
	2	AXCFG_Reg 0x68 [1:0] = 0x2	Enable L1 entry.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.12 A-Link L0s/L1 NAK Reduction

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	AXINDP_Reg 0xA0[7:4] = 0x3	Enter L1 sooner after ACK'ing PM request. This is done to reduce the number of NAK received with L1 enabled.
	AXINDP_Reg 0xB1[19] = 0x1	Turn off receiver when UMI Root Complex transmitter is in L0s.
	AXINDP_Reg 0xB1[28] = 0x1	Enables deassertion of PG2RX_CR_EN to lock clock recovery parameter when lane is in electrical idle. 0 = CR_EN is always asserted 1 = CR_EN is de-asserted when RX_EN is de-asserted during L0s/L1 and inactive lanes

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide sb800_rrg_nda_xxx
RTC	ACPI	PM REG	UMI/PCIe Bridges	I/O REG	XIOAPIC			
			X					

4.13 PLL Power Down in A-Link L1

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	AXINDC_Reg 0x40 [0] = 1 AXINDC_Reg 0x40 [3] = 1 AXINDC_Reg 0x40 [4] = 0 AXINDC_Reg 0x40 [9] = 0 AXINDC_Reg 0x40 [12] = 1	Enable unused lane power down feature Enable PLL OFF during L1 state Enable PLL Buffer power down during L1 state Enable PLL to power down during L1 state Enable PHY RX Front end circuit to shut off during L1 when PLL power down is enabled
	AXINDC_Reg 0x02 [8] = 1	Enable fix for race problem between PLL calibrator and LC wake up from L1.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.14 AB Internal Clock Gating

ASIC Rev	Step	Register Settings	Function/Comment
Hudson-1 All Rev.	1	ABCFG_reg 0x10054 [23:16] = 0x04 ABCFG_reg 0x98 [15:12] = 0x4	Program # of cycles to delay before gating internal clocks after idle condition.
	2	ABCFG_reg 0x54 [24] = 0x0 ABCFG_reg 0x10054 [24] = 0x1 ABCFG_reg 0x98 [11:8] = 0x7	Enable AB internal clock gating.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.15 Non-Posted Memory Write Support

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	AXINDC_Reg 0x10 [9] = 1	Enable Non-Posted Memory Write Support.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.16 SMI Ordering

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG 0x90[21] = 1	SMI ordering enhancement enable

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.17 Posted Pass Non-Posted Feature

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	**Downstream Traffic:** Step 1: ABCFG 0x10060[31] = 1 Step 2: ABCFG 0x1009C[4] = 1 ABCFG 0x1009C[5] = 1 Step 3: ABCFG 0x9C[2] = 1 ABCFG 0x9C[3] = 1 ABCFG 0x9C[4] = 1 ABCFG 0x9C[5] = 1 ABCFG 0x9C[6] = 1 ABCFG 0x9C[7] = 1 Step 4: ABCFG 0x90[21] = 1 ABCFG 0x90[22] = 1 ABCFG 0x90[23] = 1 Step 5: ABCFG 0xF0[6] = 1 ABCFG 0xF0[5] = 1 Step 6: AXINDC_Reg 0x2[9] = 1 Step 7: ABCFG 0x10090[9] = 1 ABCFG 0x10090[10] = 1 ABCFG 0x10090[11] = 1 ABCFG 0x10090[12] = 1 **Upstream traffic:** Step 7: ABCFG 0x58[10] = 1 Step 8: ABCFG 0xF0[3] = 1 ABCFG 0xF0[4] = 1 Step 9: ABCFG 0x54[1] = 1 Step 10: Only when GPP is enabled. RCINDC_Reg 0x2[9] = 1	Posted pass non-posted downstream direction feature enable. 0x54[1] is to enhance Upstream DMA read arbitration

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

4.18 UMI Gen2 Speed Change

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	Step 1: AXINDP_Reg 0xA4[0] = 0x1 Step 2: AXCFG_Reg 0x88[3:0] = 0x2 Step3: AXINDP_Reg 0xA4[18] = 0x1	To enable UMI link to Gen 2; 5 GT/s

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5 PCIe® General Purpose Ports

5.1 GPP Lane Configuration

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0xC0 [3:0] = 0x0 Or ABCFG_reg 0xC0 [3:0] = 0x2 Or ABCFG_reg 0xC0 [3:0] = 0x3 Or ABCFG_reg 0xC0 [3:0] = 0x4	The following four configurations are supported: 0000: PortA lanes[3:0] 0001: N/A 0010: PortA lanes[1:0], PortB lanes[3:2] 0011: PortA lanes[1:0], PortB lane2, PortC lane3 0100: PortA lane0, PortB lane1, PortC lane2, PortD lane3. Other combinations are not supported. The configuration setting is board design specific.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.2 GPP Port A/B/C/D Enable

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0xC0 [4] = 1	1: Enable Port A 0: Disable Port A Set this bit to 1 or 0 based on lane configuration
	ABCFG_reg 0xC0 [5] = 1	1: Enable Port B 0: Disable Port B Set this bit to 1 or 0 based on lane configuration
	ABCFG_reg 0xC0 [6] = 1	1: Enable Port C 0: Disable Port C Set this bit to 1 or 0 based on lane configuration
	ABCFG_reg 0xC0 [7] = 1	1: Enable Port D 0: Disable Port D Set this bit to 1 or 0 based on lane configuration

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.3 GPP Reset

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0xC0 [8] = 0	GPP lanes are in reset mode until software writes 0 to this register bit. The register should be programmed after software has enabled the GPP. Set this bit to 0 to release reset so all the GPP lane configurations can take effect.
	PM_REG 0xC0 [22] = 1 PM_REG 0xC4 [4] ** Note 1 **	These two registers should be used to de-assert the PCIe® reset to the device on GPP. Note 1** Software should toggle PM_REG 0xC4 [4] just before the link is activated. The spec requires reset should be de-asserted 20 ms before link activity. Please refer to PCI Express Specification Rev 2.1 for more details.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.4 PCIe® Ports De-emphasis Settings

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs		Polling RCINDP_Reg 0xA5[7:0]; If read back 0x10, no change for corresponding port's register If read back 0x29 or 0x2A, do the following register setting for corresponding port and toggle external PCIE_RST through GPIO50
	ABCFG_reg 0x340 [21] = 0	0: -6dB de-emphasis for port A 1: -3.5dB de-emphasis for port A
	ABCFG_reg 0x344 [21] = 0	0: -6dB de-emphasis for port B 1: -3.5dB de-emphasis for port B
	ABCFG_reg 0x348 [21] = 0	0: -6dB de-emphasis for port C 1: -3.5dB de-emphasis for port C
	ABCFG_reg 0x34C [21] = 0	0: -6dB de-emphasis for port D 1: -3.5dB de-emphasis for port D

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.5 Write Capability for PCIe® Read-Only Registers

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	RCINDC_Reg 0x10 [0] = 1 ABCFG_reg 0x330 [10] = 0	SBIOS needs to set this bit to disable the writable function of the PCIe read-only registers.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.6 Serial Number Capability

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0x330 [26] = 0	Disable serial number capability

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.7 Multi-function Enable

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG 0x90[20] = 1	Enable GPP bridge multi-function.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.8 GPP Upstream Memory Write Arbitration Enhancement

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG 0x54[26] = 1	Arbitration enhancement for GPP specific traffic

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.9 GPP Memory Write Max Payload Improvement

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	RCINDC_Reg 0x10[12:10] = 0x4	Set Memory Write transfer to chip with 64 Byte max payload

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.10 Multiple GPP Device Support

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG 0xF0[2] = 1	Multiple GPP device traffic support when there are UR happens.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.11 Separate Control for Release from Reset and Hold Training for each GPP Port

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG 0xC0[12] = 0 ABCFG 0xC0[13] = 0 ABCFG 0xC0[14] = 0 ABCFG 0xC0[15] = 0	Port A will be released from reset and hold training Port B will be released from reset and hold training Port C will be released from reset and hold training Port D will be released from reset and hold training BIOS determines when to release when doing training sequences. If the port is not used, BIOS needs to set the hold_training to 0x1 for the corresponding port (see Section 5.19 GPP Power Saving).

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.12 GPP PCIe® Native Interrupt Support

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PCIe Cfg 0x3D[7:0] = 0x01	Enable to support GPP PCIe native interrupt support. GPP bridge pci cfg space 0x3D Need to program these bits before RCINDC_Reg 0x10 [0] = 1 is programmed.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.13 Hot Plug: PCIe Native Support

ASIC Rev	Step	Register Settings	Function/Comment
Hudson-1 All Revs	1	RCINDP_Reg 0x10[3] = 0x1	Enable native PME.
	2	PCIe_Cfg 0x5A[8] = 0x1	For slot which supports hot plug, “Slot Implemented” bit needs to be set to 1. This bit is HwInit.
	3	PCIe_Cfg 0x6C[6] = 0x1.	Report Hot-Plug Capable. This bit is HwInit.
	4	RCINDP_Reg 0x20[19] = 0x0	Enable flushing TLPs when Data Link is down.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.14 Link Bandwidth Notification Capability Enable

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	RCINDC 0xC1[0] = 1	Enable GPP Link Bandwidth Notification Capability.
	PCIe Cfg 0x68[10] = 0	Link Bandwidth Management Interrupt Enable default value needs to be set to 0b for all GPP Root Ports’ pci cfg space.
	PCIe Cfg 0x68[11] = 0	Link Autonomous Bandwidth Interrupt Enable default value needs to be set to 0b for all GPP Root Ports’ pci cfg space.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.15 GPP Endpoint L1/L0s (ASPM)

ASIC Rev	Step	Register Settings	Function/Comment
Hudson-1 All Revs	1	L0s enable: PCIe_Cfg 0x68[1:0] = 0x1 L1 enable: PCIe_Cfg 0x68[1:0] = 0x2 L1/L0s enable: PCIe_Cfg 0x68[1:0] = 0x3	PCIe_Cfg 0x68 is in standard PCI configuration space. BIOS will need to program all the GPP ports based on the GPP port configuration.
	2	In the EP device, follow the capability list to find the PCIe® capability (capability ID = 0x10). LINK_CNTL[1:0] pcieConfigDev*: 0x68 PM_CONTROL Set bit [1:0] to 0x1 for L0s. Set bit [1:0] to 0x2 for L1 Set bit [1:0] to 0x3 for L0s/L1	Enable Endpoint device to support L0s/L1.
If GPP is enabled, the settings must be programmed for all GPP ports.			
Hudson-1 All Revs	1	RCINDP_Reg 0xA0[11:8] = 0x9	Set GPP L0s inactivity timer to 10us.
	2	RCINDP_Reg 0xA0[15:12] = 0x6	Set GPP L1 inactivity timer to 40us.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.16 GPP L1 Entry Delay Shortening

ASIC Rev	Step	Register Settings	Function/Comment
Hudson-1 All Revs	1	RCINDP_Reg 0xA0[7:4] = 0x1	Enter L1 sooner after ACK'ing PM request. This is done to reduce number of NAK received with L1 enabled.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.17 PLL Power Down in GPP L1

ASIC Rev	Register Settings	Function/Comment
If any GPP lanes are not used, they should be programmed to enable the Power Saving feature to minimize power consumption.		
Hudson-1 All Revs	RCINDC_Reg 0x40 [0] = 1	Enable unused GPP lane power down feature
	RCINDC_Reg 0x40 [3] = 1	Enable PLL OFF during in L1 state
	RCINDC_Reg 0x40 [4] = 0	Enable PLL Buffer power down during L1 state
	RCINDC_Reg 0x40 [9] = 0	Enable PLL to power down during L1 state
	RCINDC_Reg 0x40 [12] = 1	Enable PHY RX Front end circuit to shut off during L1 when PLL power down is enabled *Note: before accessing RCINDC_Reg, SBIOS needs to release GPP Reset first, refer to section 5.3
	RCINDC_Reg 0x02 [8] = 1	Enable fix for the race problem between PLL callibrator and LC wake up from L1.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.18 GPP Immediate Ack PM_Active_State_Request_L1

ASIC Rev	Register Settings	Function/Comment
If any GPP lanes are used, they should be programmed to enable the IMMEDIATE_ACK feature to workaround any device that doesn't follow the ordering rule. Please also enable the BIOS option (L1_IMMEDIATE_ACK) for all the ports. Default BIOS is to enable this L1_IMMEDIATE_ACK feature.		
Hudson-1 All Revs	For Port A, B, C and D : RCINDP_Reg 0xA0 [23] = 1	Always ACK an ASPM L1 entry DLLP (i.e., never generate PM_NAK)

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.19 GPP Power Saving

ASIC Rev	Step	Register Settings	Function/Comment
Hudson-1 All Revs	1	ABCFG 0xC0[8] = 0	Release GPP reset
	2	If no device is present or if link training fails, set the following: ABCFG 0xC0[12] = 1 (for Port A) ABCFG 0xC0[13] = 1 (for Port B) ABCFG 0xC0[14] = 1 (for Port C) ABCFG 0xC0[15] = 1 (for Port D)	Set hold_training for unused GPP ports. If any of the ports is not used, the programming of this register will keep the port in reset and prevent it from initiating the training as a power saving feature. Note this is also a requirement stated in section 5.11 "Separate Control for Release from Reset and Hold Training for each GPP Port".
	3	Enable "GPP Endpoint L1/L0s (ASPM)" for all Endpoint devices attached to GPP.	Refer to section: GPP Endpoint L1/L0s (ASPM)
	4	Enable "PLL Power Down in A-Link L1"	Refer to section: PLL Power Down in A-Link L1
	5	Enable "PLL Power Down in GPP L1"	Refer to section: PLL Power Down in GPP L1
	6	ABCFG 0x90[19] = 1 ABCFG 0x90[6] = 1	Enable PHY PLL Power Down for both NB/SB and GPP
	7	Use attached table to disable RX/TX pads. Set corresponding bits to 1 to disable pads.	Disable TX and RX pads' power for unused GPP ports.
	8	If no devices are present or link training fails in all 4 GPP ports: RCINDC_Reg 0x65[27:16] = 0xCFF	Force B_PPLL_PDNB to disable PLL. Force B_PPLL_BUF_PDNB to disable 10x driver in PLL. Force B_PIMP_TX_PDNB to disable TX impedance calibration pad. Force B_PIMP_TX_PDNB to disable RX impedance calibration pad.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.19.1 GPP Power Saving with Hot Plug/Unplug

ASIC Rev	Step	Register Settings	Function/Comment
Hudson-1 All Revs	1	ABCFG 0xC0[8] = 0x0	Release GPP reset
	2	Enable GPP port with hot-plugged device. Port A enable: ABCFG 0xC0[12] = 0x0 Port B enable: ABCFG 0xC0[13] = 0x0 Port C enable: ABCFG 0xC0[14] = 0x0	Release hold_training for port with hot-plugged device.

		Port D enable: ABCFG 0xC0[15] = 0x0	
	3	RCIND_Reg 0x65[27:16] = 0x000	Re-enable PLL and TX/RX impedance calibration pads.
	4	Use attached table to enable RX/TX pads. Set corresponding bits to 0 to enable pads.	Enable TX and RX pads' power for hot plugged GPP ports.
	5	Delay 200 us.	
The following needs to be programmed for the GPP port after the associated device is hot unplugged.			
Hudson-1 All Revs	1	RCINDP_Reg 0xA2[17] = 0x1	Enable reconfiguration from L1.
	2	RCINDP_Reg 0xA2[8] = 0x1	Initiate link reconfiguration.
	3	Disable GPP port with device hot-unplugged: Port A disable: ABCFG 0xC0[12] = 0x1 Port B disable: ABCFG 0xC0[13] = 0x1 Port C disable: ABCFG 0xC0[14] = 0x1 Port D disable: ABCFG 0xC0[15] = 0x1	Assert hold_training for port with device hot-unplugged.
	4	RCINDP_Reg 0xA2[17] = 0x0	Disable reconfiguration from L1.
	5	Use attached table to disable RX/TX pads. Set corresponding bits to 1 to disable pads.	Disable TX and RX pads' power for hot-unplugged GPP ports.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

5.19.2 GPP Power Saving – RX/TX Pads Power Up/Down Mapping Table

GPP Port	GPP Lane Configuration	RCINDC_Reg 0x65[15:0] bits Lane Reversal – RCINDP_Reg 0x50[0] 0 : normal	 1 : reversed
A	1 : 1 : 1 : 1 2 : 1 : 1 2 : 2 4 : 0	0, 8 0-1, 8-9 0-1, 8-9 0-3, 8-11	3, 11 2-3, 10-11 2-3, 10-11 0-3, 8-11
B	1 : 1 : 1 : 1 2 : 1 : 1 2 : 2 4 : 0	1, 9 2, 10 2-3, 10-11 n/a	2, 10 1, 9 0-1, 8-9 n/a
C	1 : 1 : 1 : 1 2 : 1 : 1 2 : 2 4 : 0	2, 10 3, 11 n/a n/a	1, 9 0, 8 n/a n/a
D	1 : 1 : 1 : 1 2 : 1 : 1 2 : 2 4 : 0	3, 11 n/a n/a n/a	0, 8 n/a n/a n/a

5.20 GPP Gen2 Speed Change

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	If (Allow Gen2) AND (Gen2 is enabled) AND (GPP port is enabled) Step 1: PCIe_Cfg 0x88[3:0] = 0x2 Step 2: RCINDP_Reg 0xA4[0] = 0x1 Step 3: RCINDP_Reg 0xA2[13] = 0x0 Step 4: RCINDP_Reg 0xC0[15] = 0x0 Step 5: RCINDP_Reg 0xA4[29] = 0x1 If (GPP Compliance Pattern Mode disabled) Step 6: Poll for RCINDP_Reg 0xA5[5:0] == 0x10, every 400 us for maximum of 501 times. If timed out, proceed with Step 7, else exit. Step 7: PCIe_Cfg 0x88[3:0] = 0x1 Step 8: RCINDP_Reg 0xA4[0] = 0x0 Step 9: RCINDP_Reg 0xA2[13] = 0x1	If Gen2 is allowed via efuse setting, Gen2's CMOS setting is enabled and GPP port is enabled, then proceed to program link to support Gen2. Set Target Link Speed in Link Control 2 register to 5.0 GT/s. Enable PCIe® Gen2. Disable PCIe 2.0 defined link width change feature. Disable RC auto speed negotiation. Allow upstream component to automatically initiate multiple speed changes. If GPP is NOT in compliance pattern testing mode, proceed with auto speed downgrade if device cannot enter Gen2. If Gen2 is enabled and link fails to enter L0, then program link to Gen1 speed. Set PCIe config space target link speed to Gen1. Disable Gen2. Disable link up configuration. RCINDP_Reg needs to be programmed for each enabled GPP port. PCIe_Cfg 0x88 is standard PCI configuration space. BIOS will need to program all the GPP ports based on the GPP port configuration.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

6 PCIB (PCI-bridge, bus-0, dev-20, fun-04)

6.1 PCI-bridge Subtractive Decode

ASIC REV	Register Settings	Function/Comment
Hudson-1 All Revs	PCIB_PCI_config 0x40 [5] = 1 PCIB_PCI_config 0x4B [7] = 1	Enable the PCI-bridge subtractive decode. This setting is strongly recommended since it supports some legacy PCI add-on cards.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
							X	
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

6.2 PCI-bridge Upstream Dual Address Window

ASIC REV	Register Settings	Function/Comment
Hudson-1 All Revs	PCIB_PCI_config 0x50 [0] = 1	PCI-bridge upstream dual address window. This setting is applicable if the system memory is more than 4GB, and the PCI devices can support dual address access.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
							X	
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

6.3 One-Channel Mode

ASIC REV	Register Settings	Function/Comment
Hudson-1 All Revs	PCIB_PCI_config 0x64 [20] = 1	Enable One-Channel Mode for upstream read. Note: This setting is mandatory.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
							X	
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

6.4 CLKRUN#

ASIC REV	Register Settings	Function/Comment
Hudson-1 All Revs	PCIB_PCI_config 0x64 [15] = 1	This bit should be set to 1 for the proper operation of CLKRUN#.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
							X	
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

6.5 PCI Bus GNT3#

ASIC REV	Register Settings	Function/Comment
PCI GNT3# function is not enabled by default. If PCI GNT3# is used at system level, the following programming is required.		
Hudson-1 All Revs	PCIB_PCI_config 0x64 [25] = 1	Enable PCI bus GNT3#. GNT3# pin is multi-function IO. Enabling this pin is board design specific.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
							X	
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7 USB – OHCI & EHCI Controllers (bus-0, dev-18/19/22, fun-00 & 02 / bus-0, dev-20, fun-05)

Please note the following information for this section:

- EHCI BAR address = EHCI_PCI_config 0x10 [31:8]
- EHCI_EOR is the EHCI operation register = EHCI_BAR + 0x20
- The device list for all USB controllers is as follows:

Device List	Function/Comment
Bus-0, dev-18, fun-0	USB1, OHCI
Bus-0, dev-18, fun-2	USB1, EHCI
Bus-0, dev-19, fun-0	USB2, OHCI
Bus-0, dev-19, fun-2	USB2, EHCI
Bus-0, dev-22, fun-0	USB3, OHCI
Bus-0, dev-22, fun-2	USB3, EHCI
Bus-0, dev-20, fun-5	USB4, OHCI

7.1 OHCI and EHCI Controllers

ASIC Rev	Register Settings	Function/Comment
OHCI / EHCI controllers are enabled by default. If all the USB ports on any of these controllers are not used, then the controller can be disabled to minimize power consumption. Writing 0 to the responsible register will disable the controller. Controller shall be disabled in pairs. If the EHCI controller needs to be disabled then the corresponding OHCI controller shall also be disabled. USB4 OHCI standalone controller is the exception as it does not have the corresponding EHCI controller; therefore disabling only the OHCI controller is allowed.		
Hudson-1 All Revs	USB OHCI/EHCI controller pair 1 enable	
	PM_IO 0xEF [0] = 1 (default)	Enable the USB1 (bus-0, dev-18) OHCI controller.
	PM_IO 0xEF [1] = 1 (default)	Enable the USB1 (bus-0, dev-18) EHCI controller.
	USB OHCI/EHCI controller pair 2 enable	
	PM_IO 0xEF [2] = 1 (default)	Enable the USB2 (bus-0, dev-19) OHCI controller.
	PM_IO 0xEF [3] = 1 (default)	Enable the USB2 (bus-0, dev-19) EHCI controller.
	USB OHCI/EHCI controller pair 3 enable	
	PM_IO 0xEF [4] = 1 (default)	Enable the USB3 (bus-0, dev-22) OHCI controller.
	PM_IO 0xEF [5] = 1 (default)	Enable the USB3 (bus-0, dev-22) EHCI controller.
	USB OHCI standalone controller enable	
	PM_IO 0xEF [6] = 1 (default)	Enable the USB4 (bus-0, dev-20, fun-5) OHCI controller.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		X						

7.2 USB S4/S5 Wake-up or PHY Power-down Support

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	Option-1: PM_IO 0xF0 [0] = 1 Option-2: PM_IO 0xF0 [0] = 0	Option-1: ***USB Wake from S5 not supported on the platform*** When the USB power rails USB PHY PLL, USB PHY core power and USB PHY DLL are connected to S0-S3 power, set the bit to 0 to disable the USB S4/S5 wakeup function Option-2: ***USB Wake from S5 supported on the platform*** When the USB power rails USB PHY PLL, USB PHY core power and USB PHY DLL are connected to S5 power, set the bit to 1 to enable the USB S4/S5 wakeup function

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		X						

7.3 USB PHY Auto-Calibration Setting

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	EHCI_BAR 0xC0 = 0x00020F00	Enable the USB PHY auto calibration resistor to match 45 ohm resistance.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.4 USB Reset Sequence

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_IO 0xF0 [2] = 1 (default)	Enable the USB controller to get reset by any software that generates a PCIRst# condition. However, this bit should be cleared before a software generated reset condition occurs during S3 resume, so that the USB controller will not lose the connection status during the S3 resume procedure. The software generated PCIRst# conditions include Keyboard Reset, or write to the IO-CF9 register.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		X						

7.5 USB Advanced Sleep Control

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_IO 0xF0 [10:8] = 0x3 (default)	Enable the USB EHCI controller advance sleep mode function to improve power saving.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		X						

7.6 USB Delay UMI L1 State

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	ABCFG_reg 0x90 [17] = 1 EHCI_PCI_Config 0x54 [0] = 1	Enable the feature in AB module to block UMI Link from entering L1 state when USB controllers indicate active bus condition. Set this bit to enable EHCI indication on bus activity. With ABCFG_reg x90 [17] set but EHCI bit not set, only OHCI activities will cause the L1 state blocking.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
			X					

7.7 USB 2.0 Ports Driving Strength

ASIC Rev	Register Settings	Function/Comment
Hudson-1 Rev A13	Step 1: EHCI_BAR 0xC4 = 0x01 EHCI_BAR 0XC0[15:8] = 0X0F	Required value for any supported driving strength. Adjust IREFADJ value Adjust NewCalbus value
Hudson-1 Rev A12	Step 1: EHCI_BAR 0xC4 = 0x00 EHCI_BAR 0XC0 [15:8]= 0X15	Required value for any supported driving strength. Adjust IREFADJ value Adjust NewCalbus value
Hudson-1 All Revs	Step 2: EHCI_BAR 0xB4 [2:0] = “HSADJ” EHCI_BAR 0xB4 [12] = 0 (“VLoad”) EHCI_BAR 0xB4 [16:13] = “port#” Step 3: EHCI_BAR 0xB4[12] = 1	Adjusts the USB2.0 ports driving strength. HSADJ to set the driving strength value. VLoadB to load the value to the PHY for the selected port. port# is the selected port. SBIOS can repeat step 2 for those ports with less margin on HS eye diagram. Set to ‘1’ to lock PHY UTMI Control interface.

Note:

The IREFADJ and NewCalBus values should be programmed for any HSADJ value used in the supported table below. Not setting these values correctly can cause the system to encounter false failures due to USB HS devices downgrade to Full Speed device.

Adjust the driving strength to compensate for designs that have longer traces.

1. Different board designs may require different settings for different ports depending on trace length and routing.

2. Only apply the setting to the ports that have longer USB trace lengths (> 12 inches) to the connector, and if the eye diagram margin is not enough. There is no need to apply these setting to the ports with shorter trace lengths or close to the USB connectors.

3. EHCI_BAR 0xB4 = EHCI_EOR 0x94 (UTMI Control Register)

4. EHCI_BAR 0xB4[2:0] (HSADJ)
   "000" = Reserved , "001" = +5%, "010" = +10%, "100" = +10%,
   "011" = +15%, "101" = +15%, "110" = Reserved, "111" = Reserved
   EHCI_BAR 0xB4[16:13] (port#)
   "0000" = port0, "0001" = port1, …… "0101" = port5, 0110 ~ 1110 = Reserved.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.8 EHCI In and Out Data Packet FIFO Threshold

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	EHCI_BAR 0xA4 = 0x00400040	IN/OUT data packet FIFO threshold for EHCI controllers. **FIFO threshold setting must be programmed in all the three EHCI host controllers:** **bus-0, dev-18 / dev-19 / dev-22, fun-2**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.9 OHCI MSI Function

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	OHCI_PCI_Config 0x40[8] = 1 (default)	Disable OHCI MSI function. For normal operation, the MSI function must be disabled by setting bit [8] in all four OHCI controllers: **bus-0, dev-18, fun-0 / bus-0, dev-19, fun-0 /** **bus-0, dev-22, fun-0 / bus-0, dev-20, fun-5.**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.10 EHCI MSI Function

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	EHCI_PCI_Config 0x50 [6] = 1	Disables EHCI MSI function. For normal operation, the MSI function must be disabled by setting bit [6] in all three EHCI controllers, **bus-0, dev-18, fun 2 / bus-0, dev-19, fun-2 / bus-0, dev-22, fun-2.**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.11 USB SMI Handshake

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	OHCI_PCI_Config 0x50 [12] = 0	Enable SMI handshake between USB and ACPI. The setting must be programmed in all four OHCI controllers: **bus-0, dev-18, fun-0 / bus-0, dev-19, fun-0 / bus-0, dev-22, fun-0 / bus-0, dev-20, fun-5.**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.12 EHCI Async Park Control

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	EHCI_PCI_Config 0x50[23] = 1 EHCI_PCI_Config 0x50 [11:8] = 0x1 (default) EHCI_PCI_Config 0x50 [15:12] = 0x2 (default)	Disable async park mode. Async park mode must be disabled in A11/A12 due to a logic bug. Below settings will be disabled automatically. Enable advanced async park mode for IN transfers when async park mode is enabled by the host driver. Enable advanced async park mode for OUT transfers when async park mode is enabled by the host driver. The settings must be programmed in all three EHCI controllers: **bus-0, dev-18, fun-2 / bus-0, dev-19, fun-2 / bus-0, dev-22, fun-2.**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.13 EHCI Async Stop Enhancement

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	EHCI_PCI_Config 0x50 [29] = 1	Enable EHCI async stop enhancement. Some software does not clear run/stop before clearing async-enable, and EHCI may take a long period of time to respond to the command. By enabling the enhancement, EHCI can respond to the command right after the completion of the current descriptor process. The setting must be programmed in all three EHCI controllers: **bus-0, dev-18, fun-2 / bus-0, dev-19, fun-2 / bus-0, dev-22, fun-2.**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.14 OHCI ISOCHRONOUS OUT Prefetch Disable

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	OHCI_PCI_Config 0x50 [9:8] = 00	Disable OHCI ISO OUT prefetch feature. Whenever there is a latency of more than 1ms for the upstream transaction, we might end up hitting a corner case bug in the OHCI arbiter block which would result in the aribiter not giving grant to the requested client .This causes blue screens under Windows® and could manifest as hangs under Linux. One of the traffic that is required to hit the bug is related to the prefetch logic. By disabling prefetch we can prevent the system from hitting the bug. The setting must be programmed in all four OHCI controllers: **bus-0, dev-18, fun-0 / bus-0, dev-19, fun-0 / bus-0, dev-22, fun-0 and dev-20 fun-5**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.15 EHCI PING Response Fix Enable

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	EHCI_PCI_Config 0x54 [1] = 1	Enable PING Response fix Whenever packet responses like ACK, NAK are corrupted inside the PHY (due to bad SI), the MAC layer is supposed to compare the lower and upper nibble and discard it. But the logic in A11 was only looking at lower nibble to decide the type of response. The fix checks both upper nibble and lower nibble of the response byte to decide upon the response type. The setting must be programmed in all three EHCI controllers: **bus-0, dev-18, fun-2 / bus-0, dev-19, fun-2 / bus-0, dev-22, fun-2**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

7.16 USB DLL Reset Sequence

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_IO 0xF3 [5] = 1 Delay 1 µS PM_IO 0xF3 [5] = 0	Reset DLL on power up. The software generated DLL reset sequence should be applied on power up (S5 → S0) and from any resume events (S3/S4).

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		X						

7.17 Frame Babble Detection

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	EHCI_BAR 0xBC [11] = 1	Disable Frame Babble detection. Erratum # 19 This setting must be programmed in all three EHCI controllers: **bus-0, dev-18, fun-2 / bus-0, dev-19, fun-2 / bus-0, dev-22, fun-2 .**

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in A45/A50/A55M Register Reference Guide
	X							
RTC	ACPI	PM REG	UMI/PCIe Bridges	I/O REG	XIOAPIC			

8 SATA: bus-0, dev-17, fun-0

8.1 SATA Configuration

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_IO 0xDA [0] = 1 (default)	Enable the SATA controller.
	SATA_PCI_config 0x40 [0] = 0	This bit needs to be cleared to convert the subclass code register to read-only. Refer to section *8.3* for the SATA subclass programming sequence.
	SATA_PCI_config 0x44 [0] = 1	Enable the SATA watchdog timer register prior to the SATA BIOS post. See Note.
	SATA_PCI config 0x40[23]=1	Disable AHCI prefetch feature. Otherwise, will have side effect.
Note: The system may hang during post if this register is not set correctly.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		X						

8.2 SATA Ports

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	SATA_PCI_config 0x40 [16] = 1	When set, SATA port 0 is disabled, and port 0 clock is shut down.
	SATA_PCI_config 0x40 [17] = 1	When set, SATA port 1 is disabled, and port 1 clock is shut down.
	SATA_PCI_config 0x40 [18] = 1	When set, SATA port 2 is disabled, and port 2 clock is shut down.
	SATA_PCI_config 0x40 [19] = 1	When set, SATA port 3 is disabled, and port 3 clock is shut down.
	SATA_PCI_config 0x40 [20] = 1	When set, SATA port 4 is disabled, and port 4 clock is shut down.
	SATA_PCI_config 0x40 [21] = 1	When set, SATA port 5 is disabled, and port 5 clock is shut down.
Note: Some board designs may choose to disable unused SATA ports to reduce power consumption.		

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.3 Staggered SATA PHY DLL Reset

The follow section is mandatory for proper initialization of SATA PHY DLL. This should be applied at the earliest possible BIOS routine **before** any SATA initialization sequence and **after every** reset to SATA controller due to, but not limited to, the following:

1. After power up and before the HT (Hypertransport™) link speed change.
2. After CF9 reset for HT link speed change programming has occurred.
3. After any other CF9 reset has occurred during normal boot sequence other than that described in step 2 below.

This programming sequence should be applied after any resume from sleep states such as S3/S4, in addition to cold boot or power up.

The purpose of this programming sequence is to stagger the SATA PHY DLL reset such that it does not draw too much current, as it would, if all DLLs were reset simultaneously.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	1. PCI_CFG 0x40[16] write 0x1: disable Port0 2. Wait 2us 3. PCI_CFG 0x40[16] write 0x0: enable Port0 4. Wait 2us 5. PCI_CFG 0x40[17] write 0x1: disable Port1 6. Wait 2us 7. PCI_CFG 0x40[17] write 0x0: enable Port1 8. Wait 2us 9. PCI_CFG 0x40[18] write 0x1: disable Port2 10. Wait 2us 11. PCI_CFG 0x40[18] write 0x0: enable Port2 12. Wait 2us 13. PCI_CFG 0x40[19] write 0x1: disable Port3 14. Wait 2us 15. PCI_CFG 0x40[19] write 0x0: enable Port3 16. Wait 2us 17. PCI_CFG 0x40[20] write 0x1: disable Port4 18. Wait 2us 19. PCI_CFG 0x40[20] write 0x0: enable Port4 20. Wait 2us 21. PCI_CFG 0x40[21] write 0x1: disable Port5 22. Wait 2us 23. PCI_CFG 0x40[21] write 0x0: enable Port5	Stagger the SATA PHY DLL reset for each port. The register definition used in this section can be referenced from Section 8.2 SATA Ports. Toggle the bit-wise per-port disable bit to reset the DLL. Wait time specified (2us) is the minimum wait time.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.4 SATA Subclass Programming Sequence

The SATA controller supports the following modes:

- IDE mode
- AHCI mode
- Raid mode

SBIOS programs the subclass code and the interface register to enable the SATA controller to be represented as the IDE controller, the AHCI controller, or the Raid controller.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	1. SATA_PCI_config 0x40 [0] = 1	Enable the subclass code register (PCI config register 0Ah) and the program interface register (PCI config register 09h) to be programmable.
	2. Program SATA Controller mode in a) IDE mode, or SATA_PCI_config 0x09 = 0x8F (default) SATA_PCI_config 0x0A = 0x01 b) AHCI mode, or SATA_PCI_config 0x09 = 0x01 SATA_PCI_config 0x0A = 0x06 c) RAID mode SATA_PCI_config 0x09 = 0x00 SATA_PCI_config 0x0A = 0x04	SBIOS is required to program the subclass code register of the SATA controller to be represented as the IDE, AHCI, or RAID controller.
	3. SATA_PCI_config 0x40 [0] = 0	Clears the bit to convert the subclass code register to be a read-only register. SBIOS is required to complete this step to ensure that the subclass code register be read-only (in order to be PCI compliant).

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.5 SATA PHY Programming Sequence

SBIOS needs to program the SATA controllers in the following sequence. Performing this procedure gives enough time for the SATA controllers to correctly complete SATA drive detection. SBIOS needs to do the same procedure after the system resumes back from the S3 state.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	SATA_PCI_config 0x84 [15:0] = 0x3006 SATA_PCI_config 0x94 [31:0] = 0x0056A607 SATA_PCI_config 0x84 [15:0] = 0x2006 SATA_PCI_config 0x94 [31:0] = 0x00061400 SATA_PCI_config 0x84 [15:0] = 0x1006 SATA_PCI_config 0x94 [31:0] = 0x00061302	Select port 0 Gen 3 Fine-tune PHY for Gen 3 Select port 0 Gen 2. Fine-tune PHY for Gen 2 Select port 0 Gen 1. Fine-tune PHY for Gen 1 This setting is for Croaker. Setting may vary through different board PCB trace length.

	SATA_PCI_config 0x84 [15:0] = 0x3206 SATA_PCI_config 0x94 [31:0] = 0x0056A607 SATA_PCI_config 0x84 [15:0] = 0x2206 SATA_PCI_config 0x94 [31:0] = 0x00061400 SATA_PCI_config 0x84 [15:0] = 0x1206 SATA_PCI_config 0x94 [31:0] = 0x00061302	Select port 1 Gen 3 Fine-tune PHY for Gen 3 Select port 1 Gen 2. Fine-tune PHY for Gen 2 Select port 1 Gen 1. Fine-tune PHY for Gen 1 This setting is for Croaker. Setting may vary through different board PCB trace length.
Hudson-1 All Revs	SATA_PCI_config 0x84 [15:0] = 0x3406 SATA_PCI_config 0x94 [31:0] = 0x0056A607 SATA_PCI_config 0x84 [15:0] = 0x2406 SATA_PCI_config 0x94 [31:0] = 0x00061402 SATA_PCI_config 0x84 [15:0] = 0x1406 SATA_PCI_config 0x94 [31:0] = 0x00064300	Select port 2 Gen 3 Fine-tune PHY for Gen 3 Select port 2 Gen 2. Fine-tune PHY for Gen 2 Select port 2 Gen 1. Fine-tune PHY for Gen 1 This setting is for Croaker. Tarpon may use default setting.
	SATA_PCI_config 0x84 [15:0] = 0x3606 SATA_PCI_config 0x94 [31:0] = 0x0056A607 SATA_PCI_config 0x84 [15:0] = 0x2606 SATA_PCI_config 0x94 [31:0] = 0x00061402 SATA_PCI_config 0x84 [15:0] = 0x1606 SATA_PCI_config 0x94 [31:0] = 0x00064300	Select port 3 Gen 3 Fine-tune PHY for Gen 3 Select port 3 Gen 2. Fine-tune PHY for Gen 2 Select port 3 Gen 1. Fine-tune PHY for Gen 1 This setting is for Croaker. Tarpon may use default setting.
	SATA_PCI_config 0x84 [15:0] = 0x3806 SATA_PCI_config 0x94 [31:0] = 0x0056A700 SATA_PCI_config 0x84 [15:0] = 0x2806 SATA_PCI_config 0x94 [31:0] = 0x00061502 SATA_PCI_config 0x84 [15:0] = 0x1806 SATA_PCI_config 0x94 [31:0] = 0x00064302	Select port 4 Gen 3 Fine-tune PHY for Gen 3 Select port 4 Gen 2. Fine-tune PHY for Gen 2 Select port 4 Gen 1. Fine-tune PHY for Gen 1 This setting is for Croaker. Tarpon may use default setting. Gen 3 eSATA is not supported. Croaker port 4 is eSATA port.
	SATA_PCI_config 0x84 [15:0] = 0x3A06 SATA_PCI_config 0x94 [31:0] = 0x0056A700 SATA_PCI_config 0x84 [15:0] = 0x2A06 SATA_PCI_config 0x94 [31:0] = 0x00061502 SATA_PCI_config 0x84 [15:0] = 0x1A06 SATA_PCI_config 0x94 [31:0] = 0x00064302	Select port 5 Gen 3 Fine-tune PHY for Gen 3 Select port 5 Gen 2. Fine-tune PHY for Gen 2 Select port 5 Gen 1. Fine-tune PHY for Gen 1 This setting is for Croaker. Tarpon may use default setting. Gen 3 eSATA is not supported. Croaker port 4 is eSATA port.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.6 SATA Identification Programming Sequence for IDE Mode

The following sequence should be included in the SBIOS drive identification loop for SATA drives detection.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	1. If any of the SATA port status register SATA_BAR5 + 0x128 [3:0] = 0x3 SATA_BAR5 + 0x1A8 [3:0] = 0x3 SATA_BAR5 + 0x228 [3:0] = 0x3 SATA_BAR5 + 0x2A8 [3:0] = 0x3 SATA_BAR5 + 0x328 [3:0] = 0x3 SATA_BAR5 + 0x3A8 [3:0] = 0x3 Then set SATA_BAR0 + 0x6 = 0xA0 or SATA_BAR0 + 0x6 = 0xB0 or SATA_BAR2 + 0x6 = 0xA0 or SATA_BAR2 + 0x6 = 0xB0 or PATA_BAR0/2 + 0x6 = 0xA0 or PATA_BAR0/2 + 0x6 = 0xB0 or Go to step (2). Else No drive is attached, exit the detection loop.	SATA_BAR5 + 0x128h : port 0 status register SATA_BAR5 + 0x1A8h : port 1 status register SATA_BAR5 + 0x228h : port 2 status register SATA_BAR5 + 0x2A8h : port 3 status register SATA_BAR5 + 0x328h : port 4 status register SATA_BAR5 + 0x3A8h : port 5 status register SATA host and device serial interface communication is done and ready if the SATA port status register = 0x3. for SATA controller primary master emulation for SATA controller primary slave emulation for SATA controller secondary master emulation for SATA controller secondary slave emulation for PATA controller primary/secondary master emulation for PATA controller primary/secondary slave emulation Otherwise, No SATA drive attached or SATA drive is not ready.
	2. If SATA_BAR0 + 0x6 = 0xA0 and SATA_BAR0 + 0x7 [7] & [3] = 0 Or SATA_BAR0 + 0x6 = 0xB0 and SATA_BAR0 + 0x7 [7] & [3] = 0 Or SATA_BAR2 + 0x6 = 0xA0 and SATA_BAR2 + 0x7 [7] & [3] = 0 Or SATA_BAR2 + 0x6 = 0xB0 and SATA_BAR2 + 0x7 [7] & [3] = 0 Or PATA_BAR0/2 + 0x6 = 0xA0 and PATA_BAR0/2 + 0x7 [7] & [3] = 0 Or PATA_BAR0/2 + 0x6 = 0xB0 and PATA_BAR0/2 + 0x7 [7] & [3] = 0 then the drive detection is completed Else loop until 30s time out, drive detection fail	SATA_BAR0 + 0x7 [7] & [3] = 0 means primary master device ready SATA_BAR0 + 0x7 [7] & [3] = 0 means primary slave device ready SATA_BAR2 + 0x7 [7] & [3] = 0 means secondary master device ready SATA_BAR2 + 0x7 [7] & [3] = 0 means secondary slave device ready PATA_BAR0/2 + 0x7 [7] & [3] = 0 means primary /secondary master device ready PATA_BAR0/2 + 0x7 [7] & [3] = 0 means primary /secondary slave device ready There is no SATA device attached on the port if time out occurs (see Note).

Note: Most drives do not need 10s timeout. The 10s timeout is only needed for some particularly large capacity SATA drives, which require a longer spin-up time during a cold boot.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.7 Restoring SATA Registers after S3 Resume State

The following registers need to be restored by SBIOS after S3 resume for the SATA controller.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	SATA_PCI_config 0x09 [7:0] SATA_PCI_config 0x0A [7:0]	Programmable interface and Subclass code. To program the subclass code register, SATA_PCI_config x40 [0] needs to be set. After the subclass is programmed, SATA_PCI_config 0x40 [0] needs to be reset.
	SATA_PCI_config 0x44 [0]	Enables the Watch-Dog timer for the all ports.
	SATA BAR5 + 0xF8 [17:0]	SATA ports indication registers.
	SATA_PCI_config 0x34 [7:0] SATA_PCI_config 0x61 [7:0]	SATA Capability registers.
	Staggered SATA PHY DLL Reset sequence	Refer to Section 8.3 for details on the programming sequence.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.8 External SATA Ports Indication Registers

The following registers need to be programmed for eSATA ports:

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	For the ports which are configured as eSATA: 1. PxCMD.ESP should be set. To set the register, write: Port 0: SATA BAR5 + 0xF8 [12] = 1 Port 1: SATA BAR5 + 0xF8 [13] = 1 Port 2: SATA BAR5 + 0xF8 [14] = 1 Port 3: SATA BAR5 + 0xF8 [15] = 1 Port 4: SATA BAR5 + 0xF8 [16] = 1 Port 5: SATA BAR5 + 0xF8 [17] = 1 2. PxCMD.HPCP should be cleared. To clear the register, write: Port 0: SATA BAR5 + 0xF8 [0]=0 Port 1: SATA BAR5 + 0xF8 [1]=0 Port 2: SATA BAR5 + 0xF8 [2]=0 Port 3: SATA BAR5 + 0xF8 [3]=0 Port4: SATA BAR5 + 0xF8 [4]=0 Port5: SATA BAR5 + 0xF8 [5]=0 3. If any of the ports was programmed as an external port, HCAP.SXS should also be set. To set the register, write SATA BAR5 + 0xFC[20] = 1	PxCMD.ESP (External SATA port) and PxCMD.HPCP (Hot Plug Capable port) registers should be programmed to indicate if the port is used for External SATA and if it requires Hot-Plug capability. To program these registers, SATA_PCI_config x40 [0] needs to be set. After the subclass is programmed, SATA_PCI_config 0x40 [0] needs to be reset. For example, if port 0 was configured as eSATA, other ports are internal SATA, SATA BAR5 + F8 [17:12] = 000001(b) SATA BAR5 + F8 [5:0] = 000000(b) PxCMD.ESP bit is mutually exclusive with PxCMD.HPCP bit in the same port. In general: If no E-SATA ports in system, then HCAP.SXS = 0, else HCAP.SXS = 1. ESP HPCP eSATA (signal only connector) 1 0 iSATA 0 0 PxCMD ESP located at: SATA BAR5 + port offset + 0x18 [21] PxCMD HPCP located at: SATA BAR5 + port offset + 0x18 [18]

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.9 Dynamic Power Saving

ASIC Rev	Register Settings	Function/Comment
Enable Dynamic power saving for additional power saving		
Hudson-1 All Revs	SATA_PCI config 0x40h [2] =1	When set, dynamic power saving function for SATA core clock will be performed during partial/slumber mode to reduce power consumption.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.10 Aggressive Link Power Management

ASIC Rev	Register Settings	Function/Comment
Disabling ALPM will prevent the OS driver from enabling HIPM and DIPM. This setting is required only if both DIPM and HIPM are not required to be supported at the platform level.		
Hudson-1 All Revs	SATA BAR5 + 0xFC [11] = 0	To disable ALPM. To program these registers, SATA_PCI_config x40 [0] needs to be set. After the subclass is programmed, SATA_PCI_config 0x40 [0] needs to be reset. Once this bit is cleared, SATA BAR5 + 0x00 [26] will be 0.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.11 Port Multiplier and FIS-based Switching Support

The following register settings disable support for Port Multiplier and FIS-based Switching.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	SATA BAR5 + 0xFC [12] = 0	Disable Port Multiplier support. To program these registers, SATA_PCI_config x40 [0] needs to be set. After the subclass is programmed, SATA_PCI_config 0x40 [0] needs to be reset. Once this bit is cleared, SATA BAR5 + 0x00 [17] will be 0.
	SATA BAR5 + 0xFC [10] = 0 SATA BAR5 + 0xF8 [27:22] = 0	Disable FIS-based Switching support. To program these registers, SATA_PCI_config x40 [0] needs to be set. After the subclass is programmed, SATA_PCI_config 0x40 [0] needs to be reset. Once these bits are cleared, SATA BAR5 + 0x00 [16] and SATA BAR5 + port offset + 0x18 [22] will be 0.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.12 CCC (Command Completion Coalescing) Support

The following register settings disable support for Command Completion Coalescing.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	SATA_BAR5 + 0xFC [19] = 0	To disable Command Completion Coalescing support. To program these registers, SATA_PCI_config x40 [0] needs to be set. After the subclass is programmed, SATA_PCI_config 0x40 [0] needs to be reset. Once this bit is cleared, SATA BAR5 + 0x00 [7] will be 0.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

Register 0xFC[19] controls the CCC capability setting in register BAR5, offset 0 bit 7. Setting it to 0 will make CCC not visible to software. CCC is enabled by default, on power up. BIOS should leave 0xFC[19] untouched for normal operation. The setting to disable should only be used if CCC needs to be disabled for specific platform configuration.

8.13 SATA MSI and D3 Power State Capability

8.13.1 SATA MSI Settings

SATA controller does not support message based Interrupts. The capability pointer offset needs to be re-programmed from its default setting to prevent the driver from enabling this feature.

8.13.2 D3 Power State Settings

SATA controller does not support D3 power state. The capability pointer offset needs to be re-programmed from its default setting to prevent the driver from enabling this feature.

8.13.3 Capability Pointer Settings

The following settings re-program the capability pointer to the recommended start of the capabilities table of supported features. (Hide MSI and D3 state capability from driver/OS.)

ASIC Rev	Register Settings	Function/Comment
SB80 All Revs	1. SATA_PCI_config 0x40 [0] = 1 2. SATA_PCI_config 0x34 [7:0] = 0x70 3. SATA_PCI_config 0x40 [0] = 0	To program the starting offset of capability header without MSI and D3 support.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the register reference guide RRG-xxxSB800-xx
x								
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			

8.14 SATA PCI Watchdog Timer

The programming sequence detailed below enables and sets the Watchdog timer.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	1. SATA_PCI_config 0x44 [0] = 1 2. SATA_PCI_config 0x46 [7:0] = 0x20	Enables the Watchdog timer. Sets the Watchdog timer to 0x20.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
X								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

8.15 Flash Controller

The programming sequence below hides the flash controller.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_IO 0xDC [7] = 0x0 PM_IO 0xDC [1:0] = 0x01	Hides flash controller

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

8.16 Enhance ALIGN Checking after OOB for Gen 3

This section targets the OOB compatibility for Gen3 (6.0 Gbps) devices.
The following programming sequence will increase the number of consecutive ALIGN primitive checking after OOB (when Host is in HR_AwaitAlign state). As a result, Host can proceed to HR_SendAlign state after CDR becomes more stable and can avoid the CDR pseudo-lock period. Because S5 shadow register load back is used, there is no need to restore the value after S3.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	1. SATA_PCI_config 0x84[26] = 0x0 2. SATA_PCI_config 0x84[13:12] = 0x3 3. SATA_PCI_config 0xA0[6:2] = 0x0F	1. Enable S5 shadow register reload. 2. Prepare to change the Gen3 PHY fine-tune registers 3. Program Host to check 127 consecutive ALIGNs before checking 3 back-to-back non-ALIGN *Note: #1 and #2 can be performed using one PCI configuration write because they are at the same offset, provided that the rest of the 32 bit values are unchanged.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
x								
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			

9 SATA IDE Controller 2: (bus-0, dev-20, fun-01)

9.1 Restoring SATA IDE Controller2 Registers after S3 Resume State

The registers in section *9.3 Hide MSI Capability of IDE Controller 2* must be restored by SBIOS after S3 resume for the SATA controller if the registers' values are programmed differently from the reset default values.

9.2 Optionally Disable SATA IDE Controller 2

The programming sequence detailed below disables SATA IDE Controller 2. This bit is also known as "Combined_Mode Disable".

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_IO 0xDA [3] = 1	When this bit is set, the SATA IDE Controller 2 (bus-0, dev-20, fun-01) will be disabled. Port4/5 are owned by SATA Controller (bus-0, dev-17, fun-00)

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the Hudson1 Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe Bridges	I/O REG	XIOAPIC			
		x						

9.3 Hide MSI Capability of IDE Controller 2

The programming sequence detailed below disables MSI support of SATA IDE Controller 2.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	1. PATA_PCI_config 0x40 [0] = 1 2. PATA_PCI_config 0x34 [7:0] = 0x00 3. PATA_PCI_config 0x06 [4] = 0x0 4. PATA_PCI_config 0x40 [0] = 0	Enable modification to capabilities pointer. Hide the MSI. Set [Capabilities List] field as logic zero. Disable modification to capabilities pointer.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
			x					
RTC	ACPI	PM REG	UMI/PCIe Bridges	I/O REG	XIOAPIC			

9.4 Channel Selection

This selection of IDE Primary or Secondary channel is no longer required in current implementation.

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_IO 0xDA [1] = 0 (default)	Port4/5 will be utilizing Primary IDE channel of SATA IDE Controller 2 (bus-0, dev-20, fun-01)

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe Bridges	I/O REG	XIOAPIC			
		x						

10 HD Audio (bus-0, dev-20, fun-2)

10.1 Enabling/Disabling HD Audio Controller

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_Reg 0xEB [0] = 1 (default)	0 = Disable the HD Audio controller 1 = Enable the HD Audio controller

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

10.2 HD Audio I/O Pad Configuration

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	GPIO_Reg 0xA7 [7:0] = 0x3E GPIO_Reg 0xA8 [7:0] = 0x3E GPIO_Reg 0xA9 [7:0] = 0x3E GPIO_Reg 0xAA [7:0] = 0x3E	See Register Specification for individual bit definition. Hudson-1 HD Audio Controller supports up to 4 codecs with one AZ_SDIN from each codec. The four AZ_SDIN pins are shared with GPIO 167 – 170. If a particular pin is to be used for HD Audio functionality, in addition to being configured for Azalia, and if the integrated pull-down is to be used rather than an external pull-down resistor, the appropriate bits need to be set. For example, if only GPIO167 and GPIO168 are to be used for Azalia, then only 0xA7 and 0xA8 need to be programmed to 0x3E.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
				x				

11 GEC (bus-0, dev-20, fun-06)

11.1 GEC I/O Termination Setting

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	PM_Reg 0xF6 = Power-on default setting PM_Reg 0xF7 = Power-on default setting PM_Reg 0xF8 = 0x6C PM_Reg 0xF9 = 0x27 PM_Reg 0xFA = 0x00	Hudson-1 GEC RGMII I/O Pad settings for 3.3V CMOS

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

12 On-Chip Clock Generator

12.1 FC Clocks Settings

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	MISC_Reg 0x40 [16] = 1 MISC_Reg 0x40 [11:9] = 0x6	Hudson-1 does not support the Flash function. Turn off Flash clocks for power saving.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

Note: MISC_Reg is defined at register space AcpiMMioAddr + 0xE00 ~ 0xEFF. The base address "AcpiMMioAddr" is defined at PM_IO x24 [31:12].

12.2 Internal Clock Generator Enable Status

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	MISC_Reg 0x80 [4] = 1 (Read only)	Set LPCCLK1 pin strap to '1' to enable internal clock generator. SBIOS should read the PM_MISC_Reg x80[4] as '1' to indicate internal clock generator mode enable.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

Note: MISC_Reg is defined at register space AcpiMMioAddr + 0xE00 ~ 0xEFF. The base address "AcpiMMioAddr" is defined at PM_IO x24 [31:12].

12.3 Spread Spectrum Settings

12.3.1 Enable SS Settings

ASIC Rev	Register Settings	Function/Comment
Hudson-1 spread spectrum can be enabled by the following sequence when the chip is configured for internal clock or external clock mode. Refer to section 12.2 above.		
Hudson-1 All Revs	Misc_Reg 0x40 [25] = 1b Misc_Reg 0x18 [15:8] = 83h ***INTERNAL CLOCK MODE*** Misc_Reg 0x18[25:21] = 01h ***EXTERNAL CLOCK MODE*** Misc_Reg 0x18 [25:21] = 04h Misc_Reg 0x10 [23:0] = 9975BEh Misc_Reg 0x08 [31:24] = 91h	-> Allow to change spread profile SS divisor based on reference clock 25 MHz SS divisor based on reference clock 100 MHz -> New spread profile

	Misc_Reg 0x08 [15:8] = 21h Misc_Reg_08h [0] = 1b	-> Enable spread

Miscellaneous registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from “AcpiMMioAddr “ + 0xE00 to “AcpiMMioAddr” + 0xEFF.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

12.3.2 Disable SS Settings

ASIC Rev	Register Settings	Function/Comment
Hudson-1 spread spectrum can be disabled by the following sequence when the chip is configured for internal clock or external clock mode. Refer to section 12.2 above.		
Hudson-1 All Revs	Misc_Reg_40h [25] = 0b Misc_Reg_08h [0] = 0b	-> Disable change of spread profile (power up default) -> Disable spread (power up default)

Miscellaneous registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from “AcpiMMioAddr “ + 0xE00 to “AcpiMMioAddr” + 0xEFF.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

12.4 PLL 100Mhz Reference Clock Buffer Setting for Internal Clock Generator Mode

ASIC Rev	Register Settings	Function/Comment
Hudson-1 All Revs	MISC_Reg 0x04 [13] = 1	Set this bit to “1” to turn off 100MHz reference clock input buffer in internal clock generator mode for power saving.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	UMI/PCIe BRIDGES	I/O REG	XIOAPIC			
		x						

Note: MISC_Reg is defined at register space AcpiMMioAddr + 0xE00 ~ 0xEFF. The base address “AcpiMMioAddr” is defined at PM_IO 0x24 [31:12].

12.5 Spread Profile for Ontario APU Related Platform

ASIC Rev	Register Settings	Function/Comment
Apply the following setting if the APU is of Family 14h and models 00h to 0Fh. (Ontario APU)		
Hudson-1 All Revs	MISC_Reg 0x40[25] = 1b Misc_Reg x08[0] = 0b Misc_Reg x18[15:5] = 418h Misc_Reg x18[19:16] = 0b Misc_Reg x10[23:8] = 828Fh Misc_Reg x10[7:0] = A8h Misc_Reg x1C[5:0] = 00h Misc_Reg x08[31:28] = 1h Misc_Reg x08[7] = 0b Misc_Reg x08[8] = 1b Misc_Reg x10[25:24] = 01b Misc_Reg x08[0] = 1b	This spread profile setting is for HDMI & DVI output from DP with -0.425%.

SATA	USB	SMBUS	PATA	AC97	HD AUDIO	LPC	PCI	For register details refer to the sections check-marked in the A45/A50/A55M Register Reference Guide
RTC	ACPI	PM REG	A-LINK	I/O REG	XIOAPIC			
		x						

Note: MISC_Reg is defined at register space AcpiMMioAddr + 0xE00 ~ 0xEFF. The base address “AcpiMMioAddr” is defined at PM_IO 0x24 [31:12].

Appendix: Revision History

Date	Revision	Description
February, 2012	3.00	• Released as a public version. • Added new Section 2.13 PCIe® Wake Status and PME Wake Status.
May, 2011	2.02	• Changed the document title to show the marketing names of the Hudson-1 family members instead of the engineering codename. • Updated Section 2.5 Mt C1e Enable. • Added new section 2.12 PCIe Native Mode. • Updated Section 3.5 Spi Prefetch Enhancement. • Added new Section 5.18 GPP Immediate Ack PM_Active_State_Request_L1. • Updated Section 5.19.1 by adding programming sequence for hot unplug of PCIe device. • Added new Section 7.17 Frame Babble Detection.
January, 2011	2.01	• Added new setting PM_Reg 0x80[7] = 1b to Section 2.5 Mt C1e Enable. • Updated Section 5.15 GPP Endpoint L1/L0s (ASPM).
November, 2010	2.00	• Added variant Hudson-E1 to the document. • Added new Section 2.5 Mt C1e Enable. • Added new Section 2.11 HWM Sensor Clk. • Updated Section 3.5 Spi Prefetch Enhancement. • Updated section 4.12 (including changing title from “A-Link L1 Entry Delay Shortening” to “A-Link L0s/L1 NAK Reduction”. • Updated Section 5.3 GPP Reset. • Removed previous section 5.14 GPP Lane Reversal Support. • Added new Section 7.16 USB DLL Reset Sequence. • Updated Section 8.13 SATA MSI and D3 Power State Capability. • Added new Section 12.5 Spread Profile for Ontario APU Related Platform.
June, 2010	1.02	• Updated Figure 1 Hudson-1 Internal PCI Devices and Major Functional Blocks. • Updated Section 2.1 Revision ID. • Added new Section 2.3 MMIO Programming for Legacy Devices. • Added new Section 2.7 SMAF Matching Setting. • Added new Section 2.8 Keyboard Reset Settings for Legacy Free Systems. • Added new Section 2.9 NB Power Good Control on System Reset • Fixed typo in Section 7.6 USB Delay A-Link Express L1 State where ABCFG_reg x 90 [16] was corrected to ABCFG_reg x 90 [17] • Updated Section 7.7 USB 2.0 Ports Driving Strength. • Added new Section 8.3 Staggered SATA PHY DLL Reset • Added reference to section 8.3 in Section 8.7 Restoring SATA Registers after S3 Resume State. • Added a new setting (3) to Section 9.3 “Hide MSI Capability of IDE Controller 2”. • Fixed typo in section heading of Section 10 “HD Audio (bus-0, dev-20, fun-2)”
March, 2010	1.01	• Edited description of step 2 in section 5.19 GPP Power Saving. • In section 5.20 GPP Gen2 Speed Change, for step 5, added what to do if GPP is NOT in Compliance Pattern testing mode. • Added comments to section 7.1 “OHCI and EHCI Controllers” to explain that USB controllers must be disabled in pairs. • Fixed typo in section 7.6 “USB Delay UMI L1 State”, where bit[16] of ABCFG_Reg 0x90 was changed to bit[17]. • Added three new sub-sections to section 9 “SATA IDE Controller 2: (bus-0, dev-20, fun-01)”
December, 2009	1.00	• First release.