AMD A45/A50M/A55E Fusion Controller Hub Register Reference Guide

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Advanced Micro Devices

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Revision History

Date	Revision	Description
May 2012	3.05	• Added new register BlinkControl [PM_Reg: DFh]
April 2012	3.03	• Simple rev number jump due to release of public version rev 3.02.
January 2012	3.01	• Section 4.3.1 PCIe® Bridges: o Corrected default value of bits[15:0] of SSID_ID [pcieCfg0: 0xB4]. • Section 3.1.5 ASF SMBus Host Interface Registers: o Updated ASFStatus [ASF_IO: 0Ah] o Updated DataBankSel [ASF_IO: 13h]
November 2011	3.00	• Update to section 2.3.3 Power Management (PM) Registers: o Updated description of bits[19:18] of IsaDecode [PM_Reg: 00h].
May 2011	2.01	• Changed cover title and updated the Introduction to show marketing names of the Hudson-1 family. • Update to section 2.2.6.2 EHCI Operational Registers: o Added new bit[11] description to EOR MISC Control [EOR_Reg : EHCI_EOR + 9Ch] • Update to section 2.3.3 Power Management (PM) Registers: o Updated description of bit[7] (Force_smaf_match) of PciControl [PM_Reg: 08h]. o Updated WatchDogTimerEn [PM_Reg: 48h] • Update to section 3.1.6 WatchDogTimer Registers: o Changed default value of bit[3] of WatchDogControl [WD_Mem_Reg: 00h]
November 2010	2.00	• Added Hudson-E1 to the document. • Changed EC to IMC throughout the document. • Updated Figure 2: Hudson-1 PCI Internal Devices. • Updates to section 2.1 SATA Controller (Device 17, Function 0): o Added a note to four MSI_* registers (PCI_Reg 50h to 5Ch) that SATA MSI is not supported. • Added new section 2.1.4 IDE Controller Registers (Bus 0, Device 20, Function 1). • Updates to section 2.3.1 PCI Configuration Registers Definition: o Changed defaulft value of bit[4] of STATUS [PCI_Reg: 06h] from 1 to 0. • Updates to section 2.3.2 ACPI Registers: o Updated bits[12:10] and bit[13] of [AcpiPm1CntBlk:00h]. o Renamed PmaControl [AcpiPmaCntBlk: 00h] to Pm2Control [AcpiPm2CntBlk: 00h]. • Update to section 2.3.3 Power Management (PM) Registers: o Changed setting of 1 to 0 for bit[7] (Force_smaf_match) of

Date	Revision	Description
		PciControl [PM_Reg: 08h]. o Updated WatchDogTimerEn [PM_Reg: 48h] o Updated WatchDogTimerConfig [PM_Reg: 4Ch] o Updated description of RtcShadow [PM_Reg: 5Bh]. o Removed AcpiPm2CntBlk [PM_Reg: 6Ch], while renaming AcpiPmaCntBlk [PM_Reg: 6Eh] to that name. o Updated bit[6] of CStateEn [PM_Reg: 7Eh] o Updated bits 17 and 18 of BreakEvent [PM_Reg: 80h] o Made bit[13] (LDTSTPCMD) of [PM_Reg: 88h] reserved. o Updated bits 2, 3, 4, [13:12] and [15:14] of MessageCState [PM_Reg: A0h] o Updated bit[21] of S5/Reset Status [PM_Reg: C0h]. o Changed bit[21] of MiscFixReg [PM_Reg: C0h] from reserved to UsrRst2NbPwrGdDis o Updated description of bit[6] (TwarnEn) of Misc [PM_Reg: C8h]. o Clarified description of bit[2] (SetMaxGen2) of SataConfig [PM_Reg: DAh]. o Updated description of bit[1] (PCIDisable) of PcibConfig [PM_Reg: EAh] o Updated description of bit [0] of USBControl [PM_Reg: F0h]. • Update to section 2.3.4 Power Management Block 2 (PM2) Registers: o Added recommended value for bits[3:0] of HwmClkControl [PM2_Reg: EFh]. • Updates to section 2.3.5 SMI Registers: o For these registers: SciMap6 [SMI_Reg:58h], SmiStatus0 [SMI_Reg:80h] and SmiControl1 [SMI_Reg:A4h], interchanged device 22 with device 20 in the field descriptions releated to events 26 and 27. • Updates to section 3.1.8 Real Time Clock (RTC) o Added a note that when Bank 1 is selected, byte offsets 00h – 0Dh Time/Alarm/Control registers and byte offsets 0Eh – 3Fh User RAM are read-only. o Updated Figure 3: Register Bank Definition and Memory Address Mapping. • Update to section 3.2 Host PCI Bridges Registers: o Changed bits[2:1] of PCICLK Enable Bits [PCI_Reg:4Ah] to Reserved. o Updated description of bit[3] (PCICLK7Enable) of PCICLK Enable Bits [PCI_Reg:4Ah] to ensure that it is always set to 1. • Update to the following registers in section 3.2.1 ABCFG Registers: o MiscCtl_54 [ABCFG_Reg:54h] o BIF Control 1 [ABCFG_Reg:98h]

Date	Revision	Description
		○ BIF Control 0 [ABCFG_Reg:90h] • Updates to section 4.3 PCIe® Bridge Register Descriptions (Device 21, Function 0/1/2/3): ○ All variants support up to 4 GPP ports. ○ Changed default value of SUB_CLASS [pcieCfg0:0xA] ○ Changed default value of BASE_CLASS [pcieCfg0:0xB] ○ Changed default value of bit 7 of HEADER [pcieCfg0:0xB] • Added new Chapter 5 Integrated Micro-Controller Registers.
November 2009	1.00	• First NDA release.

Chapter 1 Introduction

1.1 About this Manual

This manual is a register reference guide for the AMD Hudson-1 family of FCH. The Hudson-1 is designed to operate with AMD's APUs in desktop, mobile, and embedded platforms.

Note: The term Hudson-1 is used in this document to refer to the following Hudson-1 family members:

Marketing Name	Codename
A45	Hudson-D1
A50M	Hudson-M1
A55E	Hudson-E1

The information in this document applies to all members of the Hudson-1 family unless otherwise indicated. For the differences between the variants, refer to their respective databooks available at the AMD NDA site.

1.2 Nomenclature and Conventions

1.2.1 Recent Updates

Updates recent to each revision are highlighted in red.

1.2.2 Numeric Representations

- Hexadecimal numbers are prefixed with "0x" or suffixed with "h," whenever there is a possibility of confusion. Other numbers are decimal.
- Registers (or fields) of an identical function are sometimes indicated by a single expression in which the part of the signal name that changes is enclosed in square brackets. For example, registers HOST_DATA0 through to HOST_DATA7 is represented by the single expression HOST_DATA[7:0].

1.2.3 Register Description

All registers in this document are described with the format of the sample table below. All offsets are in hexadecimal notation, while programmed bits are in either binomial or hexadecimal notation.

Table 1: Notation—Example

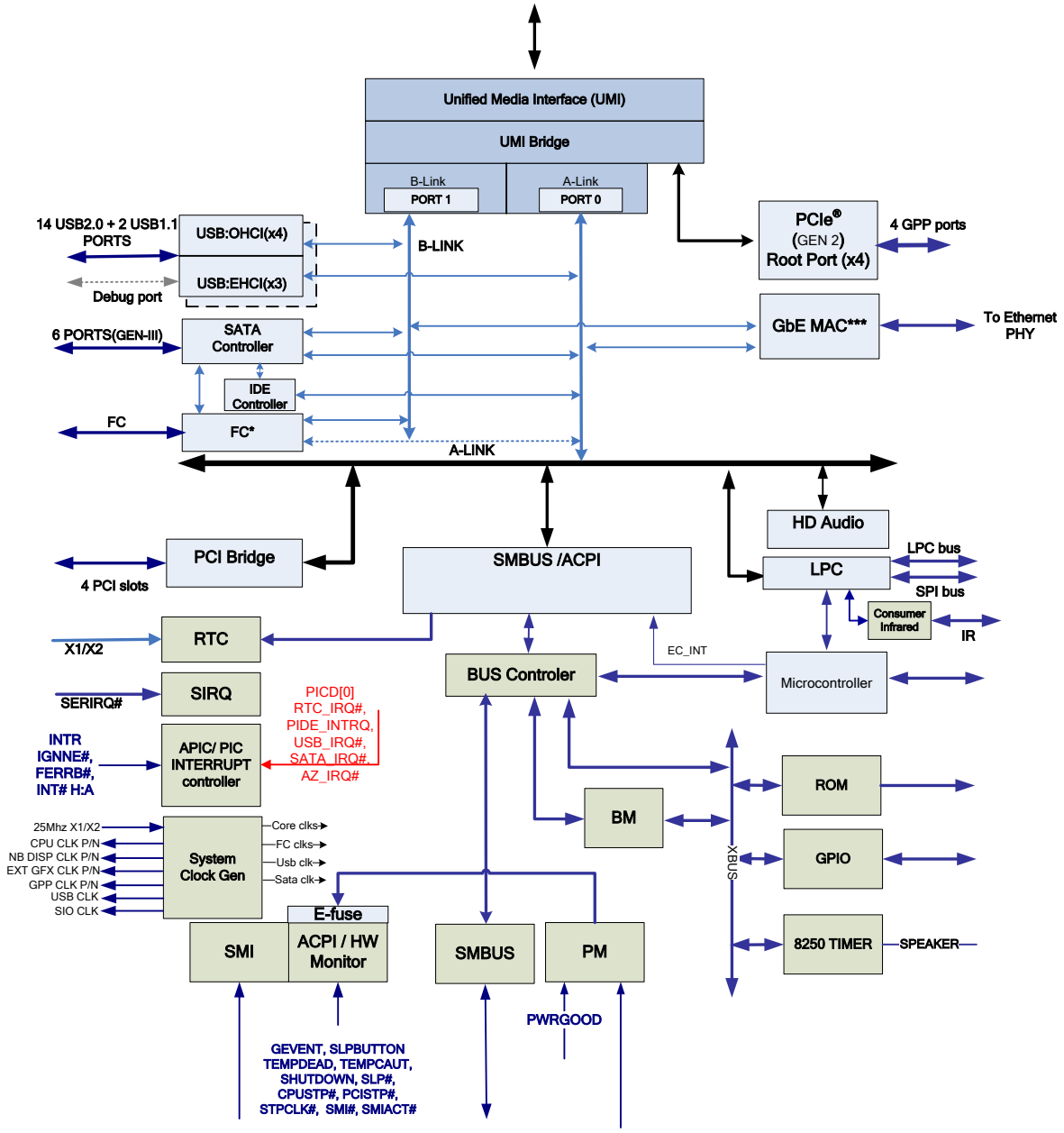
Latency Timer – RW – 8 bits – [Offset: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Latency Timer (R/W)	7:0	00h	This bit field is used to specify the time in number of PCI clocks, the SATA controller as a master is still allowed to control the PCI bus after its GRANT_L is deasserted. The lower three bits [0A:08] are hardwired to 0 h, resulting in a time granularity of 8 clocks.
Latency Timer. Reset Value: 00h			

Register Information	Value/Content in the Example
Register name	Latency Timer
Read / Write capability R = Readable W = Writable RW = Readable and Writable	RW
Register size	8 bits
Register address(es)*	Offset: 0Dh
Field name	Latency Timer (R/W)
Field position/size	7:0
Field default value	00h
Field description	“This bit … 8 clocks.”
Field mirror information	
Brief register description	Latency Timer. Reset Value: 00h
*** Note**: There maybe more than one address; the convention used is as follows: **[aperName:offset]** - single mapping, to one aperture/decode and one offset **[aperName1, aperName2, …, aperNameN:offset]** - multiple mappings to different apertures/decodes but same offset **[aperName:startOffset-endOffset]** - mapped to an offset range in the same aperture/decode	

Warning: Do not attempt to modify values of registers or bit fields marked "Reserved." Doing so may cause the system to behave in unexpected manners**.**

1.3 Block Diagram

Figure 1 below shows the Hudson-1 internal PCI devices and the major function blocks.



Notes:
* Flash controller function is not supported on all Hudson-1 variants.
** PCI controller function is not supported on some Hudson-1 variants.
*** GbE MAC is not supported on some Hudson-1 variants.

Figure 1: Hudson-1 PCI Internal Devices and Major Function Blocks

Chapter 2 Register Descriptions: PCI Devices

Note: The Hudson-1 internal PCI devices are listed in *Figure 2* below. The sub-sections that follow provide descriptions of the PCI configuration space, the I/O space, and the memory space registers for each device. PCI configuration space registers are only accessible with configuration Read or configuration Write cycles and with the target device selected by settling its corresponding IDSEL bit in the configuration cycle address field.

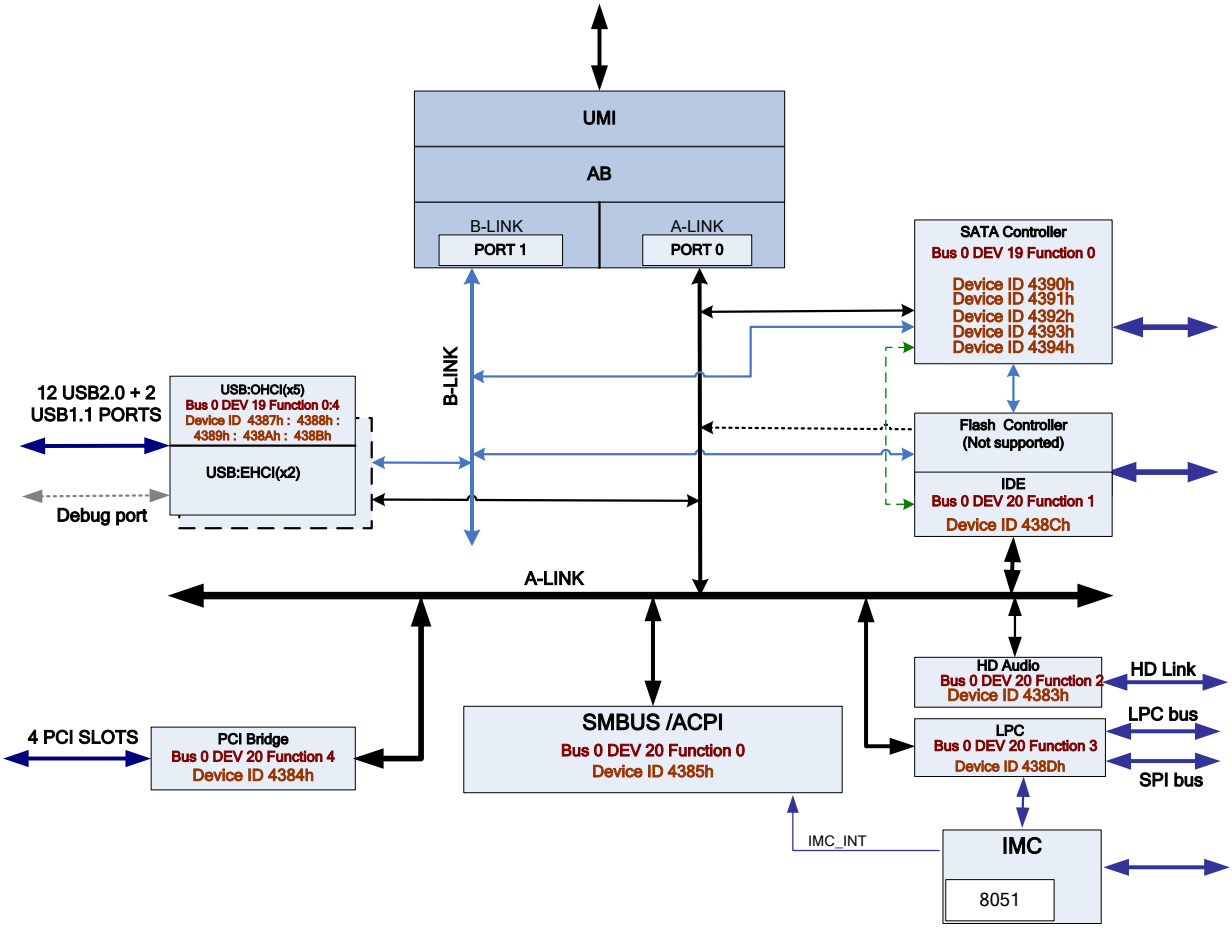


Figure 2: Hudson-1 PCI Internal Devices

2.1 SATA Controller (Device 17, Function 0)

2.1.1 PCI Configuration Registers

These registers are accessible only when the SATA controller detects a Configuration Read or Write operation, with its IDSEL asserted, on the 32-bit PCI bus.

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID/Class Code	08h
Cache Link Size	0Ch
Master Latency Timer	0Dh
Header Type	0Eh
BIST Mode Type	0Fh
Base Address 0	10h
Base Address 1	14h
Base Address 2	18h
Base Address 3	1Ch
Bus Master Interface Base Address	20h
AHCI Base Address	24h
Subsystem ID and Subsystem Vendor ID	2Ch
Capabilities Pointer	34h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min_gnt	3Eh
Max_latency	3Fh
Misc control	40h
Watch Dog Control And Status	44h
Watch Dog Counter	46h
Reserved	48h
MSI Control	50h
MSI Address	54h
MSI Upper Address	58h
MSI Data	5Ch
Power Management Capability ID	60h
Power Management Capability	62h
Power Management Control And Status	64h
Serial ATA Capability Register 0	70h
Serial ATA Capability Register 1	74h
IDP Index	78h
IDP Data	7Ch
Reserved	80h
Reserved	82h
PHY Core Control Settings	84h
Reserved	88h
Reserved	8Ch
Reserved	8Eh
Reserved	90h
PHY PortX GenX Fine Tune	94h
Reserved	98h
Reserved	9Ch
Reserved	A0h
Advanced Features Capability Register0	A4h
Advanced Features Capability Register1	A8h

Register Name	Offset Address
Reserved	AAh
Port0 BIST Error Count	ACh
Port0 BIST Control/Status	B0h
Reserved	B2h
Port1 BIST Error Count	B4h
Port1BIST Control/Status	B8h
Reserved	BAh
Port2 BIST Error Count	BCh
Port2 BIST Control/Status	C0h
Reserved	C2h
Port3 BIST Error Count	C4h
Port3 BIST Control/Status	C8h
Reserved	CAh
Port4 BIST Error Count	CCh
Port4 BIST Control/Status	D0h
Reserved	D2h
Port5 BIST Error Count	D4h
Port5 BIST Control/Status	D8h
Reserved	DAh
BIST pattern Count	DCh
PCI Target Control TimeOut Counter	E0h
Reserved	E2h
T-Mode BIST Transit Pattern DW1	E4h
T-Mode BIST Transit Pattern DW2	E8h
BIST Transmit Pattern Definition	ECh
Reserved	EE-EFh
20-BIT BIST Transmit Pattern	F0
Reserved	F3-FFhh

Vendor ID – R – 16 bits – [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1002h	Vendor Identifier. The vendor ID is 1002h. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor IDs.

Device ID – R – 16 bits – [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	4390h	This register holds a unique 16-bit value assigned to a device. . 4390h for IDE controller, 4391h for AHCI controller, 4392h for RAID controller, 4393h for RAID 5 controller, E-fuse will default/limit for non-RAID 5 controller. Note: When E-fuse ROM bit 133 is enabled, the default value of Device ID is 4393h. Reg0x40[0] (I/O Access Enable) should be set to 1, then the value of DEVICE ID can be changed. After that, if reg0x40[0] is cleared, the new value will stay and won't change to the default value of 4393h. When E-fuse ROM bit 133 is disabled, Device ID can be programmed only to 4390/4391/4392. Attempts to program Device ID with 4393h when E-fuse ROM bit 133 is disabled will result in Device ID becoming 4392h.

Command – RW – 16 bits – [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Access Enable	0	0b	This bit controls access to the I/O space registers. When this bit is 1, it enables the SATA controller to respond to PCI I/O space access.
Memory Access Enable	1	0b	This bit controls access to the memory space registers. When this bit is 1, it enables the SATA controller to respond to PCI memory space access.
Bus Master Enable	2	0b	Enable or disable the device behaving as a Bus Master. 1: Enable 0: Disable.
Special Cycle Recognition Enable	3	0b	Read Only. Hard-wired to 0 indicating no special support.
Memory Write and Invalidate Enable	4	0b	Read Only. Hard-wired to 0 indicating that Memory Write and Invalidate Enable is not supported.
VGA Palette Snoop Enable	5	0b	Read Only. Hard-wired to 0 indicating the SATA host controller does not need to snoop VGA palette cycles.
PERR# Detection Enable	6	0b	If set to 1, the IDE host controller asserts PERR# when it is the agent receiving data AND when it detects a parity error. PERR# is not asserted if this bit is 0..
Wait Cycle Enable	7	0b	Read Only. Hard-wired to 0 indicating the SATA controller does not need to insert a wait state between the address and the data on the AD lines.
SERR# Enable	8	0b	If set to 1 and bit[6] is set, the SATA controller asserts SERR# when it detects an address parity error. SERR# is not asserted if this bit is 0..
Fast Back-to-Back Enable	9	0b	Read Only. Hard-wired to 0 indicates that fast back to back to the same agent are allowed only.
Interrupt Disable	10	0b	This bit disables the device/function from asserting INTx#. 0: Enable the assertion of the device/function's INTx# signal. 1: Disable the assertion of the device/function's INTx# signal.
Reserved	15:11	00h	Reserved.

Status – RW – 16 bits – [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0h	Reserved.
Interrupt Status	3	0b	This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's **INTx#** signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
Capabilities List	4	1b	Read Only. Default to 1 to indicate that the Capabilities Pointer is located at 34h. Can be programmed if reg0x40[0] (I/O Access Enable) is set.
66MHz Support	5	1b	66MHz capable. This feature is supported in the SATA controller.
Reserved	6	0b	Reserved.

Status – RW – 16 bits – [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Fast Back-to-Back Capable	7	0b	Read Only. Hard-wired to 0 indicating that Fast Back-to-Back is incapable.
Data Parity Error	8	0b	Data Parity Reported. Set to 1 if SATA controller detects PERR# asserted while acting as PCI master (regardless whether PERR# was driven by SATA controller or not.) Writing a 1 clears this bit.
DEVSEL# Timing	10:9	01b	Read only. These bits indicate DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
Signaled Target Abort	11	0b	This bit is set to 1, when the SATA controller signals Target Abort. Writing a 1 clears this bit.
Received Target Abort	12	0b	This bit is set to 1 when the SATA controller generated PCI cycle (SATA controller is the PCI master) is aborted by a PCI target. Writing a 1 clears this bit.
Received Master Abort Status	13	0b	Received Master Abort Status. Set to 1 when the SATA controller acting as a PCI master, aborts a PCI bus memory cycle. Writing a 1 clears this bit.
SERR# Status	14	0b	SERR# status. This bit is set to 1 when the SATA controller detects a PCI address parity error. Writing a 1 clears this bit.
Detected Parity Error	15	0b	Detected Parity Error. This bit is set to 1 when the SATA controller detects a parity error. Writing a 1 clears this bit.

Revision ID/Class Code - R – 32 bits – [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	40h	These bits default to 40h to indicate the revision level of the chip design.
Operating Mode Selection	15:8	8Fh	RW Programmable I/F. Bit[15] – Master IDE Device. Always 1. Bit[14:12] – Reserved. Always read as 0's. Bit[11] – Programmable indicator for Secondary. Always 1 to indicate that both modes are supported. Bit[10] – Operating Mode for Secondary. 0: Compatibility Mode 1: Native PCI-mode Bit[9] – Programmable indicator for Primary. Always 1 to indicate that both modes are supported. Bit[8] – Operating Mode for Primary. 0: Compatibility Mode 1: Native PCI-mode See Note 1*
Sub-Class Code	23:16	01h	Sub-Class Code. 01h to indicate an IDE Controller. See Note 2**
Class Code	31:24	01h	Class Code. These 8 bits are read only and wired to 01h to indicate a Mass-Storage Controller.

*Note 1: All eight bits are writable when reg0x40[0] (CC_reg_wr_en) is set. Also when Sub-Class Code is 01h, indicating an IDE controller, bits[11:8] are writable.

**Note 2 This field is only writable when reg0x40[0] (CC_reg_wr_en) is set.

Sub-Class Code	Program Interface:	Controller Type
01	8F	IDE
06	01	AHCI
04	00	RAID

Cache Line Size – RW – 8 bits – [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Reserved
Cache Line Size	7:4	0h	If the value is 1, cache line size is 16 DW (64 byte).

Master Latency Timer – RW – 8 bits – [PCI_Reg:0Dh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0h	Reserved
Master Latency Timer	7:3	00h	This field specifies, in units of PCI bus clocks, the guaranteed time slice allowed to IDE host controller for burst transactions.

Header Type – R – 8 bits – [PCI_Reg:0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	6:0	00h	Since the IDE host controller is a single-function device, this field contains a value of 00h.
Multi-function device	7	0b	This bit defaults to 0b to indicate single-function device.

BIST Mode Type – RW – 8 bits – [PCI_Reg:0Fh]			
Field Name	**Bits**	**Default**	**Description**
Completion Code	3:0	0h	Read Only. Indicates the completion code status of BIST. A non-zero value indicates a failure.
Reserved	5:4	0h	Reserved
Start BIST	6	0	Since bit[7] is 0, programming this bit has no effect.
BIST Capable	7	0	Read Only. Hard-wired to 0 indicating no HBA related BIST function.

Base Address 0 – RW – 32 bits – [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	2:1	0h	Reserved.
Primary IDE CS0 Base Address	31:3	0000_0000h	In IDE mode: Base address for Primary IDE Bus CS0. This register is used for native mode only. Base Address 0 is not used in compatibility mode.

Base Address 1 – RW – 32 bits – [PCI_Reg:14h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	1	0b	Reserved.
Primary IDE CS1 Base Address	31:2	0000_0000h	In IDE mode: Base Address for Primary IDE Bus CS1. This register is used for native mode only. Base Address 1 is not used in compatibility mode.

Base Address 2 – RW – 32 bits – [PCI_Reg:18h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to the I/O space.
Reserved	2:1	0h	Reserved.

Base Address 2 – RW – 32 bits – [PCI_Reg:18h]			
Field Name	**Bits**	**Default**	**Description**
Secondary IDE CS0 Base Address	31:3	0000_ 0000h	In IDE mode: Base Address for Secondary IDE Bus CS0. This register is used for native mode only. Base Address 2 is not used in compatibility mode.

Base Address 3 – RW – 32 bits – [PCI_Reg:1Ch]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to I/O space.
Reserved	1	0b	Reserved.
Secondary IDE CS1 Base Address	31:2	0000_ 0000h	Base Address for Secondary IDE Bus CS1. This register is used for native mode only. Base Address 3 is not used in compatibility mode.

Bus Master Interface Base Address – RW – 32 bits – [PCI_Reg:20h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	This bit is wired to 1 to indicate that the base address field in this register maps to I/O space.
Reserved	3:1	0h	Reserved.
Bus Master Interface Register Base Address	31:4	0000_ 0000h	Base Address for Bus Master interface registers and correspond to AD[31:4].

AHCI Base Address – RW – 32 bits – [PCI_Reg:24h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	0b	This bit is wired to 0 to indicate a request for register memory space.
Reserved	9:1	00h	Reserved.
AHCI Base Address	31:10	000000h	Base address of register memory space. This represents a memory space for support of 4 ports.

Subsystem ID and Subsystem Vendor ID – RW – 32 bits – [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	Subsystem Vendor ID. Can only be written once by software.
Subsystem ID	31:16	0000h	Subsystem ID. Can only be written once by software.

Write once and read only.

Capabilities Pointer – R – 8 bits – [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	60h	The first pointer of Capability block. Can be programmed if reg0x40[0] (CC_reg_wr_en) is set.

Interrupt Line – RW – 8 bits – [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	Identifies which input on the interrupt controller the function's PCI interrupt request pin (as specified in its Interrupt Pin register) is routed to.

Interrupt Pin – R – 8 bits – [PCI_Reg:3Dh]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin	7:0	01h	Hard-wired to 01h.

Min_gnt – R – 8 bits – [PCI_Reg:3Eh]			
Field Name	**Bits**	**Default**	**Description**
Minimum Grant	7:0	00h	This register specifies the desired settings for how long of a burst the SATA controller needs. The value specifies a period of time in units of ¼ microseconds. Hard-wired to 0's and always read as 0's.

Max_latency – R – 8 bits – [PCI_Reg:3Fh]			
Field Name	**Bits**	**Default**	**Description**
Maximum Latency	7:0	00h	This register specifies the Maximum Latency time required before the SATA controller as a bus-master can start an access. Hard-wired to 0's and always read as 0's.

Misc Control – RW – 32 bits – [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
Subclass Code Write Enable	0	0b	Once set, Program Interface register (PCI_Reg:09h), Subclass code register (PCI_Reg:0Ah), Multiple Message Capable bits (PCI_Reg50h[19:17]) can be programmable.
Reserved	15:1	0h	
Disable port0	16	0b	When set, PHY port0 is disabled, port0 clock at link/transport layer is shut down.
Disable port1	17	0b	When set, PHY port1 is disabled, port1 clock at link/transport layer is shut down.
Disable port2	18	0b	When set, PHY port2 is disabled, port2 clock at link/transport layer is shut down.
Disable port3	19	0b	When set, PHY port3 is disabled, port3 clock at link/transport layer is shut down.
Disable port4	20	0b	When set, PHY port4 is disabled, port4 clock at link/transport layer is shut down.
Disable port5	21	0b	When set, PHY port5 is disabled, port5 clock at link/transport layer is shut down.
Reserved	31:22	0b	

Watch Dog Control And Status – RW – 16 bits – [PCI_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
Watchdog Enable	0	0b	Set the bit to enable the watchdog counter for all the PCI down stream transactions for SATA ports.
Watchdog Timeout Status	1	0b	Watchdog Counter Timeout Status bit. This bit indicates that the watchdog counter has expired for PCI down stream transaction and as a result, the transaction was aborted. Software write of 1 clears the status.
Reserved	15:2	0h	Reserved.

Watch Dog Counter – RW – 16 bits – [PCI_Reg:46h]			
Field Name	**Bits**	**Default**	**Description**
Watchdog Counter	7:0	80h	Specifies the timeout retry count for PCI down stream retries. This value is used for SATA ports.
Reserved	15:8	00h	Reserved.

Reserved– RW – 32 bits – [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0b	

MSI Control – RW- 32 bits – [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	05h	Read Only. Capability ID, indicates this is MSI capability ID.
Capability Next Pointer	15:8	70h	Read-Only. Defaults to 70h, points to Index Data pair capability.
Message Signaled Interrupt Enable	16	0b	MSI Enable.
Multiple Message Capable	19:17	010b	Multiple Message Capable (MMC).
Multiple Message Enable	22:20	0h	Multiple Message Enable (MME).
MSI 64-bit Address	23	1b	Read Only 64-bit address supported.
Reserved	31:24	00h	Reserved.
Note: SATA MSI is not supported			

MSI Address – RW- 32 bits – [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0h	Reserved.
MSI Address	31:2	0000_0000h	Lower 32 bits of the system specified message address. Always DW aligned.
Note: SATA MSI is not supported			

MSI Upper Address – RW- 32 bits – [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
MSI Upper Address	31:0	0000_0000h	Upper 32 bits of the system specified message address.
Note: SATA MSI is not supported			

MSI Data – RW- 16 bits – [PCI_Reg:5Ch]			
Field Name	**Bits**	**Default**	**Description**
MSI Data	15:0	0000h	MSI Data
Note: SATA MSI is not supported			

Power Management Capability ID – R – 16 bits – [PCI_Reg:60h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	01h	Default = 01h. Indicates that this pointer is a PCI power management.
Capability Next Pointer	15:8	50h	Hardwired to 50h, points to MSI Capability.

Power Management Capability – R- 16 bits – [PCI_Reg:62h]			
Field Name	**Bits**	**Default**	**Description**
Version (VS)	2:0	010b	Indicates support for Revision 1.1 of the *PCI Power Management Specification.*
PME Clock (PMEC)	3	0b	Indicates that PCI clock is not required to generate PME#.
Reserved	4	0b	Reserved
Device Specific Initialization	5	1b	Indicates whether device-specific initialization is required. Hard wired to 1.
Aux_Current	8:6	0h	Reports the maximum Suspend well current required when in the $D3_{COLD}$ state. Hardwire to 000b.
D1_Support	9	0b	D1 state is not supported.
D2_Support	10	0b	D2 state is not supported.
PME_Support	15:11	00h	Hardwired to 00h.

PCI Power Management Control And Status – RW- 16 bits – [PCI_Reg:64h]			
Field Name	**Bits**	**Default**	**Description**
Power State (PS)	1:0	00b	This field is used both to determine the current power state of the HBA and to set a new power state. The values are: 00 – D0 state 11 – $D3_{HOT}$ state The D1 and D2 states are not supported. When in the $D3_{HOT}$ state, the configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked.
Reserved	7:2	00h	Reserved
PME Enable (PMEE)	8	0b	Read Only. Hardwired to 0 to indicate PME is disabled
Reserved	14:9		Reserved.
PME Status	15	0b	Read Only. Hardwired to 0 as PME is disabled

Serial ATA Capability Register 0 – R- 32 bits – [PCI_Reg:70h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	12h	Hardwired to 12h to indicate that this pointer is a Serial ATA Capability.
Capability Next Pointer	15:8	A4h	Hardwired to A4h, points to Advance Control capability.
Minor Revision	19:16	0h	Minor revision number of the SATA Capability Pointer implemented.
Major Revision	23:20	1h	Major revision number of the SATA Capability Pointer implemented.
Reserved	31:24	0h	Reserved

This set of registers, when supported, is used for the Index-Data Pair mechanism.

Serial ATA Capability Register 1 – R- 32 bits – [PCI_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**
BAR Location	3:0	1111b	Value 1111b indicates Index-Data pair is implemented in Dwords directly following SATACR1 in the PCI configuration space.
BAR Offset	23:4	000h	Indicates the offset into the BAR where the Index-Data Pair are located in Dword granularity.
Reserved	31:24	0h	Reserved.

Serial ATA Capability Register 1 – R- 32 bits – [PCI_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**

This set of registers, when supported, is used for the Index-Data Pair mechanism.

IDP Index Register – RW- 32 bits – [PCI_Reg:78h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved.
IDP Index	9:2	00h	This register selects the Dword offset of the memory mapped AHCI register to be accessed. The IDP Index should be sized such that it can access the entire ABAR register space for the particular implementation.
Reserved	31:10	000000h	Reserved.

This set of registers, when supported, is used for the Index-Data Pair mechanism.

IDP Data Register – RW- 32 bits – [PCI_Reg:7Ch]			
Field Name	**Bits**	**Default**	**Description**
IDP Data	31:0	F722_FF85h	This register is a "window" through which data is read or written to the memory mapped register pointed to by the IDP Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by IDP Index.

All register accesses to IDP Data are Dword granularity.

Reserved – RW- 16 bits – [PCI_Reg:80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	0h	

Reserved – R/RW- 16 bits – [PCI_Reg:82h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	0h	

PHY Core Control – RW – 32 bits – [PCI_Reg:84h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	8:0	0b	
PHY Fine Tune Target Port	11:9	0h	Write to this field to indicate which port's fine tune settings software will read/write from/to. 0h: Port 0 is selected 1h: Port 1 is selected 2h: Port 2 is selected 3h: Port 3 is selected 4h: Port 4 is selected 5h: Port 5 is selected 6h-7h: Reserved ***Note 1**

PHY Core Control – RW – 32 bits – [PCI_Reg:84h]			
Field Name	**Bits**	**Default**	**Description**
Generation I/II/III	13:12	1h	Write to this field to indicate which Generation Speed software would like the setting to be applied to. 0h: Reserved 1h: Setting is for Gen 1 2h: Setting is for Gen 2 3h: Setting is for Gen 3 ***Note 1**
Write Settings To All 6 Ports	14	0b	Level signal that allows simultaneously writing port-dependent PHY fine-tune settings to all 6 ports (values in offset 0x94). Software does not need to write individual port settings. This signal has NO effect on read and shall be used for write only. 1: Port0-Port5 fine-tune settings will be written at the same time with the same values placed into PHY.PXGX and PHY.PX fields of reg0x94. 0: Port0-Port5 PHY.PXGX and PHY.PX fields will not be changed at the same time and need to be individually entered using PHY.CCNTL.PN. ***Note2**
Reserved	17:15	0h	
Reserved	31:18	1b	

***Note 1**
Software uses these fields to read/write PHY.PXGX (PCI_REG: 0x94). For example, if PHY.PXGX.TX.DRV_STR[2:0] is to be modified for port2/Gen3, then software will exercise the following sequence:
1. Write 0x2 to PHY.CCNTL.PN,
2. Write 0x3 to PHY.CCNTL.GEN
3. Write desired value to PHY.PXGX.TX.DRV_STR[2:0]

***Note 2**
For example, if PHY.PXGX.TX.DRV_STR[2:0] is to be modified for all 6 ports for Gen3, then software will exercise the following sequence:
1. Write 0x3 to PHY.CCNTL.GEN
2. Write 0x1 to PHY.CCNTL.WRALL
3. Write desired value to PHY.PXGX.TX.DRV_STR[2:0]

Reserved- RW- 32 bits - [PCI_Reg:88h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved - RW- 16 bits - [PCI_Reg:8Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	-	

Reserved- RW- 16 bits - [PCI_Reg:8Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	-	

Reserved - RW- 32 bits - [PCI_Reg:90h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Phy Fine Tune PortX GenX Setting - RW- 32 bits - [PCI_Reg:94h]			
Field Name	**Bits**	**Default**	**Description**
Transmitter De-emphasis	7:0	Gen1: 3h Gen2: 3h Gen3: 3h	Tx De-emphasis setting. Unit: dB 00h: 0 02h: 1.58 03h: 2.50 06h: 3.52 07h: 4.68 0Eh: 6.02 0Fh: 7.60 1Eh: 9.54 1Fh: 12.04 Other values: invalid
Transmitter Driving Strength	10:8	Gen1: 2h Gen2: 3h Gen3: 6h	Tx drive strength control. Unit: mVppd 0h: 213 1h: 419 2h: 502 3h: 585 4h: 672 5h: 755 6h: 838 7h: 921
Reserved	11	-	
Transmitter Output Slew Control	15:12	Gen1: 4h Gen2: 1h Gen3: Ah	Tx Output slew control Modifications to this field should be limited to the following only: Gen1 allowable settings: 4h & 7h Gen2 allowable settings: 1h & 3h Gen3 allowable settings: any values between 8h & Fh, inclusively. Setting values other than the ones specified will cause intermitten results. Rise/Fall time is controlled by the combined force of CP_TX_DRV_STR[2:0], CP_TX_SLEW_CNTRL[3:0] and CP_TX_DEEMPH_STR[7:0]. Depending on the channel loss, the value of CP_TX_SLEW_CNTRL[3:0] and CP_TX_DEEMPH_STR[7:0] may have to be adjusted based on package and board design.
Reserved	23:16	-	
Reserved	31:24	-	

Notes:
- The default values are generation speed dependent.
- The entire 0x94h registers are Generation Speed sensitive as well as Per-Port sensitive, that is, they are accessed through PHY.CCNTL.GEN and PHY.CCNTL.PN. This implies that there will be totally 18 sets of registers implemented for this offset internally, from software point-of-view, there will be only 1 set. For example, if software wants to set PHY.PXGX.DEEMPH_STR[7:0] for GEN3, it will first set PHY.CCNTL.GEN to 2'b11, then proceed to writing the 8-bit value into PHY.PXGX.DEEMPH_STR[7:0]. Similarly, if software wants to read the Gen2 value, it will then set PHY.CCNTL.GEN to 2'b10 before reading.

Reserved - RW- 32 bits - [PCI_Reg:98h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved - RW- 32 bits - [PCI_Reg:9Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved - RW- 32 bits - [PCI_Reg:A0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Advanced Features Capability Register0 – R - 32bits - [PCI_Reg:A4h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	13h	The value of 13h in this field identifies the function as being AF capable.
NXT_PTR	15:8	00h	Next pointer. End of list.
Length	23:16	06h	AF Structure Length (Bytes). Returns a value of 06h.
TP_CAP	24	1b	Set to 1b to indicate support for the Transactions Pending (TP) bit (reg0xA8[8]. TP must be supported if FLR is supported.
FLR_CAP	25	1b	Set to 1b to indicate support for Function Level Reset (FLR).
Reserved	31:26	00h	Will be implemented as read only

Advanced Features Capability Register1 – R - 16bits - [PCI_Reg:A8h]			
Field Name	**Bits**	**Default**	**Description**
INITIATE_FLR	0	0b	A write of 1b initiates Function Level Reset (FLR). FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there. The value read by software from this bit is always 0b.
RESERVED	7:1	00h	Reserved. Shall be implemented as read only returning a value of 000 0000b.
TP	8	0b	Transactions Pending (TP): A value of 1b indicates that the Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. A value of 0b indicates that all non-posted transactions have been completed.
Reserved	15:9	00h	Reserved.

Reserved - RW- 16 bits - [PCI_Reg:AAh]			
Field Name	**Bits**	**Default**	Description
Reserved	15:0	-	

Port0 BIST Error Count - R – 32 bits - [PCI_Reg:ACh]			
Field Name	**Bits**	**Default**	**Description**
Port0 BIST Error Count	31:0	0000_0000h	Once FFFFFFFFh is reached, the counter value will stay at that value.

Port0 BIST Control/Status - RW - 16 bits - [PCI_Reg:B0h]			
Field Name	**Bits**	**Default**	**Description**
Port0 Link BIST Enable	0	0b	Once set, Port0 is put into Link BIST mode, overriding normal operation. Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[24] (IOBIST ATE Ports) (indicating Port0) is set, this bit will be set to 1'b1 automatically. Deasserting reg0xEC[3] or reg0xEC[24] will return this field to its original value.
Port0 PRBS10 Error Count Valid	1	0b	Read-Only. Indicates whether Port0 BIST Error Count is valid when Port0 Link BIST Pattern 4'b1000 or 4'b1001 is selected. This field is invalid when all other Link BIST patterns are selected.
Port0 Link BIST Pattern	5:2	0000b	0000: Pseudo-random with ALIGN insertion (when Error Count is used, must choose this pattern). 0001: D10.2 Highest frequency (for Rx eye diagram measurement). 0010: SYNC primitive (for Rx eye diagram measurement). 0011: Lone Bit Pattern (LBP) 0100: Mid Frequency Test Pattern (MFTP) 0101: 20-bit data pattern, programmed at reg0xF0. 0110: Force Far End Retimed Loop Back Mode in HBA. 0111: T-mode Enable. T-mode is defined as "Far end transmit only mode without Device initiating". In T-mode, the BIST pattern that is generated is based on the programming in the BIST Transmit Pattern Registers DW1 (reg0xE4) and DW2 (reg0xE8). 1000: HFTP pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1001: PRBS10 pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1010: Forced Far End Analog Loop Back Mode—HBA does NOT need BIST Activate FIS from device to be able to run in this mode. Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[24] (IOBIST ATE Ports) (indicating Port0) is set, this field is controlled by reg0xEC[4] (IOBIST PRBS10 Or HFTP Transmission), where only 4'b1000 or 4'b1001 will be selected. Deasserting reg0xEC[3] or reg0xEC[24] will return this field to its original value.
Port0 Error Count Reset	6	0b	When set, Port0 BIST Error Count (reg0xAC) and Port0 BIST Done (bit[9]) are reset. This bit needs to be set for 10ms, then cleared. 10ms is to ensure PHY is ready in proper frequency, mode, and round-trip latency.
Port0 BIST Error Count Freeze Mode	7	0b	When set, Port0 BIST Error Count will stop incrementing if Port0 BIST Error Count Hold is set. When reset, Port0 BIST Error Count will stop incrementing if Port0 BIST Done is set. This is to say, when set, BIST will be free running and Port0 BIST Pattern Count will be ignored. This is useful when running overnight to observe the total error count. Note that when this bit is set, the user needs to time the test duration in order to derive BER, since pattern count is already ignored.
Port0 BIST Error Count Hold	8	0b	When set, Port0 BIST Error Count will hold the current value. It won't be increased even on the event of a mis-comparison. When cleared, it has no effect on Port0 BIST Error Count.

Port0 BIST Control/Status - RW - 16 bits - [PCI_Reg:B0h]			
Field Name	**Bits**	**Default**	**Description**
Port0 BIST Done	9	0b	Read Only When set, it means BIST has verified x amount of patterns specified in the BIST pattern count. It will be reset by Port0 BIST Error Count Reset.
Port0 SATA BIST Enable	10	0b	Enable SATA BIST Vendor Mode: for using AR0/BAR2 offset0 (IDE Data Port) to initiate BIST active FIS.
Port0 BIST with disconnect Enable	11	0b	When set and a BIST Activate FIS is received from the device, the HBA will ignore all OOB signaling from the device. The HBA can exit this mode either through a hardware reset or a software initiated COMRESET. **Note:** This bit will not be cleared by a software-initiated COMRESET.
Port0 Link BIST Speed	13:12	00h	PHY Port0 speed control for Link BIST mode. 2'b11 : GENIII 2'b10: GENII 2'b01: GENI 2'b00: GENI Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[24] (IOBIST ATE Ports) (indicating Port0) is set, this field is controlled by reg0xEC[6:5] (IOBIST ATE Gen Speed). Deasserting reg0xEC[3] or reg0xEC[24] will return this field to its original value.
Reserved	15:14	0h	Reserved.

Port1 BIST Error Count - R - 32 bits - [PCI_Reg:B4h]			
Field Name	**Bits**	**Default**	**Description**
Port1 BIST Error Count	31:0	0000h	When FFFFFFFFh is reached, the counter value will stay at this value.

Port1 BIST Control/Status - RW - 16 bits - [PCI_Reg:B8h]			
Field Name	**Bits**	**Default**	**Description**
Port1 Link BIST Enable	0	0b	Once set, Port1 is put into Link BIST mode, overriding normal operation. Note: When reg0xEC[3] (IOBIST Op Mode) is set and 0xEC[25] (IOBIST ATE Ports) (indicating Port1) is set, this bit will be set to 1'b1 automatically. Deasserting reg0xEC[3] or reg0xEC[25] will return this field to its original value.
Port1 PRBS10 Error Count Valid	1	0b	Read-Only. Indicates whether the Port1 BIST Error Count is valid when Port1 Link BIST Pattern 4'b1000 or 4'b1001 is selected. This field is invalid when all other Link BIST patterns are selected.

Port1 BIST Control/Status - RW - 16 bits - [PCI_Reg:B8h]			
Field Name	**Bits**	**Default**	**Description**
Port1 Link BIST Pattern	5:2	0000b	0000: Pseudo-random with ALIGN insertion (when Error Count is used, must choose this pattern). 0001: D10.2 Highest frequency (for Rx eye diagram measurement). 0010: SYNC primitive (for Rx eye diagram measurement). 0011: Lone Bit Pattern (LBP) 0100: Mid Frequency Test Pattern (MFTP) 0101: 20-bit data pattern, programmed at reg0xF0. 0110: Force Far End Retimed Loop Back Mode in HBA. 0111: T-mode Enable. T-mode is defined as "Far end transmit only mode without Device initiating". In T-mode, the BIST pattern that is generated is based on the programming in the BIST Transmit Pattern Registers DW1 (reg0xE4) and DW2 (reg0xE8). 1000: HFTP pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1001: PRBS10 pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1010: Forced Far End Analog Loop Back Mode—HBA does NOT need BIST Activate FIS from device to be able to run in this mode. Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[25] (IOBIST ATE Ports) (indicating Port1) is set, this field is controlled by reg0xEC[4] (IOBIST PRBS10 Or HFTP Transmission), where only 4'b1000 or 4'b1001 will be selected. Deasserting reg0xEC[3] or reg0xEC[25] will return this field to its original value.
Port1 Error Count Reset	6	0b	When set, Port1 BIST Error Count and Port1 BIST Done are reset. This bit needs to be set for 10ms, then cleared. 10ms is to ensure PHY is ready in proper frequency, mode, and round-trip latency.
Port1 BIST Error Count Freeze Mode	7	0b	When set, Port1 BIST Error Count will stop incrementing if Port1 BIST Error Count Hold is set. When reset, Port 1 BIST Error Count will stop incrementing if Port1 BIST Done is set. This is to say, when set, BIST will be free running and BIST pattern count will be ignored. This is useful when running overnight to observe the total Error Count. Note that when this bit is set, the user needs to time the test duration in order to derive BER, since pattern count is already ignored.
Port1 BIST Error Count Hold	8	0b	When set, Port1 BIST Error Count will hold the current value. It won't be increased even on the event of mis-comparison. When clear, it has no effect on Port1 BIST Error Count.
Port1 BIST Done	9	0b	Read Only When set, it means BIST has verified certain amount of patterns specified in the BIST pattern count. It will be reset by Port1 BIST Error Count Reset.
Port1 SATA BIST Enable	10	0b	Enable SATA BIST Vendor Mode: for using AR0/BAR2 offset0 (IDE Data Port) to initiate BIST active FIS.
Port1 BIST with disconnect Enable	11	0b	When set and a BIST Activate FIS is received from the device, the HBA will ignore all OOB signaling from the device. The HBA can exit this mode either through a hardware reset or a software initiated COMRESET. **Note:** This bit will not be cleared by a software initiated COMRESET.

Port1 BIST Control/Status - RW - 16 bits - [PCI_Reg:B8h]			
Field Name	**Bits**	**Default**	**Description**
Port1 Link BIST Speed	13:12	00h	PHY Port1 speed control for Link BIST mode. 2'b11 : GENIII 2'b10: GENII 2'b01: GENI 2'b00: GENI Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[25] (IOBIST ATE Ports) (indicating Port1) is set, this field is controlled by reg0xEC[6:5] (IOBIST ATE Gen Speed). Deasserting reg0xEC[3] or reg0xEC[25] will return this field to its original value.
Reserved	15:14	0h	Reserved.

Port2 BIST Error Count - R - 32 bits - [PCI_Reg:BCh]			
Field Name	**Bits**	**Default**	**Description**
Port2 BIST Error Count	31:0	0000h	When FFFFFFFFh is reached, the counter value will stay at that value.

Port2 BIST Control/Status - RW - 16 bits - [PCI_Reg:C0h]			
Field Name	**Bits**	**Default**	**Description**
Port2 Link BIST Enable	0	0b	Once set, Port2 is put into Link BIST mode, overriding normal operation. Note: When reg0xEC[3] (IOBIST Op Mode) is set and 0xEC[26] (IOBIST ATE Ports) (indicating Port2) is set, this bit will be set to 1'b1 automatically. Deasserting reg0xEC[3] or reg0xEC[26] will return this field to its original value.
Port2 PRBS10 Error Count Valid	1	0b	Read-Only. Indicates whether Port2 BIST Error Count is valid when Port2 Link BIST Pattern 4'b1000 or 4'b1001 is selected. This field is invalid when all other Link BIST patterns are selected.

Port2 BIST Control/Status - RW - 16 bits - [PCI_Reg:C0h]			
Field Name	**Bits**	**Default**	**Description**
Port2 Link BIST pattern	5:2	0000b	0000: Pseudo-random with ALIGN insertion (when Error Count is used, must choose this pattern). 0001: D10.2 Highest frequency (for Rx eye diagram measurement). 0010: SYNC primitive (for Rx eye diagram measurement). 0011: Lone Bit Pattern (LBP) 0100: Mid Frequency Test Pattern (MFTP) 0101: 20-bit data pattern, programmed at PCI_Reg:F0h. 0110: Force Far End Retimed Loop Back Mode in HBA. 0111: T-mode Enable. T-mode is defined as "Far end transmit only mode without Device initiating". In T-mode, the BIST pattern that is generated is based on the programming in the BIST Transmit Pattern Registers DW1 (reg0xE4) and DW2 (reg0xE8). 1000: HFTP pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1001: PRBS10 pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1010: Forced Far End Analog Loop Back Mode—HBA does NOT need BIST Activate FIS from device to be able to run in this mode. Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[26] (IOBIST ATE Ports) (indicating Port2) is set, this field is controlled by reg0xEC[4] (IOBIST PRBS10 Or HFTP Transmission), where only 4'b1000 or 4'b1001 will be selected. Deasserting reg0xEC[3] or reg0xEC[26] will return this field to its original value.
Port2 BIST Error Count Reset	6	0b	When set, BIST Error Count and Port2 BIST Done are reset. This bit needs to be set for 10ms, then cleared. 10ms is to ensure PHY is ready in proper frequency, mode and round trip latency.
Port2 BIST Error Count Freeze Mode	7	0b	When set, Port2 BIST Error Count will stop incrementing if Port2 BIST Error Count Hold is set. When reset, Port2 BIST Error Count will stop incrementing if Port2 BIST Done is set. This is to say, when set, BIST will be free running and BIST pattern count will be ignored. This is useful when running overnight to observe the total Error Count. Note that when this bit is set, the user needs to time the test duration in order to derive BER, since pattern count is already ignored.
Port2 BIST Error Count Hold	8	0b	When set, Port2 BIST Error Count will hold the current value. It won't be increased even on the event of mis-comparison. When clear, it has no effect on Port2 BIST Error Count.
Port2 BIST Done	9	0b	Read Only When set, it means BIST has verified certain amount of patterns specified in the BIST pattern count. It will be reset by BIST Error Count Reset.
Port2 SATA BIST Enable	10	0b	Enable SATA BIST Vendor Mode: for using AR0/BAR2 offset0 (IDE Data Port) to initiate BIST active FIS.
Port2 BIST with disconnect Enable	11	0b	When set and a BIST Activate FIS is received from the device, the HBA will ignore all OOB signaling from the device. The HBA can exit this mode either through a hardware reset or a software initiated COMRESET. **Note:** This bit will not be cleared by a software initiated COMRESET.

Port2 BIST Control/Status - RW - 16 bits - [PCI_Reg:C0h]			
Field Name	**Bits**	**Default**	**Description**
Port2 Link BIST Speed	13:12	00h	PHY Port2 speed control for Link BIST mode. 2'b11 : GENIII 2'b10: GENII 2'b01: GENI 2'b00: GENI Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[25] (IOBIST ATE Ports) (indicating Port2) is set, this field is controlled by reg0xEC[6:5] (IOBIST ATE Gen Speed). Deasserting reg0xEC[3] or reg0xEC[25] will return this field to its original value.
Reserved	15:14	0h	Reserved.

Port3 BIST Error Count - R - 32 bits - [PCI_Reg:C4h]			
Field Name	**Bits**	**Default**	**Description**
Port3 BIST Error Count	31:0	0000h	When FFFFFFFFh is reached, the counter value will stay at that value.

Port3 BIST Control/Status - RW - 16 bits - [PCI_Reg:C8h]			
Field Name	**Bits**	**Default**	**Description**
Port3 Link BIST Enable	0	0b	Once set, Port3 is put into Link BIST mode, overriding normal operation. Note: When reg0xEC[3] (IOBIST Op Mode) is set and 0xEC[26] (IOBIST ATE Ports) (indicating Port3) is set, this bit will be set to 1'b1 automatically. Deasserting reg0xEC[3] or reg0xEC[26] will return this field to its original value.
Port3 PRBS10 Error Count Valid	1	0b	Read-Only. Indicates whether Port3 BIST Error Count is valid when Port 3Link BIST Pattern 4'b1000 or 4'b1001 is selected. This field is invalid when all other Link BIST patterns are selected.

Port3 BIST Control/Status - RW - 16 bits - [PCI_Reg:C8h]			
Field Name	**Bits**	**Default**	**Description**
Port3 Link BIST Pattern	5:2	0000b	0000: Pseudo-random with ALIGN insertion (when Error Count is used, must choose this pattern). 0001: D10.2 Highest frequency (for Rx eye diagram measurement). 0010: SYNC primitive (for Rx eye diagram measurement). 0011: Lone Bit Pattern (LBP) 0100: Mid Frequency Test Pattern (MFTP) 0101: 20-bit data pattern, programmed at reg0xF0. 0110: Force Far End Retimed Loop Back Mode in HBA. 0111: T-mode Enable. T-mode is defined as "Far end transmit only mode without Device initiating". In T-mode, the BIST pattern that is generated is based on the programming in the BIST Transmit Pattern Registers DW1 (reg0xE4) and DW2 (reg0xE8). 1000: HFTP pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1001: PRBS10 pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1010: Forced Far End Analog Loop Back Mode—HBA does NOT need BIST Activate FIS from device to be able to run in this mode. Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[24] (IOBIST ATE Ports) (indicating Port3) is set, this field is controlled by reg0xEC[4] (IOBIST PRBS10 Or HFTP Transmission), where only 4'b1000 or 4'b1001 will be selected. Deasserting reg0xEC[3] or reg0xEC[24] will return this field to its original value.
Port3 BIST Error Count Reset	6	0b	When set, BIST Error Count and Port3 BIST Done are reset. This bit needs to be set for 10ms, then cleared. 10ms is to ensure PHY is ready in proper frequency, mode and round trip latency.
Port3 BIST Error Count Freeze Mode	7	0b	When set, Port3 BIST Error Count will stop incrementing if Port3 BIST Error Count Hold is set. When reset, Port3 BIST Error Count will stop incrementing if Port3 BIST Done is set. This is to say, when set, BIST will be free running and BIST pattern count will be ignored. This is useful when running overnight to observe the total Error Count. Note that when this bit is set, the user needs to time the test duration in order to derive BER, since pattern count is already ignored.
Port3 BIST Error Count Hold	8	0b	When set, Port3 BIST Error Count will hold the current value. It won't be increased even on the event of mis-comparison. When cleared, it has no effect on Port3 BIST Error Counter.
Port3 BIST Done	9	0b	Read Only When set, it means BIST has verified certain amount of patterns specified in the BIST pattern count. It will be reset by BIST Error Count Reset.
Port3 SATA BIST Enable	10	0b	Enable SATA BIST Vendor Mode: for using AR0/BAR2 offset0 (IDE Data Port) to initiate BIST active FIS.
Port3 BIST with disconnect Enable	11	0b	When set and a BIST Activate FIS is received from the device, the HBA will ignore all OOB signaling from the device. The HBA can exit this mode either through a hardware reset or a software initiated COMRESET. **Note:** This bit will not be cleared by a software initiated COMRESET.

Port3 BIST Control/Status - RW - 16 bits - [PCI_Reg:C8h]			
Field Name	**Bits**	**Default**	**Description**
Port3 Link BIST Speed	13:12	00h	PHY Port3 speed control for Link BIST mode. 2'b11 : GENIII 2'b10: GENII 2'b01: GENI 2'b00: GENI Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[25] (IOBIST ATE Ports) (indicating Port3) is set, this field is controlled by reg0xEC[6:5] (IOBIST ATE Gen Speed). Deasserting reg0xEC[3] or reg0xEC[25] will return this field to its original value.
Reserved	15:14	0h	Reserved.

Port4 BIST Error Count - R - 32 bits - [PCI_Reg:CCh]			
Field Name	**Bits**	**Default**	**Description**
Port4 BIST Error Count	31:0	0000h	When FFFFFFFFh is reached, the counter value will stay at this value.

Port4 BIST Control/Status - RW - 16 bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
Port4 Link BIST Enable	0	0b	Once set, Port4 is put into Link BIST mode, overriding normal operation. Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[28] (IOBIST ATE Ports) (indicating Port4) is set, this bit will be set to 1'b1 automatically. Deasserting reg0xEC[3] or reg0xEC[28] will return this field to its original value.
Port4 PRBS10 Error Count Valid	1	0b	Read-Only. Indicates whether the Port4 BIST Error Count is valid when Port4 Link BIST Pattern 4'b1000 or 4'b1001 is selected. This field is invalid when all other Link BIST patterns are selected.

Port4 BIST Control/Status - RW - 16 bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
Port4 Link BIST pattern	5:2	0000b	0000: Pseudo-random with ALIGN insertion (when Error Count is used, must choose this pattern). 0001: D10.2 Highest frequency (for Rx eye diagram measurement). 0010: SYNC primitive (for Rx eye diagram measurement). 0011: Lone Bit Pattern (LBP) 0100: Mid Frequency Test Pattern (MFTP) 0101: 20-bit data pattern, programmed at reg0xF0. 0110: Force Far End Retimed Loop Back Mode in HBA. 0111: T-mode Enable. T-mode is defined as "Far end transmit only mode without Device initiating". In T-mode, the BIST pattern that is generated is based on the programming in the BIST Transmit Pattern Registers DW1 (reg0xE4) and DW2 (reg0xE8). 1000: HFTP pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1001: PRBS10 pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1010: Forced Far End Analog Loop Back Mode—HBA does NOT need BIST Activate FIS from device to be able to run in this mode. Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[24] (IOBIST ATE Ports) (indicating Port4) is set, this field is controlled by reg0xEC[4] (IOBIST PRBS10 Or HFTP Transmission), where only 4'b1000 or 4'b1001 will be selected. Deasserting reg0xEC[3] or reg0xEC[24] will return this field to its original value.
Port4 BIST Error Count Reset	6	0b	When set, Port4 BIST Error Count and Port4 BIST Done are reset. This bit needs to be set for 10ms, then cleared. 10ms is to ensure PHY is ready in proper frequency, mode and round trip latency.
Port4 BIST Error Count Freeze Mode	7	0b	When set, Port4 BIST Error Count will stop incrementing if Port4 BIST Error Count Hold is set. When reset, Port4 BIST Error Count will stop incrementing if Port4 BIST Done is set. This is to say, when set, BIST will be free running and BIST pattern count will be ignored. This is useful when running overnight to observe the total Error Count. Note that when this bit is set, the user needs to time the test duration in order to derive BER, since pattern count is already ignored.
Port4 BIST Error Count Hold	8	0b	When set, Port4 BIST Error Count will hold the current value. It won't be increased even on the event of mis-comparison. When clear, it has no effect on Port4 BIST Error Count.
Port4 BIST Done	9	0b	Read Only When set, it means BIST has verified certain amount of patterns specified in the BIST pattern count. It will be reset by BIST Error Count Reset.
Port4 SATA BIST Enable	10	0b	Enable SATA BIST Vendor Mode: for using AR0/BAR2 offset0 (IDE Data Port) to initiate BIST active FIS.
Port4 BIST with disconnect Enable	11	0b	When set and a BIST Activate FIS is received from the device, the HBA will ignore all OOB signaling from the device. The HBA can exit this mode either through a hardware reset or a software initiated COMRESET. **Note:** This bit will not be cleared by a software initiated COMRESET.

Port4 BIST Control/Status - RW - 16 bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
Port4 Link BIST Speed	13:12	00h	PHY Port4 speed control for Link BIST mode. 2'b11 : GENIII 2'b10: GENII 2'b01: GENI 2'b00: GENI Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[25] (IOBIST ATE Ports) (indicating Port4) is set, this field is controlled by reg0xEC[6:5] (IOBIST ATE Gen Speed). Deasserting reg0xEC[3] or reg0xEC[25] will return this field to its original value.
Reserved	15:14	0h	Reserved.

Port5 BIST Error Count - R - 32 bits - [PCI_Reg:D4h]			
Field Name	**Bits**	**Default**	**Description**
Port5 BIST Error Count	31:0	0000h	When FFFFFFFFh is reached, the counter value will stay at that value.

Port5 BIST Control/Status - RW - 16 bits - [PCI_Reg:D8h]			
Field Name	**Bits**	**Default**	**Description**
Port5 Link BIST Enable	0	0b	Once set, Port5 is put into Link BIST mode, overriding normal operation. Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[28] (IOBIST ATE Ports) (indicating Port5) is set, this bit will be set to 1'b1 automatically. Deasserting reg0xEC[3] or reg0xEC[28] will return this field to its original value.
Port5 PRBS10 Error Count Valid	1	0b	Read-Only. Indicates whether Port5 BIST Error Count is valid when Port5 BIST Pattern 4'b1000 or 4'b1001 is selected. This field is invalid when all other Link BIST patterns are selected.

Port5 BIST Control/Status - RW - 16 bits - [PCI_Reg:D8h]			
Field Name	**Bits**	**Default**	**Description**
Port5 Link BIST pattern	5:2	0000b	0000: Pseudo-random with ALIGN insertion (when Error Count is used, must choose this pattern). 0001: D10.2 Highest frequency (for Rx eye diagram measurement). 0010: SYNC primitive (for Rx eye diagram measurement). 0011: Lone Bit Pattern (LBP) 0100: Mid Frequency Test Pattern (MFTP) 0101: 20-bit data pattern, programmed at reg0xF0. 0110: Force Far End Retimed Loop Back Mode in HBA. 0111: T-mode Enable. T-mode is defined as "Far end transmit only mode without Device initiating". In T-mode, the BIST pattern that is generated is based on the programming in the BIST Transmit Pattern Registers DW1 (reg0xE4) and DW2 (reg0xE8). 1000: HFTP pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1001: PRBS10 pattern directly at the PHY-CORE interface without going through 8b/10b encoding. 1010: Forced Far End Analog Loop Back Mode—HBA does NOT need BIST Activate FIS from device to be able to run in this mode. Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[24] (IOBIST ATE Ports) (indicating Port5) is set, this field is controlled by reg0xEC[4] (IOBIST PRBS10 Or HFTP Transmission), where only 4'b1000 or 4'b1001 will be selected. Deasserting reg0xEC[3] or reg0xEC[24] will return this field to its original value.
Port5 BIST Error Count Reset	6	0b	When set, Port5 BIST Error Count and Port5 BIST Done are reset. This bit needs to be set for 10ms, then cleared. 10ms is to ensure PHY is ready in proper frequency, mode and round trip latency.
Port5 BIST Error Count Freeze Mode	7	0b	When set, Port5 BIST Error Count will stop incrementing if Port5 BIST Error Count Hold is set. When reset, Port5 BIST Error Count will stop incrementing if Port5 BIST Done is set. This is to say, when set, BIST will be free running and BIST pattern count will be ignored. This is useful when running overnight to observe the total Error Count. Note that when this bit is set, the user needs to time the test duration in order to derive BER, since pattern count is already ignored.
Port5 BIST Error Count Hold	8	0b	When set, the BIST error counter will hold the current value. It won't be increased even on the event of mis-comparison. When clear, it has no effect on Port5 BIST Error Count.
Port5 BIST Done	9	0b	Read Only When set, it means BIST has verified certain amount of patterns specified in the BIST pattern count. It will be reset by Port5 BIST Error Count Reset.
Port5 SATA BIST Enable	10	0b	Enable SATA BIST Vendor Mode: for using AR0/BAR2 offset0 (IDE Data Port) to initiate BIST active FIS.
Port5 BIST with disconnect Enable	11	0b	When set and a BIST Activate FIS is received from the device, the HBA will ignore all OOB signaling from the device. The HBA can exit this mode either through a hardware reset or a software initiated COMRESET. **Note:** This bit will not be cleared by a software initiated COMRESET.

Port5 BIST Control/Status - RW - 16 bits - [PCI_Reg:D8h]			
Field Name	**Bits**	**Default**	**Description**
Port5 Link BIST Speed	13:12	00h	PHY Port5 speed control for Link BIST mode. 2'b11 : GENIII 2'b10: GENII 2'b01: GENI 2'b00: GENI Note: When reg0xEC[3] (IOBIST Op Mode) is set and reg0xEC[25] (IOBIST ATE Ports) (indicating Port5) is set, this field is controlled by reg0xEC[6:5] (IOBIST ATE Gen Speed). Deasserting reg0xEC[3] or reg0xEC[25] will return this field to its original value.
Reserved	15:14	0h	Reserved.

BIST Pattern Count - RW - 32 bits - [PCI_Reg:DCh]			
Field Name	**Bits**	**Default**	**Description**
BIST Pattern Count	31:0	0000_2000h	This count specifies how many Octal WORD patterns need to be checked before Portx (x is 0 to 5) BIST Done bit is set. This count value is used for all the 6 ports. The default value of 400h would be used for tester, which means 32K DWORD pattern would be compared for BIST test. Value of "0000_0000"h means the maximum patterns (16,000, 000, 000) checked. This register is used for both SATA BIST and Link BIST. The maximum amount of patterns that can be transferred before Done bit asserts is 0x1_0000_0000h Dword x 4 x 40 bits = 6.87 x 10^11 bits. This is not enough to effectively measure a complete BER of 10 ^ -12. When IOBIST is in BER non-free-running mode, this pattern count will be doubled. That is, it specifies how many DOWords (1 DOWord = Double Octuple Word = 16 Dwords) need to be transmitted before Done bit is set. For example, a value of 0x0000_2000 will suggest 180,224 Dwords to be transmitted.

PCI Target Control TimeOut- RW - 16 bits - [PCI_Reg:E0h]			
Field Name	**Bits**	**Default**	**Description**
PCI Target Control TimeOut Count	7:0	80h	This register is used for programming the PCI Target Control TimeOut Count used to clear any stale target commands to the hosts controller. Granularity is 15.5us (Count * 15.5 us) The counter will be disabled if the count is programmed to 0x0.
Reserved	15:8	00h	Reserved.

Reserved - RW- 16 bits - [PCI_Reg:E2h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	-	

T-Mode BIST Transit Pattern DW1 - RW - 32 bits - [PCI_Reg:E4h]			
Field Name	**Bits**	**Default**	**Description**
T-mode BIST Transit Pattern DW1	31:0	0000_0000h	Transit Pattern DW1

T-Mode BIST Transit Pattern DW2 - RW - 32 bits - [PCI_Reg:E8h]			
Field Name	**Bits**	**Default**	**Description**
T-mode BIST Transit Pattern DW2	31:0	0000_0000h	Transit Pattern DW2

BIST Control- RW – 16 bits – [PCI_Reg:ECh]			
Field Name	**Bits**	**Default**	**Description**
T-mode A bit	0	0b	ALIGN primitives bypass mode
T-mode S bit	1	0b	Scrambling Bypass.
T-mode P bit	2	0b	The transmit primitives bit.
Reserved	31:3	-	

20-BIT BIST Transit Pattern - RW - 32 bits - [PCI_Reg:F0h]			
Field Name	**Bits**	**Default**	**Description**
20-BIT BIST Transit Pattern	19:0	0000_0000h	20-bit Transit Data Pattern without going through 8b/10b encode.
Reserved	31:20	0h	Reserved.

2.1.2 SATA I/O Registers for IDE Mode

2.1.2.1 BAR0/BAR2/BAR1/BAR3 Registers

BAR0/BAR2 uses 8 bytes of I/O space. BAR0 is used for Primary channel and BAR2 is used for Secondary channel during IDE native mode. BAR1/BAR3 uses 2 bytes of I/O space. BAR1 is used for Primary channel and BAR3 is used for Secondary channel during IDE native mode.

Address (hex)			**Name and Function**	
Compatibility Mode		**Native Mode (Offset)**	**Read Function**	**Write Function**
IDE Command Block Registers				
Primary	**Secondary**	**BAR0/BAR2**		
1F0	170	(Primary or Secondary) Base Address 0 + 0	Data (16 bit)	Data (16 bit)
1F1	171	(Primary or Secondary) Base Address 0 + 1	Error register	Features register
1F2	172	(Primary or Secondary) Base Address 0 + 2	Sector Count	Sector Count
1F3	173	(Primary or Secondary) Base Address + 3	Sector Number	Sector Number
1F4	174	(Primary or Secondary) Base Address + 4	Cylinder Low	Cylinder Low

Address (hex)			Name and Function	
Compatibility Mode		**Native Mode (Offset)**	**Read Function**	**Write Function**
1F5	175	(Primary or Secondary) Base Address + 5	Cylinder High	Cylinder High
1F6	176	(Primary or Secondary) Base Address + 6	Drive/Head	Drive/Head
1F7	177	(Primary or Secondary) Base Address + 7	Status	Command
IDE Control Block Registers				
Primary	**Secondary**	**BAR1/BAR3**		
3F6	376	(Primary or Secondary) Base Address + 2	Alternate Status	Device Control

2.1.2.2 BAR4 Registers

BAR4 uses 16 bytes of I/O space. The Bus-master interface base address register (BAR4) defines the base address of the IO spare.

Register Name	Offset Address [Primary/Secondary]
Bus-master IDE Command	00h/08h
Bus-master IDE Status	02h/0Ah
Descriptor Table Pointer	04h/0Ch

Bus-master IDE Command - RW- 8 bits - [IO_Reg: BAR4 + 00/08h]			
Field Name	**Bits**	**Default**	**Description**
Bus Master IDE Start/Stop	0	0b	Bus Master IDE Start (1)/Stop (0). This bit will not be reset by interrupt from IDE device. This must be reset by soft ware (device driver).
Reserved	2:1		Reserved.
Bus Master Read/Write	3	0b	Bus Master IDE r/w (direction) control 0: Memory -> IDE 1: IDE -> Memory This bit should not change during Bus Master transfer cycle, even if terminated by Bus Master IDE Stop.
Reserved	7:4	0h	Reserved.

Bus-master IDE Status - RW- 8 bits - [IO_Reg: BAR4 + 02/0Ah]			
Field Name	**Bits**	**Default**	**Description**
Bus Master Active	0	0b	Bus Master IDE active. This bit is set to 1 when bit[0] in the Bus Master IDE command address register is set to 1. The IDE host controller sets this bit to 0 when the last transfer for a region is performed. This bit is also set to 0 when bit 0 of the Bus Master IDE command register is set to 0.
Bus Master DMA Error	1	0b	IDE DMA error. This bit is set when the IDE host controller encounters a target abort, master abort, or parity error while transferring data on the PCI bus. Writing a 1 clears this bit.

Bus-master IDE Status - RW- 8 bits - [IO_Reg: BAR4 + 02/0Ah]			
Field Name	**Bits**	**Default**	**Description**
IDE Interrupt	2	0b	IDE Interrupt. Indicates when an IDE device has asserted its interrupt line. IRQ14 is used for the primary channel, and IRQ15 is used for the secondary channel. If the Interrupt Status bit is set to 0, by writing a 1 to this bit while the interrupt line is still at the active level, this bit will remain 0 until another assertion edge is detected on the interrupt line.
Reserved	4:3		Reserved.
Master Device DMA Capable	5	0b	Device 0 (Master) DMA capable.
Slave Device DMA Capable	6	0b	Device 1 (Slave) DMA capable.
Simplex Only	7	0b	Read Only. Simplex only. This bit is hard-wired to 0.

Descriptor Table Pointer - RW- 32 bits - [IO_Reg: BAR4 + 04/0Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved.
Descriptor Table Base Address	31:2	0000_0000h	Base Address of Descriptor Table. These bits correspond to Address [31-02].

2.1.3 SATA Memory Mapped Registers for AHCI Mode

2.1.3.1 BAR5 Registers

These are the AHCI memory mapped registers, the base address is defined through ABAR (BAR5) register.

Register Name	Offset Address
Generic Host Control	00h-2Bh
Reserved	2Ch-9Fh
Vendor Specific registers	A0h-FFh
Port 0 port control registers	100h-17Fh
Port 1 port control registers	180h-1FFh
Port 2 port control registers	200h-27Fh
Port 3 port control registers	280h-2FFh
Port 4 port control registers	300h-37Fh
Port 5 port control registers	380h-3FFh

2.1.3.2 Generic Host Control

The following registers apply to the entire HBA.

Register Name	Offset Address
Host Capabilities (CAP)	00h-03h
Global Host Control (GHC)	04h-07h
Interrupt Status (IS)	08h-0Bh
Ports Implemented (PI)	0Ch-0Fh
Version (VS)	10h-13h
Command Completion Coalescing Control (CCC_CTL)	14h-17h
Command Completion Coalescing Ports (CCC_PORTS)	18h-1Bh

Register Name	Offset Address
Enclosure Management Location (EM_LOC)	1Ch-1Fh
Enclosure Management Control (EM_CTL)	20h-23h
CAP2 (HBA Capabilities Extended)	24-27h
BIOS/OS Handoff Control and Status (BOHC)	28-2Bh
Vendor Specific	A0h-FFh

HBA Capabilities – R - 32bits [Mem_reg: ABAR + 00h]			
Field Name	**Bits**	**Default**	**Description**
Number of Ports	4:0	00101b	0's based value indicating the maximum number of ports supported by the HBA silicon. A maximum of 32 ports can be supported. A value of 0h, indicating one port, is the minimum requirement. Note that the number of ports indicated in this field may be more than the number of ports indicated in the GHC.PI register. The default value of this register is 4 ports since the HBA is in IDE mode after power-on reset. This register is writable when reg0x40[0] (Subclass Code Write Enable) is set.
Supports External SATA (SXS)	5	0b	1: Indicates that the HBA has one or more Serial ATA ports that have a signal-only connector (i.e. power is not part of that connector) that is externally accessible. If this bit is set to 1, software may refer to the PxCMD.ESP bit to determine whether a specific port has its signal connector externally accessible as a signal-only connector. 0: Indicates that the HBA has no Serial ATA ports that have a signal-only connector externally accessible.
Enclosure Management Supported (EMS)	6	0b	1: Indicates that the HBA supports enclosure management. When enclosure management is supported, the HBA has implemented the EM_LOC and EM_CTL global HBA registers. 0: Indicates that the HBA does not support enclosure management and the EM_LOC and EM_CTL global HBA registers are not implemented.
Command Completion Coalescing Supported (CCCS)	7	1b	1: Indicates that the HBA supports command completion coalescing. When command completion coalescing is supported, the HBA has implemented the CCC_CTL and the CCC_PORTS global HBA registers. 0: Indicates that the HBA does not support command completion coalescing and the CCC_CTL and CCC_PORTS global HBA registers are not implemented.
Number of Command Slots (NCS)	12:8	11111b	0's based value indicate the number of command slots per port supported by this HBA. A minimum of 1 and a maximum of 32 slots per port can be supported. The same number of command slots is available on each implemented port.
Partial State Capable (PSC):	13	1b	Indicates whether the HBA can support transitions to the Partial state. 0: Software must not allow the HBA to initiate transitions to the Partial state via aggressive link power management nor the PxCMD.ICC field in each port, and the PxSCTL.IPM field in each port must be programmed to disallow device initiated Partial requests. 1: HBA and device initiated Partial requests can be supported.

HBA Capabilities – R - 32bits [Mem_reg: ABAR + 00h]			
Field Name	**Bits**	**Default**	**Description**
Slumber State Capable (SSC):	14	1b	Indicates whether the HBA can support transitions to the Slumber state. 0: Software must not allow the HBA to initiate transitions to the Slumber state via aggressive link power management nor the PxCMD.ICC field in each port, and the PxSCTL.IPM field in each port must be programmed to disallow device initiated Slumber requests. 1: HBA and device initiated Slumber requests can be supported.
PIO Multiple DRQ Block (PMD)	15	1b	0: HBA only supports single DRQ block data transfers for the PIO command protocol. 1: HBA supports multiple DRQ block data transfers for the PIO command protocol. 0
FIS-based Switching Supported (FBSS)	16	0b	1: Indicates HBA supports Port Multiplier FIS-based switching. 0: Indicates HBA does not support FIS-based switching. AHCI 1.0 and 1.1 HBAs will have this bit cleared to 0.
Supports Port Multiplier (SPM)	17	1b	Indicates whether HBA can support a port multiplier. When set, a port multiplier using command-based switching is supported. When cleared to 0, a port multiplier is not supported, and a port multiplier may not be attached to this HBA.
Supports AHCI mode only (SAM)	18	0b	The SATA controller may optionally support AHCI access mechanisms only. 0: Indicates that in addition to the native AHCI mechanism (via ABAR), the SATA controller implements a legacy, task-file based register interface such as SFF-8038i. 1: Indicates the SATA controller does not implement a legacy, task-file based register interface.
Supports Non-Zero DMA Offsets (SNZO)	19	0b	1: Indicates HBA can support non-zero DMA offsets for DMA Setup FISes. This bit is reserved for future AHCI enhancements. AHCI 1.0 and 1.1 HBAs will have this bit cleared to 0.
Interface Speed Support (ISS)	23:20	3h	Indicates the maximum speed HBA can support on its ports. These encodings match the system software programmable PxSCTL.DET.SPD field. Values are: **Bits** **Definition** 0000 Reserved 0001 Gen 1 (1.5 Gbps) 0010 Gen 1 (1.5 Gbps) and Gen 2 (3 Gbps) 0011 Gen1 (1.5 Gbps) and Gen 2 (3 Gbps) and Gen 3 (6 Gbps) *0011 - 1111 Reserved*
Supports Command List Override (SCLO)	24	1b	1: HBA supports the PxCMD.CLO bit and its associated function. 0: HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.
Supports Activity LED (SAL)	25	1b	1: HBA supports a single activity indication output pin. This pin can be connected to an LED on the platform to indicate device activity on any drive. 0: This function is not supported.

HBA Capabilities – R - 32bits [Mem_reg: ABAR + 00h]			
Field Name	**Bits**	**Default**	**Description**
Supports Aggressive Link Power Management (SALP)	26	1b	1: HBA can support auto-generating link requests to the Partial or Slumber states when there are no commands to process. 0: This function is not supported and software will treat the PxCMD.ALPE and PxCMD.ASP bits as reserved.
Supports Staggered Spin-up (SSS)	27	0b	1: HBA supports staggered spin-up on its ports, for use in balancing power spikes. 0: This function is not supported. This value is loaded by the BIOS prior to OS initialization.
Supports Mechanical Presence Switch (SMPS)	28	1b	1: HBA supports mechanical presence switches on its ports for use in hot plug operations. 0; This function is not supported. This value is loaded by the BIOS prior to OS initialization.
Supports SNotification Register (SSNTF)	29	1b	1: HBA supports the PxSNTF (SNotification) register and its associated functionality. 0: HBA does not support the PxSNTF (SNotification) register and its associated functionality.
Supports Native Command Queuing (SNCQ)	30	1b	Indicates whether HBA supports Serial ATA native command queuing. 1: HBA can handle DMA Setup FISes natively, and can handle the auto-activate optimization through that FIS. 0: Native command queuing is not supported and software should not issue any native command queuing commands.
Supports 64-bit Addressing (S64A)	31	1b	Indicates whether HBA can access 64-bit data structures. 1: HBA will make the 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry read/write. 0: These bits are read-only and treated as 0s by the HBA.

This register indicates basic capabilities of the HBA to driver software.

Global HBA Control – RW - 32bits [Mem_reg: ABAR + 04h]			
Field Name	**Bits**	**Default**	**Description**
HBA Reset (HR)	0	0b	When set by software, this bit causes an internal reset of the HBA. All state machines that relate to data transfers and queuing shall return to an idle condition, and all ports shall be re-initialized via COMRESET (if staggered spin-up is not supported). If staggered spin-up is supported, then it is the responsibility of software to spin-up each port after the reset has completed. When the HBA has performed the reset action, it shall reset this bit to 0. A software write of 0 shall have no effect.
Interrupt Enable (IE)	1	0b	This global bit enables interrupts from the HBA. When cleared (reset default), all interrupt sources from all ports are disabled. When set, interrupts are enabled.

Global HBA Control – RW - 32bits [Mem_reg: ABAR + 04h]			
Field Name	**Bits**	**Default**	**Description**
MSI Revert to Single Message (MRSM)	2	0b	When set to 1by hardware, indicates that HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, HBA has not reverted to single MSI mode (i.e., hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: • MC.MSIE = 1 (MSI is enabled) • MC.MMC > 0 (multiple messages requested) • MC.MME > 0 (more than one message allocated) • MC.MME != MC.MMC (messages allocated not equal to number requested) When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, hardware has been programmed to use single MSI mode, and is not "reverting" to that mode. Read Only
Reserved	30:3	00000000h	Reserved.
AHCI Enable (AE)	31	0b	When set, indicates that communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. When set, software shall only communicate with the HBA using AHCI. When cleared, software shall only communicate with the HBA using legacy mechanisms. When cleared, FISes are not posted to memory, and no commands are sent via AHCI mechanisms. Software shall set this bit to 1 before accessing other AHCI registers.

This register controls various global actions of the HBA.

Interrupt Status - RW -32 bits [Mem_reg: ABAR + 08h]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pending Status (IPS)	31:0	0h	If set, indicates that the corresponding port has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. The IPS[x] bit is only defined for ports that are implemented or for the command completion coalescing interrupt defined by CCC_CTL.INT. All other bits are reserved. Writing a 1 clear these bits.

This register indicates which of the ports within the controller have an interrupt pending and require service.

Ports Implemented - R -32 bits [Mem_reg: ABAR + 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Port Implemented (PI)	31:0	0000000Fh	This register is bit significant. If a bit is set to 1, the corresponding port is available for software to use. If a bit is cleared to 0, the port is not available for software to use. The maximum number of bits set to 1 shall not exceed CAP.NP + 1, although the number of bits set in this register may be fewer than CAP.NP + 1. At least one bit should be set to 1.

This register indicates which ports are exposed by the HBA. It is loaded by the BIOS. It indicates which ports that the HBA supports are available for software to use. For example, on an HBA that supports 6 ports as indicated in CAP.NP, only ports 1 and 3 could be available, with ports 0, 2, 4, and 5 being unavailable. Software must not read or write to registers within unavailable ports.

AHCI Version- R – 32 bits [Mem_reg: ABAR + 10h]			
Field Name	**Bits**	**Default**	**Description**
Minor Version Number (MNR)	15:0	0200h	Indicates the minor version is “10”.
Major Version Number (MJR)	31:16	0001h	Indicates the major version is “1”.

Command Completion Coalescing Control (CCC_CTL) - RW – 32bits [Mem_reg: ABAR + 14h]			
Field Name	**Bits**	**Default**	**Description**
CCC_CTL Enable	0	0h	When cleared to 0, the command completion coalescing feature is disabled and no CCC interrupts are generated. When set to 1, the command completion coalescing feature is enabled and CCC interrupts may be generated based on timeout or command completion conditions. Software shall only change the contents of the TV and CC fields when this bit is cleared to 0. On transition of this bit from 0 to 1, any updated values for the TV and CC fields shall take effect.
Reserved	2:1	0h	Reserved
CCC Interrupt (INT)	7:3	1Fh	Read Only. Specifies the interrupt used by the CCC feature. This interrupt must be marked as unused in the Ports Implemented register (ABAR + 0Ch) by having the corresponding bit being set to 0. Thus, the CCC interrupt corresponds to the interrupt for an unimplemented port on the controller. When a CCC interrupt occurs, the corresponding bit of ABAR + 08h [31:0] (Interrupt Status. Interrupt Pending Status) shall be asserted to 1. This field also specifies the interrupt vector used for MSI.
Command Completions (CC)	15:8	01h	Specifies the number of command completions that are necessary to cause a CCC interrupt. The HBA has an internal command completion counter, hCccComplete. hCccComplete is incremented by one each time a selected port has a command completion. When hCccComplete is equal to the command completions value, a CCC interrupt is signaled. The internal command completion counter is reset to 0 on the assertion of each CCC interrupt. A value of 0 for this field shall disable CCC interrupts being generated based on the number of commands completed, i.e. CCC interrupts are only generated based on the timer in this case.

Command Completion Coalescing Control (CCC_CTL) - RW – 32bits [Mem_reg: ABAR + 14h]			
Field Name	**Bits**	**Default**	**Description**
Timeout Value (TV)	31:16	0001h	The timeout value is specified in 1 millisecond intervals. The timer accuracy shall be within 5%. hCccTimer is loaded with this timeout value. hCccTimer is only decremented when commands are outstanding on selected ports. The HBA will signal a CCC interrupt when hCccTimer has decremented to 0. hCccTimer is reset to the timeout value on the assertion of each CCC interrupt. A timeout value of 0 is reserved.

The register is used to configure the command completion coalescing feature for the entire HBA.
Implementation Note: HBA state variables (examples include hCccComplete and hCccTimer) are used to describe the required externally visible behavior. Implementations are not required to have internal state values that directly correspond to these variables.

Command Completion Coalescing Ports - RW – 32bits [Mem_reg: ABAR + 18h]			
Field Name	**Bits**	**Default**	**Description**
Ports (PRT)	31:0	00000000h	This register is bit significant. Each bit corresponds to a particular port, where bit 0 corresponds to port 0. If a bit is set to 1, the corresponding port is part of the command completion coalescing feature. If a bit is cleared to 0, the port is not part of the command completion coalescing feature. Bits set to 1 in this register must also have the corresponding bit set to 1 in the Ports Implemented register (ABAR + 0Ch). An updated value for this field shall take effect within one timer increment (1 millisecond).

The command completion coalescing ports register is used to specify the ports that are coalesced as part of the CCC feature when CCC_CTL.EN = '1'.

Registers at offsets A0h to FFh are vendor specific.

CAP2(HBA Capabilities Extended) – R - 32 bits – [Offset: 24h]			
Field Name	**Bits**	**Default**	**Description**
BIOS/OS Handoff(BOH)	0	0b	When set to 1, the HBA supports the BIOS/OS handoff mechanism. When cleared to 0, the HBA does not support the BIOS/OS handoff mechanism. When BIOS/OS handoff is supported, the HBA has implemented the BOHC global HBA register (Offset:28h). When cleared to 0, it indicates that the HBA does not support BIOS/OS handoff and the BOHC global HBA register is not implemented.
Reserved	31:1	0000h	Reserved. Read Only

This register indicates capabilities of the HBA to driver software.

BIOS/OS Handoff Control and Status - RW - 32 bits - [Offset:28h]			
Field Name	**Bits**	**Default**	**Description**
BIOS Owned Semaphore(BOS)	0	0b	The BIOS sets this bit to establish ownership of the HBA controller. BIOS will clear this bit in response to a request for ownership of the HBA by system software via OOS.
OS Owned Semaphore(OOS)	1	0b	The system software sets this bit to request ownership of the HBA controller. Ownership is obtained when this bit reads 1 and the BOS bit reads 0.
SMI on OS Ownership Change Enable(SOOE)	2	0b	This bit, when set to 1, enables an SMI when the OOC bit has been set to 1.

BIOS/OS Handoff Control and Status - RW - 32 bits - [Offset:28h]			
Field Name	**Bits**	**Default**	**Description**
OS Ownership Change(OOC)	3	0b	This bit is set to 1 when the OOS bit transitions from 0 to 1. This bit is cleared by writing a 1 to it. Writing 0 has no effect on it.
BIOS Busy(BB)	4	0b	This bit is used by the BIOS to indicate that it is busy cleaning up for ownership change.
Reserved	31:05	00000000h	Reserved. Read Only

This register controls various global actions of the HBA. **This register is not affected by an HBA reset.**

2.1.3.3 Port Registers (One Set Per Port)

The following registers describe the registers necessary to implement port 0. Additional ports shall have the same register mapping. Port 1 starts at 180h, port 2 starts at 200h, port 3 at 280h, etc. The algorithm for software to determine the offset is as follows:

- Port offset = 100h + (PI Asserted Bit Position * 80h)

Register Name	Offset Address
Port-N Command List Base Address(PNCLB)	00h-03h + Port offset
Port-N Command List Base Address Upper 32-Bits(PNCLBU)	04h-07h + Port offset
Port-N FIS Base Address(PNFB)	08h-0Bh + Port offset
Port-N FIS Base Address Upper 32-Bits(PNFBU)	0Ch-0Fh + Port offset
Port-N Interrupt Status(PNIS)	10h-13h + Port offset
Port-N Interrupt Enable(PNIE)	14h-17h + Port offset
Port-N Command and Status(PNCMD)	18h-1Bh + Port offset
Reserved	1Ch-1Fh + Port offset
Port-N Task File Data(PNTFD)	20h-23h + Port offset
Port-N Signature(PNSIG)	24h-27h + Port offset
Port-N Serial ATA Status (PNSSTS)	28h-2Bh + Port offset
Port-N Serial ATA Control (PNSCTL)	2Ch-2Fh + Port offset
Port-N Serial ATA Error (PNSERR)	30h-33h + Port offset
Port-N Serial ATA Active (PNSACT)	34h-37h + Port offset
Port-N Command Issue(PNCI)	38h-3Bh + Port offset
Port-N SNotification (PNSNTF)	3Ch-3Fh + Port offset
Reserved for FIS-based Switching Definition	40h-43h + Port offset
Reserved	44h-6Fh + Port offset
Port-N Vendor Specific(PNVS)	70h-7Fh + Port offset

*N is the port number, 0 ~ 5

Port-N Command List Base Address -RW -32 bits [Mem_reg: ABAR + port offset + 00h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	9:0	000h	Reserved.
Command List Base Address (CLB)	31:10	000000h	Indicates the 32-bit base physical address for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1K-bytes in length. This address must be 1K-byte aligned as indicated by bits 09:00 being read only.

Port-N Command List Base Upper Address -RW - 32 bits [Mem_reg: ABAR + port offset + 04h]			
Field Name	**Bits**	**Default**	**Description**
Command List Base Address Upper (CLBU)	31:0	00000000h	Indicates the upper 32-bits for the command list base physical address for this port. This base is used when fetching commands to execute. This register shall read only 0 for HBAs that do not support 64-bit addressing.

Port–N FIS Base Address -RW -32 bits [Mem_reg: ABAR + port offset + 08h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	00h	Reserved.
FIS Base Address (FB):	31:8	0h	Indicates the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256-byte aligned as indicated by bits 07:00 being read only.

Port-N FIS Base Address Upper –RW – 32 bits [Mem_reg: ABAR + port offset + 0Ch]			
Field Name	**Bits**	**Default**	**Description**
FIS Base Address Upper (FBU)	31:0	0h	Indicates the upper 32-bits for the received FIS base physical address for this port. This register shall read only 0 for HBAs that do not support 64-bit addressing.

Port–N Interrupt Status - RW - 32 bits [Mem_reg: ABAR + port offset + 10h]			
Field Name	**Bits**	**Default**	**Description**
Device to Host Register FIS Interrupt (DHRS)	0	0b	When the bit is set, a D2H Register FIS has been received with the 'I' bit set, and has been copied into system memory.
PIO Setup FIS Interrupt (PSS)	1	0b	When the bit is set, A PIO Setup FIS has been received with the 'I' bit set, and it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
DMA Setup FIS Interrupt (DSS)	2	0b	When the bit is set, a DMA Setup FIS has been received with the 'I' bit set and has been copied into system memory.
Set Device Bits Interrupt (SDBS)	3	0b	When the bit is set, a Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.
Unknown FIS Interrupt (UFS)	4	0b	Read Only . When the bit is set, an unknown FIS was received with the 'I' bit set and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit (ABAR + port offset + 30h[25]) to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when that FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1, or the two bits may become out-of- sync.
Descriptor Processed (DPS)	5	0b	When the bit is set, a PRD with the 'I' bit set has transferred all of its data.
Port Connect Change Status (PCS)	6	0b	Read Only 0: No change in *Current Connect Status*. This bit reflects the state of PxSERR.DIAG.X (ABAR + port offset + 30h[26]). This bit is only cleared when PxSERR.DIAG.X is cleared. 1: Change in *Current Connect Status*.

Port–N Interrupt Status - RW - 32 bits [Mem_reg: ABAR + port offset + 10h]			
Field Name	**Bits**	**Default**	**Description**
Device Mechanical Presence Status (DMPS)	7	0b	When set, indicates that a mechanical presence switch attached to this port has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid if both CAP.SMPS(ABAR + 00h[28]) and PxCMD.MPSP (ABAR+port offset+18h[19]) are set to 1.
Reserved	21:8	00h	Reserved
PhyRdy Change Status (PRCS)	22	0b	Read Only When set to 1 indicates the internal PhyRdy signal changed state. This bit reflects the state of P0SERR.DIAG.N (ABAR + port offset + 30h[16]). To clear this bit, software must clear P0SERR.DIAG.N to 0.
Incorrect Port Multiplier Status (IPMS):	23	0b	Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. The IPMS bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.
Overflow Status (OFS)	24	0b	Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
Reserved	25	0b	Reserved
Interface Non-fatal Error Status (INFS)	26	0b	Indicates that the HBA encountered an error on the Serial ATA interface and was able to continue operation.
Interface Fatal Error Status (IFS)	27	0b	Indicates that the HBA encountered an error on the Serial ATA interface, which caused the transfer to stop.
Host Bus Data Error Status (HBDS)	28	0b	Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
Host Bus Fatal Error Status (HBFS)	29	0b	Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, it indicates a target or master abort.
Task File Error Status (TFES):	30	0b	This bit is set whenever the status register is updated by the device and the error bit (bit 0) is set.
Cold Port Detect Status (CPDS)	31	0b	When set, a device status has changed as detected by the cold presence detect logic. This bit can either be set due to a non-connected port receiving a device, or a connected port having its device removed. This bit is only valid if the port supports cold presence detect as indicated by PxCMD.CPD (ABAR + port offset +18h [20]) set to 1.

Write 1 clear these status bits

Port-N Interrupt Enable - RW - 32 bits [Mem_reg: ABAR + port offset + 14h]			
Field Name	**Bits**	**Default**	**Description**
Device to Host Register FIS Interrupt Enable (DHRE)	0	0b	When set, and if both GHC.IE (ABAR + 04h [1]) and PxIS.DHRS (ABAR+port offset+10h[0]) are set, the HBA will generate an interrupt.
PIO Setup FIS Interrupt Enable (PSE)	1	0b	When set, if both GHC.IE and PxIS.PSS (ABAR+port offset+10h[1]) are set, the HBA will generate an interrupt.
DMA Setup FIS Interrupt Enable (DSE)	2	0b	When set, if both GHC.IE and PxIS.DSS (ABAR+port offset+10h[2]) are set, the HBA will generate an interrupt.
Set Device Bits FIS Interrupt Enable (SDBE)	3	0b	When set, if both GHC.IE and PxIS.SDBS (ABAR+port offset+10h[3]) are set, the HBA will generate an interrupt.
Unknown FIS Interrupt Enable (UFE)	4	0b	When set, if both GHC.IE and PxIS.UFS (ABAR+port offset+10h[4]) are set to 1, the HBA will generate an interrupt.
Descriptor Processed Interrupt Enable (DPE)	5	0b	When set, the HBA will generate an interrupt if both GHC.IE and PxIS.DPS (ABAR+port offset+10h[5]) are set.
Port Change Interrupt Enable (PCE)	6	0b	When set, the HBA will generate an interrupt if both GHC.IE and PxIS.PCS (ABAR+port offset+10h[6]) are set.

Port-N Interrupt Enable - RW - 32 bits [Mem_reg: ABAR + port offset + 14h]			
Field Name	**Bits**	**Default**	**Description**
Device Mechanical Presence Enable (DMPE)	7	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0IS.DMPS (ABAR+port offset+10h[7]) are set. For systems that do not support a mechanical presence switch, this bit will be read-only and will return a 0.
Reserved	21:8	000h	Reserved
PhyRdy Change Interrupt Enable (PRCE)	22	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0IS.PRCS (ABAR+port offset+10h[22]) are set to 1.
Incorrect Port Multiplier Enable (IPME)	23	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0IS.IPMS (ABAR+port offset+10h[23]) are set.
Overflow Enable (OFE)	24	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0IS.OFS (ABAR+port offset+10h[24]) are set.
Reserved	25		Reserved
Interface Non-fatal Error Enable (INFE)	26	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0IS.INFS (ABAR+port offset+10h[26]) are set.
Interface Fatal Error Enable (IFE)	27	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0IS.IFS (ABAR+port offset+10h[27]) are set.
Host Bus Data Error Enable (HBDE)	28	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0IS.HBDS (ABAR+port offset+10h[28]) are set.
Host Bus Fatal Error Enable (HBFE)	29	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0IS.HBFS (ABAR+port offset+10h[29]) are set.
Task File Error Enable (TFEE)	30	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0S.TFES (ABAR+port offset+10h[30]) are set.
Cold Presence Detect Enable (CPDE)	31	0b	When set, the HBA will generate an interrupt if both GHC.IE and P0S.CPDS (ABAR+port offset+10h[31]) are set. For systems that do not support cold presence detect, this bit will be a read-only and will return a 0.

Port-N Command and Status - R - 32 bits [Mem_reg: ABAR + port offset + 18h]			
Field Name	**Bits**	**Default**	**Description**
Start (ST)	0	0b	RW When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI register (ABAR+port offset+38h) is cleared by the HBA upon the HBA putting the controller into an idle state. This bit will only be set to 1 by software after PxCMD.FRE (ABAR+port offset+18h[4]) has been set to 1.
Spin-Up Device (SUD)	1	1b	This bit is read/write for HBAs that support staggered spin-up via CAP.SSS (ABAR+00h[27]). This bit reads 1 only for HBAs that do not support staggered spin-up. On an edge detect from 0 to 1, the HBA shall start a COMRESET initialization sequence to the device. Clearing this bit does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET(ABAR+port offset+2Ch[3:0])=0h, the HBA will enter listen mode.
Power On Device (POD)	2	1b	This bit is read/write for HBAs that support cold presence detection on this port as indicated by PxCMD.CPD (ABAR+port offset+18h[20]) set to 1. This bit reads 1 only for HBAs that do not support cold presence detect. When set, the HBA sets the state of a pin on the HBA to 1 so that it may be used to provide power to a cold-presence detectable port.

Port-N Command and Status - R - 32 bits [Mem_reg: ABAR + port offset + 18h]			
Field Name	**Bits**	**Default**	**Description**
Command List Override (CLO)	3	0b	RW Setting this bit to 1 causes PxTFD.STS.BSY(ABAR + port offset + 20h[7]) and PxTFD.STS.DRQ (ABAR + port offset + 20h[3]) to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect. This bit shall only be set to 1 immediately prior to setting the PxCMD.ST bit (bit 0) to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and will result in indeterminate behavior. Software must wait for CLO to be cleared to 0 before setting PxCMD.ST to 1.
FIS Receive Enable (FRE)	4	0b	When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB (ABAR + port offset + 08h) (and for 64-bit HBAs, PxFBU (ABAR + port offset + 0Ch)). When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. System software must not set this bit until PxFB (PxFBU) have been programmed with a valid pointer to the FIS receive area, and if software wishes to move the base, this bit must first be cleared, and software must wait for the FR bit in this register to be cleared.
Reserved	7:5	0h	Reserved
Current Command Slot (CCS)	12:8	00h	This field is valid when P0CMD.ST (bit 0) is set to 1 and shall be set to the command slot value of the command that is currently being issued by the HBA. When P0CMD.ST transitions from 1 to 0, this field shall be reset to 0. After P0CMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is P0CMD.CCS + 1. For example, after the HBA has issued its first command, if CCS = 0h and P0CI is set to 3h, the next command that will be issued is from command slot 1.
Mechanical Presence Switch State (MPSS)	13	1b	The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS(ABAR + 00h[28]) and PxCMD.MPSP (ABAR+port offset+18h[19]) are set to 1.
FIS Receive Running (FR):	14	0b	When set, the FIS Receive DMA engine for the port is running.
Command List Running (CR)	15	0b	When this bit is set, the command list DMA engine for the port is running.
Cold Presence State (CPS)	16	0b	The CPS bit reports whether a device is currently detected on this port via cold presence detection. If CPS is set to 1, then the HBA detects via cold presence that a device is attached to this port. If CPS is cleared to 0 , then the HBA detects via cold presence that there is no device attached to this port.

Port-N Command and Status - R - 32 bits [Mem_reg: ABAR + port offset + 18h]			
Field Name	**Bits**	**Default**	**Description**
Port Multiplier Attached (PMA)	17	0b	This bit is read/write for HBAs that support a Port Multiplier (CAP.SPM (ABAR+00h[17])= 1). This bit is read-only for HBAs that do not support a port Multiplier (CAP.SPM = 0). When set to 1 by software, a Port Multiplier is attached to the HBA for this port. When cleared to 0 by software, a Port Multiplier is not attached to the HBA for this port. Software is responsible for detecting whether a Port Multiplier is present; hardware does not auto-detect the presence of a Port Multiplier.
Hot Plug Capable Port (HPCP)	18	1b	When set to 1, it indicates that this port's signal and power connectors are externally accessible via a joint signal and power connector for blindmate device hot plug. When cleared to 0, it indicates that this port's signal and power connectors are not externally accessible via a joint signal and power connector.
Mechanical Presence Switch Attached to Port (MPSP)	19	0b	If set to 1, the platform supports an mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port. When this bit is set to 1, P0CMD.HPCP (bit 18) should also be set to 1.
Cold Presence Detection (CPD)	20	0b	If set to 1, the platform supports cold presence detection on this port. If cleared to 0, the platform does not support cold presence detection on this port. When this bit is set to 1, P0CMD.HPCP (bit 18) should also be set to 1.
External SATA Port (ESP)	21	0b	When set to 1, it indicates that this port's signal connector is externally accessible on a signal only connector. When set to 1, CAP.SXS (ABAR + 00h[5]) shall be set to 1. When cleared to 0, it indicates that this port's signal connector is not externally accessible on a signal only connector. ESP is mutually exclusive with the HPCP bit in this register.
FIS-based Switching Capable Port(FBSCP)	22	1b	When set to 1, it indicates that this port supports Port Multiplier FIS-based switching. When cleared to 0, it indicates that this port does not support FIS-based switching. This bit may only be set to 1 if both CAP.SPM (ABAR + 00h[17]) and CAP.FBSS (ABAR + 00h[16]) are set to 1.
Reserved	23	0h	Reserved
Device is ATAPI (ATAPI)	24	0b	RW When set to 1, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
Drive LED on ATAPI Enable (DLAE)	25	0b	RW When set to 1, the HBA shall drive the LED pin active for commands regardless of the state of P0CMD.ATAPI (ABAR + port offset + 18h[24]). When cleared, the HBA shall only drive the LED pin active for commands if P0CMD.ATAPI is set to 0.
Aggressive Link Power Management Enable (ALPE)	26	0b	RW When set to 1, the HBA shall aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. Software shall only set this bit to 1 if CAP.SALP (ABAR+00h[26]) is set to 1; if CAP.SALP is cleared to 0 software shall treat this bit as reserved.

Port-N Command and Status - R - 32 bits [Mem_reg: ABAR + port offset + 18h]			
Field Name	**Bits**	**Default**	**Description**
Aggressive Slumber / Partial (ASP)	27	0b	RW When set to 1, and ALPE (bit 26) is set, the HBA shall aggressively enter the Slumber state when it clears the PxCI register (ABAR + port offset + 38h) and the PxSACT register (ABAR + port offset + 34h) is cleared or when it clears the PxSACT register and PxCI is cleared. When cleared, and ALPE is set, the HBA shall aggressively enter the Partial state when it clears the PxCI register and the PxSACT register is cleared or when it clears the PxSACT register and PxCI is cleared. If CAP.SALP(ABAR+00h[26]) is cleared to 0 software shall treat this bit as reserved.
Interface Communication Control (ICC)	31:28	0h	RW This field is used to control power management states of the interface. If the Link layer is currently in the L_IDLE state, writing to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writing to this field shall have no effect. **Value** **Definition** *Fh - 7h* *Reserved* 6h **Slumber:** This shall cause the HBA to request a transition of the interface to the Slumber state. The SATA device may reject the request and the interface shall remain in its current state. *5h - 3h* *Reserved* 2h **Partial:** This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state. 1h **Active:** This shall cause the HBA to request a transition of the interface into the active state. 0h **No-Op / Idle:** When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not have occurred yet. When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (i.e. interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state.

Port-N Task Fike Data – R – 32 bits [Mem_reg: ABAR + port offset + 20h]			
Field Name	**Bits**	**Default**	**Description**
Status (STS)	7:0	7Fh	Contains the latest copy of the task file status register. Fields of note in this register that affect AHCI hardware operation are: **Bit** **Field** **Definition** 7 BSY Indicates the interface is busy 6:4 cs Command specific 3 DRQ Indicates a data transfer is requested 2:1 cs Command specific 0 ERR Indicates an error during the transfer.
ERROR	15:8	00h	Contains the latest copy of the task file error register.
Reserved	31:16	0000h	Reserved

Port-N Signature – R – 32 bits [Mem_reg: ABAR + port offset + 24h]			
Field Name	**Bits**	**Default**	**Description**
Signature (SIG)	31:0	FFFFFFFFh	Contains the signature received from a device on the first D2H Register FIS. The bit order is as follows: **Bit** **Field** 31:24 LBA High Register 23:16 LBA Mid Register 15:08 LBA Low Register 07:00 Sector Count Register

The register is updated once after each reset sequence.

Port-N Serial ATA Status – R – 32 bits [Mem_reg: ABAR + port offset + 28h]			
Field Name	**Bits**	**Default**	**Description**
Device Detection (DET)	3:0	0h	Indicates the interface device detection and Phy state. 0h: No device detected and Phy communication not established 1h:Device presence detected but Phy communication not established 3h:Device presence detected and Phy communication established 4h:Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values are reserved. Read Only.
Current Interface Speed (SPD)	7:4	0h	Indicates the negotiated interface communication speed. 0h:Device not present or communication not established 1h:Generation 1 communication rate negotiated 2h:Generation 2 communication rate negotiated 3h:Generation 3 communication rate negotiated All other values are reserved. Read Only.
Interface Power Management (IPM)	11:8	0h	Indicates the current interface state: 0h:Device not present or communication not established 1h:Interface in Active state 2h:Interface in Partial power management state 6h:Interface in Slumber power management state All other values reserved. Read Only.
Reserved	31:12	00000h	Reserved

Port-N Serial ATA Control – RW – 32 bits [Mem_reg: ABAR + port offset + 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Device Detection Initialization (DET)	3:0	0h	Controls the HBA's device detection and interface initialization. 0h: No device detection or initialization action requested 1h: Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h: Disable the Serial ATA interface and put Phy in offline mode. All other values are reserved. This field may only be modified when P0CMD.ST (ABAR + port offset + 18[0])is 0. Changing this field while the P0CMD.ST bit is set to 1 results in undefined behavior. When P0CMD.ST is set to 1, this field should have a value of 0h. Note: It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when DET=1h.
Speed Allowed (SPD)	7:4	0h	Indicates the highest allowable speed of the interface. 0h: No speed negotiation restrictions 1h: Limit speed negotiation to Generation 1 communication rate 2h: Limit speed negotiation to a rate not greater than Generation 2 communication rate 3h Limit speed negotiation to a rate not greater than Generation 3 communication rate All other values are reserved.
Interface Power Management Transitions Allowed (IPM)	11:8	0h	Indicates which power states the HBA is allowed to transition to. If an interface power management state is disabled, the HBA is not allowed to initiate that state and the HBA must $PMNAK_P$ any request from the device to enter that state. 0h No interface restrictions 1h Transitions to the Partial state disabled 2h Transitions to the Slumber state disabled 3h Transitions to both Partial and Slumber states disabled All other values are reserved.
Select Power Management (SPM):	15:12	0h	This field is not used by AHCI. Read Only.
Port Multiplier Port (PMP):	19:16	0h	This field is not used by AHCI. Read Only.
Reserved	31:20	000h	Reserved

Port-N Serial ATA Error – RW – 32 bits [Mem_reg: ABAR + port offset + 30h]			
Field Name	**Bits**	**Default**	**Description**
ERROR	15:0	0000h	The ERR field contains error information for use by host software in determining the appropriate response to the error condition. Write 1 clear. *15:12 Reserved* 11 **Internal Error (E):** The host bus adapter experienced an internal error that caused the operation to fail and may have put the host bus adapter into an error state. The internal error may include a master or target abort when attempting to access system memory, an elasticity buffer overflow, a primitive mis-alignment, a synchronization FIFO overflow, and other internal error conditions. Typically, when an internal error occurs, a non-fatal or fatal status bit in the PxIS register (ABAR + port offset + 10) will also be set to give software guidance on the recovery mechanism required. 10 **Protocol Error (P):** A violation of the Serial ATA protocol was detected. 9 **Persistent Communication or Data Integrity Error (C):** A communication error that was not recovered occurred and is expected to be persistent. Persistent communication errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 **Transient Data Integrity Error (T):** A data integrity error occurred that was not recovered by the interface. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b8b decoding error. *7:2 Reserved* 1 **Recovered Communications Error (M):** Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers. 0 **Recovered Data Integrity Error (I):** A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b8b decoding error.

Port-N Serial ATA Error – RW – 32 bits [Mem_reg: ABAR + port offset + 30h]			
Field Name	**Bits**	**Default**	**Description**
Diagnostics (DIAG)	31:16	0000h	Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes: *31:27 Reserved* 26 **Exchanged (X):** When set to one this bit indicates a COMINIT signal was received. This bit is reflected in the P0IS.PCS bit. 25 **Unknown FIS Type (F):** Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized/known. 24 **Transport state transition error (T):** Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. This bit is always 0 in the current implementation. 23 **Link Sequence Error (S):** Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. This bit is always 0 in current implementation. 22 **Handshake Error (H):** Indicates that one or more R_ERR handshake responses were received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 **CRC Error (C):** Indicates that one or more CRC errors occurred with the Link Layer. 20 **Disparity Error (D):** *This field is not used by AHCI.* This bit is always 0 in the current implementation. 19 **10B to 8B Decode Error (B):** Indicates that one or more 10B to 8B decoding errors occurred. 18 **Comm Wake (W):** Indicates that a Comm Wake signal was detected by the Phy. 17 **Phy Internal Error (I):** Indicates that the Phy detected some internal error. This bit is always 0 in the current implementation. 16 **PhyRdy Change (N):** Indicates that the PhyRdy signal changed state. This bit is reflected in the P0IS.PRCS bit (Mem_reg: ABAR + port offset + 10h[22]). Write 1 clear.

Port-N Serial ATA Active [Mem_reg: ABAR + port offset + 34h]			
Field Name	**Bits**	**Default**	**Description**
Device Status (DS)	31:0	00000000h	This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. This field is set by software prior to issuing a native queued command for a particular command slot. Prior to writing PxCI[TAG] to 1, software will set DS[TAG] to 1 to indicate that a command with that TAG is outstanding. The device clears bits in this field by sending a Set Device Bits FIS to the host. The HBA clears bits in this field that are set to 1 in the SActive field of the Set Device Bits FIS. The HBA only clears bits that correspond to native queued commands that have completed successfully. Software should only write this field when PxCMD.ST (ABAR+port offset+18h[0]) is set to 1. This field is cleared when PxCMD.ST is written from a 1 to a 0 by software. This field is not cleared by a COMRESET or a software reset.

Port-N Command Issue – RW – 32 bits [Mem_reg: ABAR + port offset + 38h]			
Field Name	**Bits**	**Default**	**Description**
Commands Issued (CI)	31:0	00000000h	This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when PxCMD.ST (ABAR+port offset+18h[0]) is set to 1. This field is also cleared when PxCMD.ST is written from a 1 to a 0 by software.

Port- N SNotification – RWC – 32 bits [Mem_reg: ABAR + port offset + 3Ch]			
Field Name	**Bits**	**Default**	**Description**
PM Notify (PMN)	15:0	0000h	This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the host with the Notification bit set. PM Port 0h sets bit 0 … PM Port Fh sets bit 15 Individual bits are cleared by software writing 1's to the corresponding bit positions. This field is reset to default on a HBA Reset, but it is not reset by COMRESET or software reset.
Reserved	31:16	0000h	Reserved

Port-N FIS-based Switching Control – RW – 32 bits [Mem_reg: ABAR + port offset + 40h]			
Field Name	**Bits**	**Default**	**Description**
Enable (EN)	0	0	When set to 1, a Port Multiplier is attached and the HBA shall use FIS-based switching to communicate with it. When cleared to 0, FIS-based switching is not being used. Software shall only change the value of the EN bit when PxCMD.ST (ABAR+port offset+18h[0]) is cleared to 0.
Device Error Clear (DEC)	1	0	When set to 1 by software, the HBA shall clear the device-specific error condition and the HBA shall flush any commands outstanding for the device that experienced the error, including clearing the PxCI (ABAR+port offset+38h) and PxSACT bits for that device to 0. When hardware has completed error recovery actions, hardware shall clear the bit to 0. A write of 0 to this bit by software shall have no effect. Software shall only set this bit to 1 if PxFBS.EN (bit 0) is set to 1 and PxFBS.SDE (bit 2) is set to 1.
Single Device Error (SDE)	2	0	When set to 1 and a fatal error condition has occurred, hardware believes the error is localized to one device such that software's first error recovery step should be to utilize the PxFBS.DEC (bit 1) functionality. When cleared to 0 and a fatal error condition has occurred, the error applies to the entire port and to clear the error PxCMD.ST (ABAR+port offset+18h[0]) shall be cleared to 0 by software. This bit is cleared on PxFBS.DEC being set to 1 or on PxCMD.ST (ABAR+port offset+18h[0]) being cleared to 0.
Reserved	7:3	0h	Reserved
Device To Issue (DEV)	11:8	0h	Set by software to the Port Multiplier port value of the next command to issue. This field enables hardware to know the port the command is to be issued to without fetching the command header. Software shall not issue commands to multiple Port Multiplier ports on the same write of the PxCI (ABAR+port offset+38h) register.

Port-N FIS-based Switching Control – RW – 32 bits [Mem_reg: ABAR + port offset + 40h]			
Field Name	**Bits**	**Default**	**Description**
Active Device Optimization (ADO)	15:12	2h	This register exposes the number of active devices that the FIS-based switching implementation has been optimized for. When there are more devices active than indicated in this field, throughput of concurrent traffic may degrade. For optimal performance, software should limit the number of active devices based on this value. The minimum value for this field shall be 2h, indicating that at least two devices may be active with high performance maintained.
Device With Error (DWE)	19:16	0h	Set by hardware to the value of the Port Multiplier port number of the device that experienced a fatal error condition. This field is only valid when PxFBS.SDE (bit 2) = 1.
Reserved	31:20	000h	Reserved

2.2 OHCI USB 1.1 and EHCI USB 2.0 Controllers (Bus 0, Device 18/19/22, Function 0; Device 20, Function 5)

2.2.1 USB1/USB2/USB3 (Device-18/19/22, func-0) OHCI PCI Configuration Registers

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID / Class Code	08h
Miscellaneous	0Ch
BAR_OHCI	10h
Subsystem Vendor ID / Subsystem ID	2Ch
Capability Pointer	34h
Interrupt Line	3Ch
Config Timers / MSI Disable	40h – 41h
Port Disable Control	42h
Reserved	46h
Port Force Reset	48h
OHCI Misc Control 1	50h
OHCI Misc Control 2	52h
Over Current Control 1	58h
OHCI OverCurrentPME Enable	68h
Target Timeout Control	74h
Reserved	78h
Reserved	7Ch
Reserved	80h
MSI Control	D0h
MSI Address	D4h
MSI Data	D8h
Reserved	E4h
Reserved	F0h
Reserved	F4h

Vendor ID – R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1002h	Vendor Identifier. The vendor ID is 0x1002. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor IDs

Device ID – R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	4397h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.

Command – RW - 16 bits - [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Space Accesses	0	0b	0: Disable the device response. 1: Allow the device to respond to I/O Space accesses.
Memory Space Accesses	1	0b	0: Disable the device response. 1: Allow the device to respond to Memory Space accesses.
Bus Master	2	0b	0: Disable the device from generating PCI accesses. 1: Allow the device to behave as a bus master.
Special Cycle	3	0b	Hard-wired to 0, indicating no Special Cycle support.
Memory Write and Invalidate Command	4	0b	0: Memory Write must be used. 1: Masters may generate the command.
VGA Palette Register Accesses	5	0b	Hard-wired to 0, indicating the device should treat palette write accesses like all other accesses.
Parity Enable	6	0b	0: the device sets its Detected Parity Error status bit (bit [15] in the Status register) when an error is detected, but continues normal operations without asserting PERR#. 1: The device must take its normal action when a parity error is detected.
Reserved	7	0b	Hard-wired to 0 per PCI2.3 spec.
SERR# Enable	8	0b	0: Disable the SERR# driver. 1: Enable the SERR# driver. Note: Address parity errors are reported only if this bit and bit [6] are 1.
Fast Back-to-Back Enable	9	0b	0: Only fast back-to-back transactions to the same agent are allowed. 1: The master is allowed to generate fast back-to-back transactions to different agents.
Interrupt Disable	10	0b	0: Enable the assertion of the device/function's INTx# signal. 1: Disable the assertion of the device/function's INTx# signal.
Reserved	15:11		Reserved

Status – R - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0		Reserved
Interrupt Status	3	0b	This bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0, and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
Capabilities List	4	1b	0: Indicates that no New Capabilities linked list is available. 1: Indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
66 MHz Capable	5	1b	Hard-wired to 1, indicating 66MHz capable.
Reserved	6		Reserved
Fast Back-to-Back Capable	7	1b	Hard-wired to 1, indicating Fast Back-to-Back capable.
Master Data Parity Error	8	0b	This bit is set when any of the following three conditions is met: (1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); (2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit (Command register) is set.
DEVSEL Timing	10:9	01b	Hard-wired to 01b – Medium timing
Signaled Target Abort	11	0b	This bit is set by a target device whenever it terminates a transaction with Target-Abort.
Received Target Abort	12	0b	This bit is set by a master device whenever its transaction is terminated with Target-Abort.
Received Master Abort	13	0b	This bit is set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort.

Status – R - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Signaled System Error	14	0b	This bit is set whenever the device asserts SERR#.
Detected Parity Error	15	0b	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit [6] in the Command register).

Revision ID / Class Code – R - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	00h	Revision ID.
PI	15:8	10h	Programming Interface. A constant value of 10h identifies the device being an OpenHCI Host Controller.
SC	23:16	03h	Sub Class. A constant value of 03h identifies the device being of Universal Serial Bus.
BC	31:24	0Ch	Base Class. A constant value of 0Ch identifies the device being a Serial Bus Controller.

Miscellaneous – RW/R - 32 bits - [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This read/write field specifies the system cache line size in units of DWORDs and must be initialized to 00h.
Latency Timer	15:8	00h	Bits [9:8] are hard-wired to 00b, resulting in a timer granularity of at least four clocks. This field specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.
Header Type	23:16	80h	This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space), and also whether or not the device contains multiple functions. Bit [23] hard-wired to 1 → the device has multiple functions. Bits [22:16] hard-wired to 00h.
BIST	31:24	00h	Hard-wired to 00h, indicating no build-in BIST support.

Bar_OHCI – RW - 32 bits - [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
IND	0	0b	Indicator. Read Only. A constant value of 0 indicates that the operational registers of the device are mapped into memory space of the main memory of the PC host system.
TP	2:1	00b	Type. Read Only. A constant value of 00b indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space; i.e., lower 4 GB of the main memory of the PC host.
PM	3	0b	Prefetch memory. Read Only. A constant value of 0 indicates that there is no support for “prefetchable memory”.
Reserved	11:4	000h	These bits are read only and hardwired to zero..
BAR	31:12	00000h	Base Address. Specifies the upper 20 bits of the 32-bit starting base address. This represent a maximum of 4-kbyte addressing space for the OpenHCI’s operational registers.

Subsystem Vendor ID / Subsystem ID – RW - 32 bits - [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	Can only be written once by software.
Subsystem ID	31:16	0000h	Can only be written once by software.

Capability Pointer – R - 8 bits - [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capability Pointer	7:0	D0h	Address of the 1st element of capability link.

Interrupt Line – RW – 32 bits - [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	The Interrupt Line register is an eight-bit register used to communicate interrupt line routing information. The register is read/write and must be implemented by any device (or device function) that uses an interrupt pin. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value; rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.
Interrupt Pin	15:8	01h	Read Only. Hard-wired to 01h, corresponding to using INTA#
MIN_GNT	23:16	00h	Read Only. Hardwired to 00h to indicate no major requirements for the settings of Latency Timers.
MAX_LAT	31:24	00h	Read Only. Hardwired to 00h to indicate no major requirements for the settings of Latency Timers.

Config Timers / MSI Disable – RW - 16 bits - [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
TRDY Timer	7:0	80h	Target Ready timer to timeout non-responding target.
MSI Disable	8	1b	When the bit is set, MSI capability will be disabled.
Reserved	15:9	00h	Reserved

Port Disable – RW ** - 16 bits - [PCI_Reg:42h]			
Field Name	**Bits**	**Default**	**Description**
Port_Disable	4:0 *	00h	When these bits are set, the corresponding ports are disabled. For example, if bit [0] is set then port-0 (its corresponding port) is disabled; if bit [1] is set, then its corresponding port (port-1) is disabled (and so on). Only value 1 can be written into the register, the bit can be cleared to 0 by system reset (PciRst#). That is, when the bit is set to 1, the value is locked and cannot be cleared by any software write.**
Reserved	11:5	00h	Reserved
Reserved	15:12	Fh	Reserved

Notes:
*Bit [4] in USB3 is a reserved bit.
**Only writing value 1 have an effect on the register value; software writing 0 has no effect. The register can only be cleared by a hardware reset.

Reserved – RW - 16 bits - [PCI_Reg:46h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	0000h	Reserved

Port Force Reset – RW - 16 bits - [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
Port0 Force Reset Enable	1:0	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Port1 Force Reset Enable	3:2	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Port2 Force Reset Enable	5:4	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Port3 Force Reset Enable	7:6	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Port4 Force Reset Enable	9:8 *****	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Reserved	15:10	00h	Reserved

*** Note:** Bits [9:8] in USB3 are reserved bits.

OHCI Misc Control 1 – RW - 16 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
OHCI Dynamic Power Saving Enable	0	0b	When this bit is set, Dynamic Power Saving for OHCI is enabled**.** By default, the power saving function is disabled.
Reserved	1	-	
Reserved	4:2	-	
Reserved	5	-	
OHCI Cache Enable	6	1b	Enable 64 byte OHCI DMA cache.
Reserved	7	-	

OHCI Misc Control 1 – RW - 16 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
OHCI Prefetch Cache Line Count	9:8	11b	Number of data cache lines prefetch requests for ISO out transaction. 00: Prefetch is disabled. 01: 1 cache line 10: 2 cache lines 11: 3 cache lines
OHCI Prefetch Time Out Timer	11:10	00b	Time out timer to purge the prefetch data in AB data FIFO if the data is not used. 00: 255ms 01: 511ms 10: 767ms 11: 1023ms
SMI Handshake Disable	12	1b	If this bit is set, the handshake between USB and ACPI is disabled when SMI is requested by USB
Reserved	14:13	-	
OHCI Disconnect Detection Time	15	0b	Set the bit to increase the OHCI disconnect (SE0 state) detection time. 0: 2.33 micro-seconds 1: 6.16 micro-seconds

OHCI Misc Control 2 – RW - 16 bits - [PCI_Reg:52h]			
Field Name	**Bits**	**Default**	**Description**
C4 Early Exit Timer	1:0	00	Timer to control the C4 exit. USB OHCI controller send C4 break up request ahead of time before the next DMA request ready. 00: 20 micro seconds 01: 30 micro seconds 10: 35 micro seconds 11: 40 micro seconds
C4 Early Exit Enable	2	0b	Set the bit to 1 to enable early C4 exit function. This bit should be set only when the system supports C4.
Reserved	7:3	0b	Reserved
OHCI Loopback Control Register Enable	8	0b	Set the bit to Enable HcLoopBackControl Register (OHCI Mem_reg xF0). The HcLoopBackControl register is hidden by default and can only be accessed by software when this bit is set.
Reserved	9	0b	Reserved
Reserved	10	-	
Reserved	11	-	
Reserved	12	-	
OHCI Hold Resume Enable	13	1b	Set the bit to enable OHCI holding resume signaling on remote resume detection.
Wake On Resume Enhancement Enable	14	1b	Set the bit to enable USB S3 wake on resume enhancement.
PME Merge Disable	15	1b	Set the bit to disable merging PMEs from all 4 USB controllers.

Over Current Control 1 – R - 32 bits - [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
HS Port0 OverCurrent Control	3:0	Fh	This register controls the OverCurrent pin mapping for port-0. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-0.

Over Current Control 1 – R - 32 bits - [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
HS Port1 OverCurrent Control	7:4	Fh	This register controls the OverCurrent pin mapping for port - 1. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-1.
HS Port2 OverCurrent Control	11:8	Fh	This register controls the OverCurrent pin mapping for port - 2. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-2.
HS Port3 OverCurrent Control	15:12	Fh	This register controls the OverCurrent pin mapping for port - 3. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-3.
HS Port4 OverCurrent Control *****	19:16	Fh	This register controls the OverCurrent pin mapping for port - 4. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for port-4.
Reserved	31:20	0h	Reserved.

There are 8 pins that can be used for USB OverCurrent function – USB_OC0#/JTG_RST#/GEVENT12#, USB_OC1#/JTG_TDI#/GEVENT13#, USB_OC2#/JTG_TCK#/GEVENT14#, USB_OC3#/JTG_TDO#/GEVENT15#, USB_OC4#/IR_RX0/GEVENT16#, USB_OC5#/IR_TX0/GEVENT17#, USB_OC6#/IR_TX1/GEVENT6, USB_OC7#/LEDBlink/GEVENT18#

Register value-to-OverCurrent Pin mapping:
USB_OC0# = 0000, USB_OC1# = 0001, USB_OC2# = 0010, USB_OC3# = 0011,
USB_OC4# = 0100, USB_OC5# = 0101, USB_OC6# = 0110, USB_OC7# = 0111

Note: Since OverCurrent pins can be used as GPM# as well, the corresponding register bits to set the pin as OverCurrent have to be set in Smbus Controller.

***Note:** USB3 does not have Port4 so the control field has no effect, but the default is still Fh.

OHCI OverCurrent PME Enable – RW - 16 bits - [PCI_Reg:68h]			
Field Name	**Bits**	**Default**	**Description**
OHCI OverCurrent PME Enable	4:0	00h	Writing this bit to 1 enables the respective port to be sensitive to over-current conditions as wake-up events when it is owned by OHCI.
Reserved	15:5	00h	Reserved

Target Timeout Control – RW - 32 bits - [PCI_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**
Retry Counter	7:0	FFh	Counter to control the purge of the delay queue when the downstream access cycle is not completed within certain time. The transaction is target aborted when counter expired. The retry counter can be disabled by writing 00h in this register.
Reserved	23:8	0000h	Reserved
Timeout Timer	31:24	80h	Timer to control the purge of the delay queue when the master that has initiated the access does not return to complete the transaction. After the timer expires, the queue is invalidated and the next transaction is serviced.

Reserved – RW - 32 bits - [PCI_Reg:78h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW - 32 bits - [PCI_Reg:78h]			
Field Name	**Bits**	**Default**	**Description**

Reserved – RW - 32 bits - [PCI_Reg:7Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW - 32 bits - [PCI_Reg:80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

MSI Control – RW - 32 bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
MSI USB	7:0	05h	MSI USB ID. Read only.
Next Item Pointer	15:8	00h	Pointer to next capability structure
MSI Control Out	16	0b	Set to 1 to disable IRQ. Use MSI instead.
Reserved	19:17	000b	Reserved
MSI Control	22:20	000b	MSI control field
Reserved	31:23	00h	Reserved

MSI Address – RW - 32 bits - [PCI_Reg:D4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0		Reserved. Read-only.
MSI Address	31:2	0h	System-specified message address.

MSI Data – RW - 16 bits - [PCI_Reg:D8h]			
Field Name	**Bits**	**Default**	**Description**
MSI Data	15:0	0h	System-specified message.

Reserved– R - 32 bits - [PCI_Reg:E4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RO - 32 bits - [PCI_Reg:F0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RO - 32 bits - [PCI_Reg:F4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

2.2.2 IDE Controller Registers (Bus 0, Device 20, Function 1)

Note: This section applies only when SATA is operating in Combined Mode

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID/Class Code	08h
Cache Link Size	0Ch
Master Latency Timer	0Dh
Header Type	0Eh
BIST Mode Type	0Fh
Base Address 0	10h
Base Address 1	14h
Base Address 2	18h
Base Address 3	1Ch
Bus Master Interface Base Address	20h
Reserved	24-28h
Subsystem ID and Subsystem Vendor ID	2Ch
Reserved	30h
Capabilities Pointer	34h
Reserved	38h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min_gnt	3Eh
Max_latency	3Fh
IDE Internal Control	40h
Reserved	42h
Watch Dog Control And Status	44h
Watch Dog Counter	46h
Reserved	48-67h
IDE MSI Programmable Weight	68h
Reserved	69-6Fh
IDE MSI Control	70h
IDE MSI Address Register	74h
IDE MSI Data Register	78h
Reserved	7C-7Fh
IDE IDP Address Register	80h
IDE IDP Data Register	84h

Vendor ID - R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1002h	Vendor Identifier.

Vendor ID Register: This register holds a unique 16-bit value assigned to a vendor, and combined with the device ID it identifies any PCI device.

Device ID - R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	439Ch	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID it, identifies any PCI device.

Command – RW – 16 bits – [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
I/O Access Enable	0	0b	I/O Access Enable. This bit controls access to the I/O space registers. When this bit is 1, it enables access to Legacy IDE ports, and PCI bus master IDE I/O registers are enabled.

Command – RW – 16 bits – [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
Memory Access Enable	1	0b	Memory Access Enable. This function is not implemented. This bit is always 0.
Bus Master Enable	2	0b	Master Enable. Bus master function enable. 1=enable, 0=disable.
Special Cycle Recognition Enable	3	0b	Read Only. Hard-wired to 0 indicates that no special support.
Memory Write and Invalidate Enable	4	0b	Read Only. Hard-wired to 0 indicates that memory write and invalidate command is not supported.
VGA Palette Snoop Enable	5	0b	Read Only. VGA Palette Snoop Enable- The IDE host controller does not need to snoop VGA palette cycles. This bit is always 0.
PERR# Detection Enable	6	0b	PERR- (Response) Detection Enable bit – If set to 1, the IDE host controller asserts PERR# when it is the agent receiving data AND it detects a parity error. PERR# is not asserted if this bit is 0.
Wait Cycle Enable	7	0b	Read Only. Wait Cycle enable - The IDE host controller does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
SERR# Enable	8	0b	SERR- enable – If set to 1, the IDE host controller asserts SERR# when it detects an address parity error. SERR# is not asserted if this bit is 0.
Fast Back-to-Back Enable	9	0b	Read Only. Fast Back-to-back enable. The IDE host controller only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
Interrupt Disable	10	0b	Interrupt disable bit (comply to PCI 2.3 spec.)
Reserved	15:11	00h	Reserved. Always wired as 0's.

Command Register: The PCI specification defines this register to control a PCI device's ability to generate and respond to PCI cycles.

Status – RW – 16 bits – [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0b	Reserved. These bits are always read as 0.
Interrupt Status	3	0b	Interrupt status bit. It complies with the PCI 2.3 specification.
Capabilities List	4	1b	This bit is hardwired to 1 to indicate that the Capabilities Pointer is located at 34h**. Can be programmed if PCI_Reg40h[0] is set.**
66MHz Support	5	1b	66MHz capable. This feature is supported in the IDE host controller.
Reserved	6	0b	Reserved.
Fast Back-to-Back Capable	7	0b	Read Only. Fast Back-to-Back Capable. This feature is not implemented and this bit is always 0.
Data Parity Error	8	0b	Data Parity reported – Set to 1 if the IDE host controller detects PERR# asserted while acting as PCI master (whether PERR# was driven by IDE host controller or not.)
DEVSEL# Timing	10:9	01b	Read Only. DEVSEL# timing – Read only bits indicating DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
Signaled Target Abort	11	0b	Signaled Target Abort – This bit is set to 1, when the IDE host controller signals Target Abort.
Received Target Abort	12	0b	Received Target Abort – This bit is set to 1 when the IDE host controller-generated PCI cycle (IDE host controller is the PCI master) is aborted by a PCI target. Cleared by writing a 1 to it.

Status – RW – 16 bits – [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Received Master Abort Status	13	0b	Received Master Abort Status. Set to 1 when the IDE host controller acting as a PCI master, aborts a PCI bus memory cycle. Cleared by writing a 1 to this bit. Default – 0.
SERR# Status	14	0b	SERR# status. This bit is set to 1 when the IDE host controller detects a PCI address parity error.
Detected Parity Error	15	0b	Detected Parity Error. This bit is set to 1 when the IDE host controller detects a parity error.

Status Register: The PCI specification defines this register to record status information for PCI related events. This is a read/write register. However, writes can only reset bits. A bit is reset when the register is written and the data in the corresponding bit location is a 1.

Revision ID/Class Code- RW - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	40h	These bits are default to 40h to indicate the revision level of the chip design. **Can be programmed if PCI_Reg40h[0] is set.**
IDE Host Controller Operating Mode Selection	15:8	8Ah	Programmable interface. These 8 bits are read/write. Bit 15 – Master IDE Device. Always 1. Bit 14-12 – Reserved. Always read as 0's. Bit 11 – Programmable indicator for Secondary. Always 1 to indicate that both modes are supported. Bit 10 – Operating Mode for Secondary. 1 = Native PCI-mode. 0 = Compatibility Mode(Default). Bit 9 – Programmable indicator for Primary. Always 1 to indicate that both modes are supported. Bit 8 – Operating Mode for Primary. 1 = Native PCI-mode. 0 = Compatibility mode (Default).
Sub-Class Code	23:16	01h	Sub-Class Code. These 8 bits are read only and wired to 01h to indicate an IDE Controller.
Class Code	31:24	01h	Class Code. These 8 bits are read only and wired to 01h to indicate a Mass-Storage Controller.
Revision ID/Class Code Register: This register contains the device's revision information, generic function of a device, and the specific register level programming interface. The Base class is 01h (Mass-Storage Controller), Sub-class is 01h (IDE Controller).			

Cache Link Size – RW – 8 bits – [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Reserved
Cache Link Size Register	7:4	00h	If the value is 1 that means the cache line size is 16 DW (64 byte).

Cache Line Size Register: This register specifies cache line size and the default value is 00.

Master Latency Timer – RW – 8 bits – [PCI_Reg:0Dh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0h	They are not used and wired to 0.
Master Latency Timer	7:3	00h	Master Latency Timer. This number represents the guaranteed time slice allotted to IDE host controller for burst transactions.

Master Latency Timer: This register specifies the value of Latency Timer in units of PCICLKs.

Header Type – R – 8 bits – [PCI_Reg:0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	00h	Read Only. Header Type. Since the IDE host controller is a single-function device, this register contains a value of 00h.

Header Type Register: This register identifies the IDE controller module as a single function device.

BIST Mode Type – R – 8 bits – [PCI_Reg:0Fh]			
Field Name	**Bits**	**Default**	**Description**
Built-in-Self Test Mode	7:0	00h	Read Only. Built-in-Self Test modes. Since the IDE host controller does not support BIST modes, this register is always read as 00.

BIST Mode Type Register: This register is used for control and status for Built-in-Self test. The IDE host controller has no BIST modes

Base Address 0 – RW – 32 bits – [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to I/O space.
Reserved	2:1	00b	Reserved. Always read as 0's.
Primary IDE CS0 Base Address	15:3	0000h	Base Address for Primary IDE Bus CS0. This register is used for native mode only. Base Address 0 is not used in compatibility mode.
Reserved	31:16	0000h	Reserved. Always read as 0's.

Base Address 0 Register (Primary CS0): When Channel Select (ACPI PCI configuration offset 0xDA bit 1) is set, SATA port 4/5 uses Secondary channel. The Primary channel is un-used.

Base Address 1 – RW – 32 bits – [PCI_Reg:14h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to I/O space.
Reserved	1	0b	Reserved. Always read as 0's.
Primary IDE CS1 Base Address	15:2	0000h	Base Address for Primary IDE Bus CS1. This register is used for native mode only. Base Address 1 is not used in compatibility mode.
Reserved	31:16	0000h	Reserved. Always read as 0's.

Base Address 1 Register (Primary CS1): When Channel select is (ACPI PCI configuration offset 0xDA bit 1) is set, SATA port 4/5 uses Secondary channel. The Primary channel is un-used.

Base Address 2 – RW – 32 bits – [PCI_Reg:18h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to I/O space.
Reserved	2:1	00b	Reserved. Always read as 0's.
Secondary IDE CS0 Base Address	15:3	0000h	Base Address for Secondary IDE Bus CS0. This register is used for native mode only. Base Address 2 is not used in compatibility mode.
Reserved	31:16	0000h	Reserved. Always read as 0's.

Base Address 2 Register (Secondary CS0): When Channel select is (ACPI PCI configuration offset 0xDA bit 1) is cleared, SATA port 4/5 uses Primary channel. The Secondary channel is un-used.

Base Address 3 – RW – 32 bits – [PCI_Reg:1Ch]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to I/O space.
Reserved	1	0b	Reserved. Always read as 0's.
Secondary IDE CS1 Base Address	15:2	0000h	Base Address for Secondary IDE Bus CS1. This register is used for native mode only. Base Address 3 is not used in compatibility mode.
Reserved	31:16	0000h	Reserved. Always read as 0's.

Base Address 3 Register (Secondary CS1): When Channel select is (ACPI PCI configuration offset 0xDA bit 1) is cleared, SATA port 4/5 uses Primary channel. The Secondary channel is un-used .

Bus Master Interface Base Address – RW – 32 bits – [PCI_Reg:20h]			
Field Name	**Bits**	**Default**	**Description**
Resource Type Indicator	0	1b	RTE (Resource Type Indicator). This bit is wired to 1 to indicate that the base address field in this register maps to I/O space.
Reserved	3:1	0h	Reserved. Always read as 0's.
Bus Master Interface Register Base Address	15:4	000h	Base Address for Bus Master interface registers and correspond to AD[15:4].
Reserved	31:16	0000h	Reserved. Always read as 0's.

Bus Master Interface Base Address Register: This register selects the base address of a 16-byte I/O space interface for bus-master functions.

Reserved Register – R – 32 bits – [PCI_Reg:24h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	00000000h	Reserved. Always read as 0's.

Reserved Register – R – 32 bits – [PCI_Reg:28h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	00000000h	Reserved. Always read as 0's.

Subsystem ID and Subsystem Vendor ID – RW – 32 bits – [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	Subsystem Vendor ID
Subsystem ID	31:16	0000h	Subsystem ID

Subsystem ID and Subsystem Vendor ID: This subsystem ID and subsystem Vendor ID register is write once and read only.

Reserved Register – R – 32 bits – [PCI_Reg:30h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	00000000h	Reserved. Always read as 0's.

MSI Capabilities Pointer – R – 32 bits – [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	70h	The first pointer of Capability block. **Can be programmed if PCI_Reg40h[0] is set.**
Reserved	31:8	000000h	Reserved. Always read as 0's.

MSI Capabilities Pointer Register: This register will show the pci configuration register starting address and it is read only.

Reserved Register – R – 32 bits – [PCI_Reg:38h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	00000000h	Reserved. Always read as 0's.

Interrupt Line – RW – 8 bits – [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	Identifies which input on the interrupt controller the function's PCI interrupt request pin (as specified in its Interrupt Pin register) is being routed to.

Interrupt Line Register: This register identifies which of the system interrupt controllers the device interrupt pin is connected to. The value of this register is used by device drivers.

Interrupt Pin – R – 8 bits – [PCI_Reg:3Dh]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin	7:0	02h	Default value is 02h, corresponding to use IntB#**. Can be programmed if PCI_Reg40h[0] is set.**

Interrupt Pin Register: This register identifies the interrupt pin a device uses. Since the IDE host controller uses IRQ14, this value is supposed to be 00. However, the IDE controller will generate the PCI interrupt INTB# signal on the PCI bus. Therefore, this pin register is set to 02h.

Min_gnt – R – 8 bits – [PCI_Reg:3Eh]			
Field Name	**Bits**	**Default**	**Description**
Minimu m Grant	7:0	00h	Hard-wired to 0's and always read as 0's.

Min_gnt Register: This register specifies the desired settings for how long of a burst the IDE host controller needs assuming a clock rate of 33MHz. The value specifies a period of time in units of ¼ microseconds.

Max_latency – R – 8 bits – [PCI_Reg:3Fh]			
Field Name	**Bits**	**Default**	**Description**
Maximum Latency	7:0	00h	Hard-wired to 0's and always read as 0's.

Max_latency Register: This register specifies the Maximum Latency time required before the IDE host controller as a bus-master can start an accesses.

IDE Internal Control – RW- 16 bits – [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
CC_reg_wr_en	0	0b	Once set, the following registers are programmable Revion ID (PCI_Reg08h[7:0]), Capability List (PCI_Reg06h[4]), Capabilities Pointer (PCI_Reg34h[7:0]), Interrup Pin ((PCI_Reg3Dh[7:0]), MSI Capability Next Pointer (PCI_Reg70h[15:8]), Multiple Message Capable bits (PCI_Reg70h[19:17])
Primary channel enable	1	1b	This is the scratch register for AMD driver INF file to indicate the Primary channel present. It has no affect on hardware.
Secondary channel enable	2	1b	This is the scratch register for AMD driver INF file to indicate the Secondary channel present. It has no affect on hardware.
Disable the fix for MSI Interrupt enable.	3	0b	When set, MSI out put will affect by PCI_CFG 0x04[10] interrupt disable and MSI enable. If not set, MIS output is only controlled by MSI enable

IDE Internal Control – RW- 16 bits – [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	13:4	00h	Reserved for read/write enable.
SATA back door access PCI Configuration or BAR5 space	14	0b	Indicate back door access type of SATA HBA PCI configuration space or BAR 5 access. 0: PCI configuration access 1: BAR 5 access
Reserved	15	0b	Reserved for read/write enable.

Reserved Register – R – 16 bits – [PCI_Reg:42h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	0000h	Reserved. Always read as 0's.

Watch Dog Control And Status - RW - 16 bits - [PCI_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
Watchdog Enable	0	0b	Set the bit to enable the watchdog counter for all the PCI down stream transaction for PATA ports.
PATA Watchdog Timeout Status	1	0b	PATA Watchdog Counter Timeout Status bit. This bit indicates that the watchdog counter in a PATA port has expired for PCI down stream transaction and the transaction got aborted due to counter has expired. Software writes 1 to clear the status
Reserved	15:2	0b	Reserved. Still read/write-able.

This register is used from preventing system hang. Reset Condition: PCI Reset, or Power Management State transition from D3 to D0.

Watch Dog Counter - RW - 16 bits - [PCI_Reg:46h]			
Field Name	**Bits**	**Default**	**Description**
Watchdog Counter	7:0	80h	Specifies the timeout retry count for PCI down stream retries. This value is used for PATA ports.
Reserved	15:8	00h	Reserved. Still read/write-able.

This register is used from preventing system hangs. Reset Condition: PCI Reset, or Power Management State transition from D3 to D0.

Reserved Register – R – 256 bits – [PCI_Reg:48h]-- [PCI_Reg:67h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	255:0	0h	Reserved. Always read as 0's.

IDE MSI Programmable Weight - RW- 8 bits - [PCI_Reg:68h]			
Field Name	**Bits**	**Default**	**Description**
MSI Interrupt Weight	5:0	01h	MSI programmable interrupt weight.
Reserved	7:6	0h	Reserved. Always wired as 0's.

IDE MSI Programmable Weight Register: This register specifies MSI weight.

Reserved Register – R – 56 bits – [PCI_Reg:69h] -- [PCI_Reg:6Fh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	55:0	0h	Reserved. Always read as 0's.

IDE MSI Control - RW- 32 bits - [PCI_Reg:70h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	05h	Capability ID (hard_wired to 05h)

IDE MSI Control - RW- 32 bits - [PCI_Reg:70h]			
Field Name	**Bits**	**Default**	**Description**
Capability Next Pointer	15:8	00h	Next Pointer (hard_wired to 00h). **Can be programmed if PCI_Reg40h[0] is set.**
Message Signaled Interrupt Enable	16	0b	MSI Enable (MSI_En)
Multiple Message Capable	19:17	0h	Multiple Message Capable (MMC). **Can be programmed if PCI_Reg40h[0] is set.**
Multiple Message Enable	22:20	0h	Multiple Message Enable (MME).
MSI 64-bit Address	23	0b	64-bit address (hard_wired to 0b)
Reserved	31:24	00h	Reserved. Always wired as 0's.

IDE MSI Control Register: This register specifies MSI Capability ID, next pointer, MSI enable, multiple message capable, multiple message enable bits.

IDE MSI Address Register - RW- 32 bits - [PCI_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**
IDE MSI Address	31:0	0000_0000h	MSI Address

IDE MSI Address Register: This register specifies MSI address.

IDE MSI Data Register - RW- 32 bits - [PCI_Reg:78h]			
Field Name	**Bits**	**Default**	**Description**
IDE MSI Data	15:0	0000h	MSI Data
Reserved	31:16	0000h	Reserved. Always wired as 0's.

IDE MSI Data Register: This register specifies MSI data.

Reserved Register – R – 32 bits – [PCI_Reg:7Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved. Always read as 0's.

IDE Index-Data-Pair (IDP) Indexing Register - RW- 32 bits - [PCI_Reg:80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved. Always wired as 0's.
IDE IDP Index	10:2	000h	Index-data-pair Address
Reserved	31:11	000000h	Reserved. Always wired as 0's.

IDE IDP Address Register: This register specifies indirect address to access SATA PCI configuration space or memory space pointed by SATA BAR 5.

IDE IDP Data Register - RW- 32 bits - [PCI_Reg:84h]			
Field Name	**Bits**	**Default**	**Description**
IDE IDP Data	31:0	0000_0000h	Index-data-pair Data This register is a "window" through which data is read or written to the memory mapped register pointed to by the IDP indexing register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers or PCI configuration registers. Since this is not a physical register, the "default" value is the same as the default value of the register pointed to by IDP indexing.

IDE IDP Data Register: This register specifies IDP data read from or write to SATA block

2.2.3 USB4 (device-20, func-5) OHCI PCI Configuration Registers

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID / Class Code	08h
Miscellaneous	0Ch
BAR_OHCI	10h
Subsystem Vendor ID / Subsystem ID	2Ch
Capability Pointer	34h
Interrupt Line	3Ch
Config Timers / MSI Disable	40h – 41h
Port Disable Control	42h
USB1.1 Pad Control	44h
Port Force Reset	48h
OHCI Misc Control 1	50h
OHCI Misc Control 2	52h
Over Current Control 1	58h
OHCI OverCurrent PME Enable	68h
Target Timeout Control	74h
Reserved	78h
Reserved	7Ch
Reserved	80h
MSI Control	D0h
MSI Address	D4h
MSI Data	D8h
Reserved	E4h
Reserved	F0h
Reserved	F4h

Vendor ID – R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1002h	Vendor Identifier. The vendor ID is 0x1002. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor IDs

Device ID – R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	4399h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.

Command – RW - 16 bits - [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Space Accesses	0	0b	0: Disable the device response. 1: Allow the device to respond to I/O Space accesses.
Memory Space Accesses	1	0b	0: Disable the device response. 1: Allow the device to respond to Memory Space accesses.
Bus Master	2	0b	0: Disable the device from generating PCI accesses. 1: Allow the device to behave as a bus master.
Special Cycle	3	0b	Hard-wired to 0, indicating no Special Cycle support.
Memory Write and Invalidate Command	4	0b	0: Memory Write must be used. 1: Masters may generate the command.
VGA Palette Register Accesses	5	0b	Hard-wired to 0, indicating the device should treat palette write accesses like all other accesses.
Parity Enable	6	0b	0: the device sets its Detected Parity Error status bit (bit [15] in the Status register) when an error is detected, but continues normal operations without asserting PERR#. 1: The device must take its normal action when a parity error is detected.
Reserved	7	0b	Hard-wired to 0 per PCI2.3 spec.
SERR# Enable	8	0b	0: Disable the SERR# driver. 1: Enable the SERR# driver. Note: Address parity errors are reported only if this bit and bit [6] are 1.
Fast Back-to-Back Enable	9	0b	0: Only fast back-to-back transactions to the same agent are allowed. 1: The master is allowed to generate fast back-to-back transactions to different agents.
Interrupt Disable	10	0b	0: Enable the assertion of the device/function's INTx# signal. 1: Disable the assertion of the device/function's INTx# signal.
Reserved	15:11		Reserved

Status – R - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0		Reserved
Interrupt Status	3	0b	This bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0, and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
Capabilities List	4	1b	0: Indicates that no New Capabilities linked list is available. 1: Indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
66 MHz Capable	5	1b	Hard-wired to 1, indicating 66MHz capable.
Reserved	6		Reserved
Fast Back-to-Back Capable	7	1b	Hard-wired to 1, indicating Fast Back-to-Back capable.
Master Data Parity Error	8	0b	This bit is set when any of the following three conditions is met: (1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); (2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit (Command register) is set.
DEVSEL Timing	10:9	01b	Hard-wired to 01b – Medium timing
Signaled Target Abort	11	0b	This bit is set by a target device whenever it terminates a transaction with Target-Abort.
Received Target Abort	12	0b	This bit is set by a master device whenever its transaction is terminated with Target-Abort.
Received Master Abort	13	0b	This bit is set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort.
Signaled System Error	14	0b	This bit is set whenever the device asserts SERR#.

Status – R - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Detected Parity Error	15	0b	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit [6] in the Command register).

Revision ID / Class Code – R - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	00h	Revision ID.
PI	15:8	10h	Programming Interface. A constant value of 10h identifies the device being an OpenHCI Host Controller.
SC	23:16	03h	Sub Class. A constant value of 03h identifies the device being of Universal Serial Bus.
BC	31:24	0Ch	Base Class. A constant value of 0Ch identifies the device being a Serial Bus Controller.

Miscellaneous – RW/R - 32 bits - [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This read/write field specifies the system cache line size in units of DWORDs and must be initialized to 00h.
Latency Timer	15:8	00h	Bits [9:8] are hard-wired to 00b, resulting in a timer granularity of at least four clocks. This field specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.
Header Type	23:16	00h	This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space), and also whether or not the device contains multiple functions. Bit [23] hard-wired to 0 → the device is single function. Bits [22:16] hard-wired to 00h.
BIST	31:24	00h	Hard-wired to 00h, indicating no build-in BIST support.

Bar_OHCI – RW - 32 bits - [PCI_Reg:10h]			
Field Name	**Bits**	**Default**	**Description**
IND	0	0b	Indicator. Read Only. A constant value of 0 indicates that the operational registers of the device are mapped into memory space of the main memory of the PC host system.
TP	2:1	00b	Type. Read Only. A constant value of 00b indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space; i.e., lower 4 GB of the main memory of the PC host.
PM	3	0b	Prefetch memory. Read Only. A constant value of 0 indicates that there is no support for “prefetchable memory”.
Reserved	11:4	000h	These bits are read only and hardwired to zero..
BAR	31:12	00000h	Base Address. Specifies the upper 20 bits of the 32-bit starting base address. This represent a maximum of 4-kbyte addressing space for the OpenHCI’s operational registers.

Subsystem Vendor ID / Subsystem ID – RW - 32 bits - [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	Can only be written once by software.
Subsystem ID	31:16	0000h	Can only be written once by software.

Capability Pointer – R - 8 bits - [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capability Pointer	7:0	D0h	Address of the 1st element of capability link.

Interrupt Line – RW – 32 bits - [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	The Interrupt Line register is an eight-bit register used to communicate interrupt line routing information. The register is read/write and must be implemented by any device (or device function) that uses an interrupt pin. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value; rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.
Interrupt Pin	15:8	01h	Read Only. Hard-wired to 01h, corresponding to using INTA#
MIN_GNT	23:16	00h	Read Only. Hardwired to 00h to indicate no major requirements for the settings of Latency Timers.
MAX_LAT	31:24	00h	Read Only. Hardwired to 00h to indicate no major requirements for the settings of Latency Timers.

Config Timers / MSI Disable – RW - 16 bits - [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
TRDY Timer	7:0	80h	Target Ready timer to timeout non-responding target.
MSI Disable	8	1b	When the bit is set, MSI capability will be disabled.
Reserved	15:9	00h	Reserved

Port Disable – RW* - 16 bits - [PCI_Reg:42h]			
Field Name	**Bits**	**Default**	**Description**
Port_Disable	4:0	00h	When these bits are set, the corresponding ports are disabled. For example, if bit [0] is set then port-0 (its corresponding port) is disabled; if bit [1] is set, then its corresponding port (port-1) is disabled (and so on). Only value 1 can be written into the register, the bit can be cleared to 0 by system reset (PciRst#). That is, when the bit is set to 1, the value is locked and cannot be cleared by any software write*.
Reserved	11:5	00h	Reserved
Reserved	15:12	Fh	Reserved

*** Note :** Only writing value 1 has an effect on the register value; software writing 0 has no effect. The register can only be cleared by hardware reset.

USB1.1 Pad Control (USB4 OHCI only) – RW - 16 bits - [PCI_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
PMOS Driving Strength Control	2:0	001b	Driving strength for the LS/FS Port0 pad PMOS transistors
Reserved	3	0b	Reserved
NMOS Driving Strength Control	6:4	001b	Driving strength for the LS/FS Port1 pad NMOS transistors
Reserved	7	0b	Reserved
Reserved	15:8	00h	Reserved

Port Force Reset – RW - 32 bits - [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
LS/FS Port0 Force Reset Enable	1:0	00b	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
LS/FS Port1 Force Reset Enable	3:2	00h	Enable “Force Reset in S-state” feature. 00/10: Force port reset is disabled. 01: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states only when port is not connected. 11: Host controller will drive the corresponding port to reset state when system entering S3/S4/S5 states regardless of port connection status.
Reserved	15:4	00h	Reserved

OHCI Misc Control 1 – RW - 16 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
OHCI Dynamic Power Saving Enable	0	0b	When this bit is set, Dynamic Power Saving for OHCI is enabled**.** By default, the power saving function is disabled.
Reserved	1	-	
Reserved	3:2	-	
Reserved	4	-	
Reserved	5	-	
OHCI Cache Enable	6	1b	Enable 64 byte OHCI DMA cache.
Reserved	7	-	
OHCI Prefetch Cache Line Count	9:8	11b	Number of data cache lines prefetch requests for ISO out transaction. 00: Prefetch is disabled. 01: 1 cache line 10: 2 cache lines 11: 3 cache lines
OHCI Prefetch Time Out Timer	11:10	00b	Time out timer to purge the prefetch data in AB data FIFO if the data is not used. 00: 255ms 01: 511ms 10: 767ms 11: 1023ms
SMI Handshake Disable	12	1b	If this bit is set, the handshake between USB and ACPI is disabled when SMI is requested by USB
Reserved	13	-	
Reserved	14	-	
OHCI Disconnect Detection Time	15	0b	Set the bit to increase the OHCI disconnect (SE0 state) detection time. 0: 2.33 micro-seconds 1: 6.16 micro-seconds

OHCI Misc Control 2 – RW - 16 bits - [PCI_Reg:52h]			
Field Name	**Bits**	**Default**	**Description**
C4 early exit timer	1:0	00	Timer to control the C4 exit. USB OHCI controller send C4 break up request ahead of time before the next DMA request ready. 00: 20 micro seconds 01: 30 micro seconds 10: 35 micro seconds 11: 40 micro seconds
C4 early exit enable	2	0b	Set the bit to 1 to enable early C4 exit function. This bit should be set only when the system supports C4.
reserved	7:3	-	Reserved
OHCI loopback control register enable	8	0b	Set the bit to Enable HcLoopBackControl Register (OHCI Mem_reg xF0). The HcLoopBackControl register is hidden by default and can only be accessed by software when this bit is set.
Reserved	9	0b	Reserved
Reserved	12:10	-	
OHCI Hold Resume Enable	13	1b	Set the bit to enable OHCI holding resume signaling on remote resume detection.
Wake On Resume Enhancement Enable	14	1b	Set the bit to enable USB S3 wake on resume enhancement.
PME Merge Disable	15	1b	Set the bit to disable merging PMEs from all 4 USB controllers.

Over Current Control 1 – R - 32 bits - [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
FS Port0 OverCurrent Control	3:0	Fh	The register is to control the OverCurrent pin mapping for full-speed port-0. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for full-speed port-0.
FS Port1 OverCurrent Control	7:4	Fh	The register is to control the OverCurrent pin mapping for full-speed port-1. There are 8 OverCurrent pins (USB_OC0 ~ USB_OC7), any value greater than 0x7h will disable the OverCurrent function for full-speed port-1.
Reserved	31:8		Reserved

There are 8 pins that can be used as USB OverCurrent function –
USB_OC0#/JTG_RST#/GEVENT12#, USB_OC1#/JTG_TDI#/GEVENT13#, USB_OC2#/JTG_TCK#/GEVENT14#, USB_OC3#/JTG_TDO#/GEVENT15#, USB_OC4#/IR_RX0/GEVENT16#, USB_OC5#/IR_TX0/GEVENT17#, USB_OC6#/IR_TX1/GEVENT6, USB_OC7#/LEDBlink/GEVENT18#

Register value-to-OverCurrent Pin mapping:
USB_OC0# = 0000, USB_OC1# = 0001, USB_OC2# = 0010, USB_OC3# = 0011,
USB_OC4# = 0100, USB_OC5# = 0101, USB_OC6# = 0110, USB_OC7# = 0111

Note: Since OverCurrent pins can be used as GPM# as well, the corresponding register bits to set the pin as OverCurrent have to be set in Smbus Controller.

OHCI OverCurrent PME Enable – RW - 16 bits - [PCI_Reg:68h]			
Field Name	**Bits**	**Default**	**Description**
OHCI OverCurrent PME Enable	1:0	00h	Writing this bit to 1 enables the respective port to be sensitive to over-current conditions as wake-up events when it is owned by OHCI.
Reserved	15:10	00h	Reserved

Target Timeout Control – RW - 32 bits - [PCI_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**
Retry Counter	7:0	FFh	Counter to control the purge of the delay queue when the host controller does not return the ack. After the counter expires, the transaction is target aborted. The retry counter can be disabled by writing 00h in this Register.
Reserved	23:8	0000h	Reserved
Timeout Timer	31:24	80h	Timer to control the purge of the delay queue when the master that has initiated the access does not return to complete the transaction. After the timer expires the queue is invalidated and the next transaction is serviced.

Reserved – RW - 32 bits - [PCI_Reg:78h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW - 32 bits - [PCI_Reg:7Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW - 32 bits - [PCI_Reg:80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

MSI Control – RW - 32 bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
MSI USB	7:0	05h	MSI USB ID. Read only.
Next Item Pointer	15:8	00h	Pointer to next capability structure
MSI Control Out	16	0b	Set to 1 to disable IRQ. Use MSI instead.
Reserved	19:17	000b	Reserved
MSI Control	22:20	000b	MSI control field
Reserved	31:23	00h	Reserved

MSI Address – RW - 32 bits - [PCI_Reg:D4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0		Reserved. Read-only.
MSI Address	31:2	0h	System-specified message address.

MSI Data – RW - 16 bits - [PCI_Reg:D8h]			
Field Name	**Bits**	**Default**	**Description**
MSI Data	15:0	0h	System-specified message.

Reserved – RW - 32 bits - [PCI_Reg:E4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RO - 32 bits - [PCI_Reg:F0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RO - 32 bits - [PCI_Reg:F4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

2.2.4 USB1/USB2/USB3/USB4 (Device-18/19/22, func-0 & Device-20, func-5) OHCI Memory Mapped Registers

Register Name	Offset Address
HcRevision	0h
HcControl	4h
HcCommandStatus	8h
HcInterruptStatus	Ch
HcInterruptEnable	10h
HcInterruptDisable	14h
HcHCCA	18h
HcPeriodCurrentED	1Ch
HcControlHeadED	20h
HcControlCurrentED	24h
HcBulkHeadED	28h
HcBulkCurrentED	2Ch
HcDoneHead	30h
HcFmInterval	34h
HcFmRemaining	38h
HcFmNumber	3Ch
HcPeriodicStart	40h
HcLSThreshold	44h
HcRhDescriptorA	48h
HcRhDescriptorB	4Ch
HCRhStatus	50h
HcRhPortStatus[1]	54h
…	…
HcRhPortStatus[NDP]	54+4*NDP
OHCI Loop Back feature Support	F0h

HcRevision - R - 32 bits - [MEM_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
REV	7:0	10h	**Revision** This read-only field contains the version of HCI specification.
L	8	1b	**Legacy** This read-only field is 1, indicating that the legacy support registers are present in this HC.
Reserved	31:9		

HcControl - 32 bits - [MEM_Reg:04h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
CBSR	1:0	00b	RW	R	**ControlBulkServiceRatio** This specifies the service ratio between Control and Bulk Eds. Before processing any of the non-periodic lists, HC must compare the ratio specified with its internal count on how many non-empty Control Eds have been processed, in determining whether to continue serving another Control ED or switching to Bulk Eds. CBSR No. of Control Eds Over Bulk Eds Served 0 1:1 1 2:1 2 3:1 3 4:1
PLE	2	0b	RW	R	**PeriodicListEnable** This bit is set to enable the processing of the periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
IE	3	0b	RW	R	**IsochronousEnable** This bit is used by HCD to enable/disable processing of isochronous Eds. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
CLE	4	0b	RW	R	**ControlListEnable** This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.

HcControl - 32 bits - [MEM_Reg:04h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
BLE	5	0b	RW	R	**BulkListEnable** This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.

HcControl - 32 bits - [MEM_Reg:04h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
HCFS	7:6	00b	RW	RW	**HostControllerFunctionalState** for USB 00b: USBRESET 01b: USBRESUME 10b: USBOPERATIONAL 11b: USBSUSPEND A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartofFrame field of HcInterruptStatus. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
IR	8	0b	RW	R	**InterruptRouting** This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If cleared, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
RWC	9	0b	RW	RW	**RemoteWakeupConnected** This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system it is the responsibility of system firmware to set this bit during POST. HC clears the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.
RWE	10	0b	RW	R	**RemoteWakeupEnable** This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
Reserved	31:11				

HcCommandStatus - 32 bits - [MEM_Reg:08h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
HCR	0	0b	RW	RW	**HostControllerReset** This bit is set by HCD to initiate a software reset of HC.Regardless of the functional state of HC, it moves to the USBSUSPEND state in which most of the operational registers are reset except those stated otherwise; e.g., the InterruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub, and no subsequent reset signaling should be asserted to its downstream ports.
CLF	1	0b	RW	RW	**ControlListFilled** This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1, causing Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
BLF	2	0b	RW	RW	**BulkListFilled** This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1, causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
OCR	3	0b	RW	RW	*OwnershipChangeRequest* This bit is set by an OS HCD to request a change of control of the HC. When set, HC will set the OwnershipChange field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
Reserved	15:4				
SOC	17:16	00b	R	RW	*SchedulingOverrunCount* These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problems.
Reserved	31:18				

HcInterruptStatus RW - 32 bits - [MEM_Reg:0Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
SO	0	0b	RW	RW	**SchedulingOverrun** This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.
WDH	1	0b	RW	RW	**WritebackDoneHead** This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
SF	2	0b	RW	RW	**StartofFrame** This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
RD	3	0b	RW	RW	**ResumeDetected** This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRESUME state.
UE	4	0b	RW	RW	**UnrecoverableError** This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing or signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
FNO	5	0b	RW	RW	**FrameNumberOverflow** This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.
RHSC	6	0b	RW	RW	**RootHubStatusChange** This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus [NumberofDownstreamPort] has changed.
Reserved	29:7				
OC	30	0b	RW	RW	**OwnershipChange** This bit is set by HC when HCD sets the OwnershipChangeRequest field in HcCommandStatus. This event, when unmasked, will always generate a System Management Interrupt (SMI) immediately. This bit is tied to 0b when the SMI pin is not implemented.
Reserved	31				

HcInterruptEnable- 32 bits - [MEM_Reg:10h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
SO	0	0b	RW	RW	**SchedulingOverrun** 0: Ignore 1: Enable interrupt generation due to Scheduling Overrun.

HcInterruptEnable- 32 bits - [MEM_Reg:10h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
WDH	1	0b	RW	RW	**HcDoneHeadWriteback** 0: Ignore 1: Enable interrupt generation due to HcDoneHead Writeback.
SF	2	0b	RW	RW	**StartofFrame** 0: Ignore 1: Enable interrupt generation due to Start of Frame.
RD	3	0b	RW	W	**ResumeDetect** 0: Ignore 1: Enable interrupt generation due to Resume Detect.
UE	4	0b	RW	RW	**UnrecoverableError** 0: Ignore 1: Enable interrupt generation due to Unrecoverable Error.
FNO	5	0b	RW	RW	**FrameNumberOverflow** 0: Ignore 1: Enable interrupt generation due to Frame Number Overflow.
RHSC	6	0b	RW	RW	**RootHubStatusChange** 0: Ignore 1: Enable interrupt generation due to Root Hub Status Change.
Reserved	29:7				
OC	30	0b	RW	RW	**OwnershipChange** 0: Ignore 1: Enable interrupt generation due to Ownership Change.
MIE	31	0b	RW	R	**MasterInterruptEnable** A 0 written to this field is ignored by HC. A 1 written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.

HcInterruptDisable - 32 bits - [MEM_Reg:14h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
SO	0	0b	RW	R	**SchedulingOverrun** 0: Ignore 1: Disable interrupt generation due to Scheduling Overrun.
WDH	1	0b	RW	R	**HcDoneHeadWriteback** 0: Ignore 1: Disable interrupt generation due to HcDoneHead Writeback.
SF	2	0b	RW	R	**StartofFrame** 0: Ignore 1: Disable interrupt generation due to Start of Frame.
RD	3	0b	RW	R	**ResumeDetect** 0: Ignore 1: Disable interrupt generation due to Resume Detect.
UE	4	0b	RW	R	**UnrecoverableError** 0: Ignore 1: Disable interrupt generation due to Unrecoverable Error.
FNO	5	0b	RW	R	**FrameNumberOverflow** 0: Ignore 1: Disable interrupt generation due to Frame Number Overflow.

HcInterruptDisable - 32 bits - [MEM_Reg:14h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
RHSC	6	0b	RW	R	**RootHubStatusChange** 0: Ignore 1: Disable interrupt generation due to Root Hub Status Change.
Reserved	29:7				
OC	30	0b	RW	R	**OwnershipChange** 0: Ignore 1: Disable interrupt generation due to Ownership Change.
MIE	31	0b	RW	R	**MasterInterruptEnable** A 0 written to this field is ignored by HC. A 1 written to this field disables interrupt generation due to events specified in the other bits of this register. This field is set after a hardware or software reset.

HcHCCA - 32 bits - [MEM_Reg:18h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	7:0				
HCCA	31:8	000000h	RW	R	**HostControllerCommunicationArea** This is the base address of the Host Controller Communication Area

HcPeriodCurrentED - 32 bits - [MEM_Reg:1Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
PCED	31:4	0000000h	R	RW	*PeriodCurrentED* This is used by HC to point to the head of one of the Periodic lists which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.

HcControlHeadED- 32 bits - [MEM_Reg:20h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
CHED	31:4	0000000h	RW	R	*ControlHeadED* HC traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.

HcControlCurrentED RW - 32 bits - [MEM_Reg:24h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				

HcControlCurrentED RW - 32 bits - [MEM_Reg:24h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
CCED	31:4	0000000h	RW	RW	**ControlCurrentED** This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks ControlListFilled in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to 0 to indicate the end of the Control list.

HcBulkHeadED - 32 bits - [MEM_Reg:28h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
BHED	31:4	0b	RW	R	**BulkHeadED** HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.

HcBulkCurrentED- RW - 32 bits - [MEM_Reg:2Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
BCED	31:4	0000000h	RW	RW	**BulkCurrentED** This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to 0 to indicate the end of the Bulk list.

HcDoneHead- 32 bits - [MEM_Reg:30h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
Reserved	3:0				
DH	31:4	0b	R	RW	**DoneHead** When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to 0 whenever HC writes the content of this register to HCCA. It also sets WritebackDoneHead of HcInterruptStatus.

HcFmInterval - 32 bits - [MEM_Reg:34h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
FI	13:0	2EDFh	RW	R	**FrameInterval** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.
Reserved	15:14				
FSMPS	30:16	0000h	RW	R	**FSLargestDataPacket** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
FIT	31	0b	RW	R	**FrameIntervalToggle** HCD toggles this bit whenever it loads a new value to FrameInterval

HcFmRemaining - 32 bits - [MEM_Reg:38h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
FR	13:0	0000h	R	RW	**FrameRemaining** This counter is decremented at each bit time. When it reaches 0, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval field of HcFmInterval and uses the updated value from the next SOF.
Reserved	30:14				
FRT	31	0b	R	RW	**FrameRemainingToggle** This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.

HcFmNumber - 32 bits - [MEM_Reg:3Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
FN	15:0	0000h	R	RW	**FrameNumber.** This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after FFFFh. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set StartofFrame in HcInterruptStatus.
Reserved	31:16				

HcPeriodicStart - 32 bits - [MEM_Reg:40h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
PS	13:0	0000h	RW	R	**PeriodicStart** After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.
Reserved	31:14				

HcLSThreshold - 32 bits - [MEM_Reg:44h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
LST	11:0	0628h	RW	R	**LSThreshold** This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining is equal or greater than this field. The value is calculated by HCD with the consideration of transmission and setup overhead.
Reserved	31:12				

HcRhDescriptorA - 32 bits - [MEM_Reg:48h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
NDP	7:0	05h/04h/ 02h*	R	R	**NumberDownstreamPorts** These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OpenHCI is 15. * Note: For USB1/USB2 (device-18/19, func-0), each OHCI controller owns 5 downstream ports. For USB3 (device-22. func-0), the OHCI controller owns 4 downstream ports. For USB4 (device-20, func-5), the stand-alone OHCI controller owns 2 downstream ports.
PSM	8	0b	RW	R	**PowerSwitchingMode** This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0: All ports are powered at the same time. 1: Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands **(**Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch **(**Set/ClearGlobalPower).
NPS	9	1b	RW	R	**NoPowerSwitching** These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0: Ports are power switched. 1: Ports are always powered on when the HC is powered on.
DT	10	0b	R	R	**DeviceType** This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
OCPM	11	1b	RW	R	**OverCurrentProtectionMode** This field describes how the overcurrent status for the Root Hub ports are reported. At reset, this field should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0: Over-current status is reported collectively for all downstream ports. 1: Over-current status is reported on a per-port basis.

HcRhDescriptorA - 32 bits - [MEM_Reg:48h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
NOCP	12	0b	RW	R	**NoOverCurrentProtection** This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0: Overcurrent status is reported collectively for all downstream ports 1: No overcurrent protection supported
Reserved	23:13				
POTPGT	31:24	02h	RW	R	**PowerOnToPowerGoodTime** This field specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2 ms.

HcRhDescriptorB - 32 bits - [MEM_Reg:4Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
DR	15:0	0000h	RW	R	**DeviceRemovable** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit [0]: Reserved Bit [1]: Device attached to Port #1 Bit [2]: Device attached to Port #2 ... Bit [15]: Device attached to Port #15

HcRhDescriptorB - 32 bits - [MEM_Reg:4Ch]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
PPCM	31:16	0000h	RW	R	**PortPowerControlMask** Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode=0), this field is not valid. Bit [0]: Reserved Bit [1]: Ganged-power mask on Port #1 Bit [2]: Ganged-power mask on Port #2 ... Bit [15]: Ganged-power mask on Port #15

HcRhStatus - 32 bits - [MEM_Reg:50h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
LPS	0	0b	RW	R	(Read) **LocalPowerStatus** The Root Hub does not support the local power status feature; thus, this bit is always read as 0. (Write) **ClearGlobalPower** In global power mode (PowerSwitchingMode=0), This bit is written to 1 to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a 0 has no effect.
OCI	1	0b	R	RW	**OverCurrentIndicator** This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented, this bit is always 0
Reserved	14:2				

HcRhStatus - 32 bits - [MEM_Reg:50h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
DRWE	15	0b	RW	R	(Read) **DeviceRemoteWakeupEnable** This bit enables the ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0: ConnectStatusChange is not a remote wakeup event. 1: ConnectStatusChange is a remote wakeup event. (Write) **SetRemoteWakeupEnable** 1: Set DeviceRemoveWakeupEnable. 0: Has no effect.
LPSC	16	0b	RW	R	(Read) **LocalPowerStatusChange** The Root Hub does not support the local power status feature; thus, this bit is always read as 0. (Write) **SetGlobalPower** In global power mode (PowerSwitchingMode=0), this bit is written to 1 to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a 0 has no effect.
OCIC	17	0b	RW	RW	**OverCurrentIndicatorChange** This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a 1. Writing a 0 has no effect.
Reserved	30:18				
CRWE	31	-	W	R	(Write) **ClearRemoteWakeupEnable** Writing a 1 clears DeviceRemoveWakeupEnable. Writing a 0 has no effect.

The register below represents a number of similar registers, starting with HcRhPortStatus1 through to HcRhPortStatus[NDP] where NDP represents the range of number of supported downstream ports.

HcRhPortStatus[1 to NDP] - RW - 32 bits - [MEM_Reg:50+4x(1 to NDP)h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
CCS	0	0b	RW	RW	(Read) **CurrentConnectStatus** This bit reflects the current state of the downstream port. 0: No device connected 1: Device connected (Write) **ClearPortEnable** The HCD writes a 1 to this bit to clear the PortEnableStatus bit. Writing a 0 has no effect. CurrentConnectStatus is not affected by any write. Note: This bit is always read 1b when the attached device is non-removable (DeviceRemovable[NDP]).
PES	1	0b	RW	RW	(Read) **PortEnableStatus** This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0: Port is disabled 1: Port is enabled (Write) **SetPortEnable** The HCD sets PortEnableStatus by writing a 1. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.

HcRhPortStatus[1 to NDP] - RW - 32 bits - [MEM_Reg:50+4x(1 to NDP)h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
PSS	2	0b	RW	RW	(Read) **PortSuspendStatus** This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0: Port is not suspended 1: Port is suspended (Write) **SetPortSuspend** The HCD sets the PortSuspendStatus bit by writing a 1 to this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets **ConnectStatusChang**e. This informs the driver that it attempted to suspend a disconnected port.
POCI	3	0b	RW	RW	(Read) **PortOverCurrentIndicator** This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal 0: No overcurrent condition. 1: Overcurrent condition detected. (Write) **ClearSuspendStatus** The HCD writes a 1 to initiate a resume. Writing a 0 has no effect. A resume is initiated only if PortSuspendStatus is set.

HcRhPortStatus[1 to NDP] - RW - 32 bits - [MEM_Reg:50+4x(1 to NDP)h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
PRS	4	0b	RW	RW	(Read) **PortResetStatus** When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0: Port reset signal is not active 1: Port reset signal is active (Write) **SetPortReset** The HCD sets the port reset signaling by writing a 1 to this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.
Reserved	7:5				

HcRhPortStatus[1 to NDP] - RW - 32 bits - [MEM_Reg:50+4x(1 to NDP)h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
PPS	8	0b	RW	RW	(Read) **PortPowerStatus** This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPowerControlMask[NDP]. In global switching mode, (PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset. 0: Port power is off 1: Port power is on (Write) **SetPortPower** The HCD writes a 1 to set the PortPowerStatus bit. Writing a 0 has no effect. Note: This bit is always reads 1b if power switching is not supported.
LSDA	9	X	RW	RW	(read) **LowSpeedDeviceAttached** This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0: Full speed device attached 1: Low speed device attached (write) **ClearPortPower** The HCD clears the PortPowerStatus bit by writing a 1 to this bit. Writing a 0 has no effect.
Reserved	15:10				

HcRhPortStatus[1 to NDP] - RW - 32 bits - [MEM_Reg:50+4x(1 to NDP)h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
CSC	16	0b	RW	RW	**ConnectStatusChange** This bit is set whenever a connect or disconnect event occurs. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0: No change in CurrentConnectStatus 1: Change in CurrentConnectStatus Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
PESC	17	0b	RW	RW	**PortEnableStatusChange** This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0: No change in PortEnableStatus 1: Change in PortEnableStatus
PSSC	18	0b	RW	RW	**PortSuspendStatusChange** This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. This bit is also cleared when ResetStatusChange is set. 0: Resume is not completed 1: Resume completed
OCIC	19	0b	RW	RW	**PortOverCurrentIndicatorChange** This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0: No change in PortOverCurrentIndicator 1: PortOverCurrentIndicator has changed
PRSC	20	0b	RW	RW	**PortResetStatusChange** This bit is set at the end of the 10-ms port reset signal. The HCD writes a 1 to clear this bit. Writing a 0 has no effect. 0: Port reset is not complete 1: Port reset is complete
Reserved	31:21				

OHCI LOOPBACK Feature Support Register

This register is not accessible when the OHCI PCI_Reg x52[8] is set to "0".

HcLoopBackControl - 32 bits - [MEM_Reg:F0h]					
Field Name	**Bits**	**Default**	**HCD**	**HC**	**Description**
LoopBackTestStart	0	0	RW	R	To start the Loop Back test. Software should set this bit to start the loop back test and should clear this bit to clear out all the test status before starting the next loop.
Reserved	3:1				
PortUnderTest	7:4	0	RW	R	Port Under Test. Software selects the port under test through these bits. Software should only program the port number to the range of # of ports that OHCI supports. 0000: port-0 0001: port-1 0010: port-2 ... and so on.
LoopBackTestData	15:8	0	RW	R	1-byte test data pattern for transmit and receive logic check the received data to match with this data pattern.
Reserved	30:16	-	-	-	
LoopBackTestDone	31	0	R	W	Read-only. Host Controller sets the bit when loop back is done. The bit is cleared when software clears the "LoopBackTestStart" bit.

Legacy Support Registers

Four operational registers are used to provide legacy support. Each of these registers is located on a 32-bit boundary. The offset of these registers is relative to the base address of the Host Controller operational registers with HceControl located at offset 100h.

Table 2: Legacy Support Registers

Offset	Register	Description
100h	HceControl	Used to enable and control the emulation hardware and report various status information.
104h	HceInput	Emulation side of the legacy Input Buffer register.
108h	HceOutput	Emulation side of the legacy Output Buffer register where keyboard and mouse data are to be written by software.
10Ch	HceStatus	Emulation side of the legacy Status register.

Three of the operational registers (HceStatus, HceInput, HceOutput) are accessible at I/O address 60h and 64h when emulation is enabled. Reads and writes to the registers using I/O addresses have side effects as outlined in Table 3 below.

Table 3: Emulated Registers

I/O Address	Cycle Type	Register Contents Accessed/Modified	Side Effects
60h	IN	HceOutput	IN from port 60h will set OutputFull in HceStatus to 0
60h	OUT	HceInput	OUT to port 60h will set InputFull to 1 and CmdData to 0 in HceStatus.
64h	IN	HceStatus	IN from port 64h returns current value of HceStatus with no other side effect.
64h	OUT	HceInput	OUT to port 64h will set InputFull to 0 and CmdData in HceStatus to 1.

HceInput Register

Table 4: HceInput Registers

HceInput –RW - 32 bits			
Field Name	**Bits**	**Default**	**Description**
InputData	7:0	00h	This register holds data that is written to I/O ports 60h and 64h.
Reserved	31:8		

I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the Host Controller's operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.

HceOutput Register

HceOutput –RW - 32 bits			
Field Name	**Bits**	**Default**	**Description**
OutputData	7:0	00h	This register hosts data that is returned when an I/O read of port 60h is performed by application software.
Reserved	31:8		

The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.

HceStatus Register

HceStatus –RW - 32 bits			
Field Name	**Bits**	**Default**	**Description**
OutputFull	0	0b	The HC sets this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists.
InputFull	1	0b	Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
Flag	2	0b	Nominally used as a system flag by software to indicate a warm or cold boot.
CmdData	3	0b	The HC sets this bit to 0 on an I/O write to port 60h and to 1 on an I/O write to port 64h.
Inhibit Switch	4	0b	This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
AuxOutputFull	5	0b	IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.
Time-out	6	0b	Used to indicate a time-out
Parity	7	0b	Indicates parity error on keyboard/mouse data.
Reserved	31:8		

The contents of the HceStatus Register are returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Accessing this register through its memory address produces no side effects.

HceControl Register

HceControl - 32 bits			
Field Name	**Bits**	**Reset**	**Description**
EmulationEnable	0	0b	When set to 1, the HC is enabled for legacy emulation. The HC decodes accesses to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generate s an emulation interrupt at appropriate times to invoke the emulation software.
EmulationInterrupt	1	-	Read-only. This bit is a static decode of the emulation interrupt condition.
CharacterPending	2	0b	When set, an emulation interrupt is generated when the OutputFull bit of the HceStatus register is set to 0.
IRQEn	3	0b	When set, the HC generates IRQ1 or IRQ12 as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, then IRQ1 is generated; if it is 1, then an IRQ12 is generated.
ExternalIRQEn	4	0b	When set to 1, IRQ1 and IRQ12 from the keyboard controller causes an emulation interrupt. The function controlled by this bit is independent of the setting of the EmulationEnable bit in this register.
GateA20Sequence	5	0b	Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.
IRQ1Active	6	0b	Indicates that a positive transition on IRQ1 from the keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
IRQ12Active	7	0b	Indicates that a positive transition on IRQ12 from the keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
A20State	8	0b	Indicates current state of Gate A20 on keyboard controller. Used to compare against value written to 60h when GateA20Sequence is active.
Reserved	31:9	-	Must read as 0s.

2.2.5 USB1/USB2/USB3 (Device-18/19/22, func-2) EHCI PCI Configuration Registers

Registers Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID / Class Code	08h
Miscellaneous	0Ch
Base Address – BAR_EHCI	10h
Subsystem ID / Subsystem Vendor ID	2Ch
Capability Pointer	34h
Interrupt Line	3Ch
EHCI Misc Control	50h
EHCI PCI Spare 1	54h
Serial Bus Release Number – SBRN	60h
Frame Length Adjustment – FLADJ	61h
Reserved	62h
PME Control	C0h
PME Data / Status	C4h

Registers Name	Offset Address
MSI Control	D0h
MSI Address	D4h
MSI Data	D8h
EHCI Debug Port Control	E4h
Reserved	F0h
Reserved	F0h
USB Legacy Support Extended Capability – USBLEGSUP	EECP+0h*
USB Legacy Support Control/Status - USBLEGCTLSTS	EECP+4 h*

*** Note:** The EECP field is in the read-only HCCPARAMS register [MEM_Reg: 08h] with the value of A0h.

Vendor ID – R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1002h	Vendor Identifier. The vendor ID is 0x1002. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor IDs

Device ID – R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	4396h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.

Command – RW - 16 bits - [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Space Accesses	0	0b	0: Disable the device response. 1: Allow the device to respond to I/O Space accesses.
Memory Space Accesses	1	0b	0: Disable the device response. 1: Allow the device to respond to Memory Space accesses.
Bus Master	2	0b	0: Disable the device from generating PCI accesses. 1: Allow the device to behave as a bus master.
Special Cycle	3	0b	Hard-wired to 0, indicating no Special Cycle support.
Memory Write and Invalidate Command	4	0b	0: Memory Write must be used. 1: Masters may generate the command.
VGA Palette Register Accesses	5	0b	Hard-wired to 0, indicating the device should treat palette write accesses like all other accesses.
Parity Enable	6	0b	0: the device sets its Detected Parity Error status bit (bit [15] in the Status register) when an error is detected, but continues normal operations without asserting PERR#. 1: The device must take its normal action when a parity error is detected.
Reserved	7	0b	Hard-wired to 0 per PCI2.3 spec.
SERR# Enable	8	0b	0: Disable the SERR# driver. 1: Enable the SERR# driver. Note: Address parity errors are reported only if this bit and bit [6] are 1.
Fast Back-to-Back Enable	9	0b	0: Only fast back-to-back transactions to the same agent are allowed. 1: The master is allowed to generate fast back-to-back transactions to different agents.
Interrupt Disable	10	0b	0: Enable the assertion of the device/function's INTx# signal. 1: Disable the assertion of the device/function's INTx# signal.
Reserved	15:11		Reserved

Status – R - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0		Reserved
Interrupt Status	3	0b	This bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
Capabilities List	4	1b	0: Indicates that no New Capabilities linked list is available. 1: Indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
66 MHz Capable	5	1b	Hard-wired to 1, indicating 66MHz capable.
Reserved	6		Reserved
Fast Back-to-Back Capable	7	1b	Hard-wired to 1, indicating Fast Back-to-Back capable.
Master Data Parity Error	8	0b	This bit is set when any of the following three conditions is met: (1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); (2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit (Command register) is set.
DEVSEL timing	10:9	01b	Hard-wired to 01b – medium timing
Signaled Target Abort	11	0b	This bit is set by a target device whenever it terminates a transaction with Target-Abort.
Received Target Abort	12	0b	This bit is set by a master device whenever its transaction is terminated with Target-Abort.
Received Master Abort	13	0b	This bit is set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort.
Signaled System Error	14	0b	This bit is set whenever the device asserts SERR#.
Detected Parity Error	15	0b	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).

Revision ID / Class Code – R - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	00h	Revision ID.
PI	15:8	20h	Programming Interface. A constant value of '20h' identifies the device being an EHCI Host Controller.
SC	23:16	03h	Sub Class. A constant value of '03h' identifies the device being of Universal Serial Bus.
BC	31:24	0Ch	Base Class. A constant value of '0Ch' identifies the device being a Serial Bus Controller.

Miscellaneous – RW - 32 bits - [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This read/write field specifies the system cache line size in units of DWORDs and must be initialized to 00h.
Latency Timer	15:8	00h	Bits[9:8] are hard-wired to 00b, resulting in a timer granularity of at least four clocks. This field specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.
Header Type	23:16	00h	Read Only. This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space) and also whether or not the device contains multiple functions. EHCI has single function and bits[23:16] are hard-wired to 00h.

Miscellaneous – RW - 32 bits - [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
BIST	31:24	00h	Hard-wired to 00h, indicating no build-in BIST support.

BAR_EHCI – RW - 32 bits - [PCI_Reg : 10h]			
Field Name	**Bits**	**Default**	**Description**
IND	0	0b	Indicator. Read Only. A constant value of 0 indicates that the operational registers of the device are mapped into memory space of the main memory of the PC host system.
TP	2:1	00b	Type. Read Only. A constant value of 00b indicates that the base register is 32-bit wide and can be placed anywhere in the 32-bit memory space; i.e., lower 4 GB of the main memory of the PC host.
PM	3	0b	Prefetch Memory. A constant value of 0 indicates that there is no support for "prefetchable memory". Read Only.
Reserved	7:4	0h	Read Only.
BA	31:8	000000h	Base Address. Corresponds to memory address signals [31:8].

BAR register. Base address used for the memory mapped capability and operational registers.

Subsystem ID / Subsystem Vendor ID – RW - 32 bits - [PCI_Reg:2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	Can only be written once by software.
Subsystem ID	31:16	0000h	Can only be written once by software.

Capability Pointer – R - 8 bits - [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capability Pointer	7:0	C0h*	Address of the 1st element of capability link.

***Note:** If PME Capability is disabled by setting PME Disable bit (PCI Register x50[5]), then Capability Pointer contains MSI Capability Pointer DCh. If MSI Capability is disabled by setting MSI Disable bit (PCI Register x50[6]), then Capability Pointer contains Debug Port Capability Pointer xE4h.

Interrupt Line - RW - 32 bits - [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	The Interrupt Line is a field used to communicate interrupt line routing information. The register is read/write and must be implemented by any device (or device function) that uses an interrupt pin. POST software will write the routing information into this register as it initializes and configures the system. The value in this field tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value; rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.
Interrupt Pin	15:8	02h	Read Only. Hard-wired to 02h, which corresponds to using INTB#
MIN_GNT	23:16	00h	Read Only. Hard-wired to 00h to indicate no major requirements for the settings of Latency Timers.
MAX_LAT	31:24	00h	Read Only. Hard-wired to 00h to indicate no major requirements for the settings of Latency Timers.

EHCI Misc Control – RW - 32 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
D3Cold PME support	0	0b	Enable EHCI host controller PME support at D3Cold. 0: Disable 1: Enable
Disable SMI	1	0b	To disable EHCI_SMI sent to “USB SMI” output (to ACPI). 0: Enable 1: Disable
Reserved	4:2	-	Reserved
PME Disable	5	0b	Set to 1 to disable PME support
MSI Disable	6	0b	Set to 1 to disable MSI support
Reserved	7	0b	Reserved
Async Park IN Control	11:8	1h	Async Park Mode Count for IN Packet 0h: Standard count as the value in USBCMD[9:8] 1h: 8 packets 2h: 16 packets 3h: 32 packets 4h: 64 packets 5h: 128 packets 6h ~ Fh : reserved
Async Park OUT Control	15:12	2h	Async Park Mode Count for OUT Packet 0h: Standard count as the value in USBCMD[9:8] 1h: 8 packets 2h: 16 packets 3h: 32 packets 4h: 64 packets 5h: 128 packets 6h ~ Fh : reserved
Cache Timer Control *	16	0b	Set to 1 to disable purge timeout timer if HC doesn't come back to request the cached data. 0 — Max Time (ns): 737280 — Min Time (ns): 491520 1 — Max Time (ns): No limit — Min Time (ns): No limit
Reserved	20:17	-	Reserved
Enable IP Gap Fix	21	0b	Set to 1 to enable IP gap protection on starting a new transaction.
Reserved	22	-	
AsyncPark Disable	23	0b	Set to 1 to disable async-park mode.
Async QH Cache Threshold Control	24	0b	For OUT, 0: Cache only if packet size is greater than 128 Bytes. 1: Cache only if packet size is greater than 64 Bytes. For IN, 0: Cache only if expected packet size is greater than 192 Bytes. 1: Cache only if expected packet size is greater than 96 Bytes.
Disable Async QH Cache	25	0b	Set to 1 to disable async QH/QTD cache.
Disable Async Data Cache	26	0b	Set to 1 to disable async data cache request.
Disable Periodic List Cache	27	0b	Set to 1 to disable periodic list cache.
Disable Async QH Cache Enhancement	28	0b	Set to 1 to disable async QH/QTD cache enhancement.
Reserved	30:29	-	Reserved
PHY Advance Power Saving Enable	31	1b	Set to 1 to enable the advance PHY power saving feature to save active power from USBPHY.

EHCI Spare 1 – RW - 32 bits - [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0h	Reserved

SBRN – R - 8 bits - [PCI_Reg:60h]			
Field Name	**Bits**	**Default**	**Description**
SBRN	7:0	20h	**Serial Bus Release Number** Hard-wired to 20h.

FLADJ – RW - 8 bits - [PCI_Reg:61h]			
Field Name	**Bits**	**Default**	**Description**
FLADJ	5:0	20h	**Frame Length Timing Value** Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. **FLADJ Value in decimals [hexadecimal value] Frame Length (# High Speed bit times in decimals)** 0 [00h] 59488 1 [01h] 59504 2 [02h] 59520 … … 31 [1Fh] 59984 32 [20h] 60000 … … 62 [3Eh] 60480 63 [3Fh] 60496
Reserved	7:6		Reserved.

Reserved – RW - 16 bits - [PCI_Reg:62h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	-	

PME Control – RW - 32 bits - [PCI_Reg:C0h]			
Field Name	**Bits**	**Default**	**Description**
Cap_ID	7:0	01h	Read only. A value of 01h identifies the linked list item as being the PCI Power Management registers.
Next ItemPointer	15:8	D0h	Read only. This field provides an offset into the function's PCI Configuration Space, pointing to the location of next item in the function's capability list. If there are no additional items in the Capabilities List, this register is set to 00h.

PME Control – RW - 32 bits - [PCI_Reg:C0h]			
Field Name	**Bits**	**Default**	**Description**
Version	18:16	010b	Read only. A value of 010b indicates that this function complies with Revision 1.1 of the PCI Power Management Interface Specification.
PME clock	19	0b	Read only. When this bit is a 0, it indicates that no PCI clock is required for the function to generate PME#.
Reserved	20		Reserved
DSI	21	0b	Read only. This Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it.
Aux_Current	24:22	000b	Read only. This 3 bit field reports the 3.3V auxiliary current requirements for the PCI function. If the Data Register has been implemented by this function, then: - Reads of this field must return a value of 000b. - The Data Register takes precedence over this field for 3.3V auxiliary current requirement reporting.
D1_Support	25	1b	If this bit is a 1, this function supports the D1. Power Management State.
D2_Support	26	1b	If this bit is a 1, this function supports the D2. Power Management State.
PME_Support	31:27	0Fh	Read only. This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit [31] 1XXXXb - PME# can be asserted from D3cold Bit [30] X1XXXb - PME# can be asserted from $D3_{hot}$ Bit [29] XX1XXb - PME# can be asserted from D2 Bit [28] XXX1Xb - PME# can be asserted from D1 Bit [27] XXXX1b - PME# can be asserted from D0

PME Data / Status – RW - 32 bits - [PCI_Reg:C4h]			
Field Name	**Bits**	**Default**	**Description**
PowerState	1:0	00b	This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given by: 00b: D0 01b: D1 10b: D2 11b: $D3_{hot}$ If software attempts to write an unsupported, optional state to this field, the write operation must be completed normally on the bus; however, the data is discarded and no state change occurs.
Reserved	7:2		Reserved
PME_En	8	0b	A 1 enables the function to assert PME#. When 0, PME# assertion is disabled. This bit defaults to 0 if the function does not support PME# generation from $D3_{cold}$.
Data_Select	12:9	0000b	This 4-bit field is used to select which data is to be reported through the Data register and Data_Scale field.
Data_Scale	14:13	00b	This 2-bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field will vary depending on which data value has been selected by the Data_Select field.
PME_Status	15	0b	This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit.
Reserved	21:16		Reserved
B2_B3#	22	1b	Read only. The state of this bit determines the action that is to occur as a direct result of programming the function to $D3_{hot}$. A 1 indicates that when the bridge function is programmed to $D3_{hot}$, its secondary bus's PCI clock will be stopped (B2).
BPCC_En	23	0b	Read only. A 0 indicates that the bus power/clock control policies are disabled. When the Bus Power/Clock Control mechanism is disabled, the bridge's PMCSR PowerState field cannot be used by the system software to control the power or clock of the bridge's secondary bus.
Data	31:24	00h	Read only. This field is used to report the state dependent data requested by the Data_Select field. The value of this field is scaled by the value reported by the Data_Scale field.

MSI Control – RW - 32 bits - [PCI_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
MSI USB	7:0	05h	MSI USB ID. Read only.
Next Item Pointer	15:8	E4h	Pointer to next capability structure
MSI Control Out	16	0b	Set to 1 to disable IRQ. Use MSI instead.
Reserved	19:17	000b	Reserved
MSI Control	22:20	000b	MSI control field
64-bit Address Capable	23	0b	Read only. If EHCI is in 64-bit address mode, as specified by 64-bit Addressing Capability bit in HCCPARAMS [MEM Reg:08h], then this bit is set to 1 indicating that EHCI is capable of generating a 64-bit message address; otherwise, it is set to 0 indicating the EHCI is not capable of generating a 64-bit address.
Reserved	31:24	00h	Reserved

MSI Address – RW - 32 bits - [PCI_Reg : D4h]			
Field Name	**Bits**	**Default**	**Description**
MSI Address	31:0	0h	System-specified message address.

MSI Upper Address – RW - 32 bits - [PCI_Reg:D8h]			
Field Name	**Bits**	**Default**	**Description**
MSI Upper Address *	31:0	0h	If the Message Enable bit (bit 0 of the Message Control register) is set, the contents of this register (if non-zero) specify the upper 32-bits of a 64-bit message address (AD[63:32]). If the contents of this register are zero, the device uses the 32-bit address specified by the message address register.

*** Note**: If EHCI is in 64-bit address mode, as specified by 64-bit Addressing Capability bit in HCCPARAMS [MEM Reg:08h], then xD8 contains the higher 32 bits of the MSI Address and xDC contains the MSI Data; otherwise, xD8 contains MSI Data.

MSI Data – RW - 16 bits - [PCI_Reg:D8h/DCh]			
Field Name	**Bits**	**Default**	**Description**
MSI Data *	15:0	0h	System-specified message

*** Note:** If EHCI is in 64-bit address mode, as specified by 64-bit Addressing Capability bit in HCCPARAMS [MEM Reg:08h], then xD8 contains the higher 32 bits of the MSI Address and xDC contains the MSI Data; otherwise xD8 contains MSI Data.

DBUG_PRT Control – RO - 32 bits - [PCI_Reg:E4h]			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0Ah	The value of 0Ah in this field identifies that the function supports a Debug Port.
Next Item Pointer	15:8	00h	Pointer to next capability structure
Offset	28:16	0E0h	This 12 bit field indicates the byte offset (up to 4K) within the BAR indicated by the BAR# field. This offset is required to be DWORD aligned and therefore bits 16 and 17 are always zero.

DBUG_PRT Control – RO - 32 bits - [PCI_Reg:E4h]			
Field Name	**Bits**	**Default**	**Description**
BAR#	31:29	1h	Indicates which one of the possible 6 Base Address Register offsets contains the Debug Port registers. For example, a value of 1h indicates the first BAR (offset 10h), while a value of 5 indicates that the BAR is at 20h. This offset is independent of whether the BAR is 32 or 64 bit. For example, if the offset were 3 indicating that the BAR at offset 18h contains the Debug Port, BARs at offset 10h and 14h may or may not be implemented. This field is read only and only values 1-6h are valid. (A 64-bit BAR is allowed.) Only a memory BAR is allowed.

Reserved – RO - 32 bits - [PCI_Reg:F0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RO - 32 bits - [PCI_Reg:F4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

USBLEGSUP – RW - 32 bits - [PCI_Reg:EECP+00h] *			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	01h	This field identifies the extended capability. A value of 01h identifies the capability as Legacy Support. This extended capability requires one additional 32-bit register for control/status information, and this register is located at offset EECP+04h. Read Only.
Next EHCI Extended Capability Pointer	15:8	00h	This field points to the PCI configuration space offset of the next extended capability pointer. A value of 00h indicates the end of the extended capability list. Read Only.
HC BIOS Owned Semaphore	16	0b	The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will set this bit to a 0 in response to a request for ownership of the EHCI controller by system software.
Reserved	23:17		These bits are reserved and must be set to 0.
HC OS Owned Semaphore	24	0b	System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as 0.
Reserved	31:25		These bits are reserved and must be set to 0.

***Note:** EECP is defined in HCCPARAMS[15:8] (EHCI MEM x08) and is hard-wired to xA0.

USBLEGCTLSTS – RW - 32 bits - [PCI_Reg:EECP+04h] *			
Field Name	**Bits**	**Default**	**Description**

USBLEGCTLSTS – RW - 32 bits - [PCI_Reg:EECP+04h] *			
Field Name	**Bits**	**Default**	**Description**
USB SMI Enable	0	0b	When this bit is a 1, and the SMI on USB Complete bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on USB Error Enable	1	0b	When this bit is a 1, and the SMI on USB Error bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on Port Change Enable	2	0b	When this bit is a 1, and the SMI on Port Change Detect bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on Frame List Rollover Enable R/W	3	0b	When this bit is a 1, and the SMI on Frame List Rollover bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on Host System Error Enable	4	0b	When this bit is a 1, and the SMI on Host System Error bit in this register is a 1, the host controller will issue an SMI immediately.
SMI on Async Advance Enable	5	0b	When this bit is a 1, and the SMI on Async Advance bit in this register is a 1, the host controller will issue an SMI immediately.
Reserved.	12:6		These bits are reserved and must be set to 0.
SMI on OS Ownership Enable	13	0b	When this bit is a 1 and the SMI on OS Ownership Change bit in this register is 1, the host controller will issue an SMI.
SMI on PCI Command Enable	14	0b	When this bit is 1 and SMI on PCI Command in this register is 1, then the host controller will issue an SMI.
SMI on BAR Enable	15	0b	When this bit is 1 and SMI on BAR is 1, then the host controller will issue an SMI.
SMI on USB Complete	16	0b	Shadow bit of USB Interrupt (USBINT) bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the USB Interrupt bit in the USBSTS register. Read Only.
SMI on USB Error	17	0b	Shadow bit of USB Error Interrupt (USBERRINT) bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the USB Error Interrupt bit in the USBSTS register. Read Only.
SMI on Port Change Detect.	18	0b	Shadow bit of Port Change Detect bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the Port Change Detect bit in the USBSTS register. Read Only.
SMI on Frame List Rollover	19	0b	Shadow bit of Frame List Rollover bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the Frame List Rollover bit in the USBSTS register. Read Only.
SMI on Host System Error	20	0b	Shadow bit of Host System Error bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the Host System Error bit in the USBSTS register. Read Only.
SMI on Async Advance	21	0b	Shadow bit of the Interrupt on Async Advance bit in the USBSTS register. To set this bit to a 0, system software must write a 1 to the Interrupt on Async Advance bit in the USBSTS register. Read Only.
Reserved.	28:22		These bits are reserved and must be set to 0.
SMI on OS Ownership Change	29	0b	This bit is set to 1 whenever the HC OS Owned Semaphore bit in the USBLEGSUP register transitions from 1 to 0 or 0 to 1.
SMI on PCI Command	30	0b	This bit is set to 1 whenever the PCI Command Register is written.
SMI on BAR R/WC	31	0b	This bit is set to 1 whenever the Base Address Register (BAR) is written.

USBLEGCTLSTS – RW - 32 bits - [PCI_Reg:EECP+04h] *			
Field Name	**Bits**	**Default**	**Description**

*** Note:** EECP is defined in HCCPARAMS[15:8] (EHCI MEM x08) and is hard-wired to xA0.

2.2.6 USB1/USB2/USB3 (Device-18/19/22, func-2) EHCI Memory Mapped Registers

2.2.6.1 EHCI Capability Registers

This block of registers is memory-mapped. Access address is equal to the offset address plus the base address defined in BAR[PCI_Reg:10h].

Registers Name	Offset Address
Capability Register Length - CAPLENGTH	00h
Reserved	01h
Host Controller Interface Version – HCIVERSION	02h
Structural Parameters – HCSPARAMS	04h
Capability Parameters - HCCPARMAS	08h
Reserved	0Ch

CAPLENGTH – R - 8 bits - [MEM_Reg:00h]
Description
This register is used as an offset to add to the register base to find the beginning of the Operational Register Space. Default value = 20h.

HCIVERSION – R - 16 bits - [MEM_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
HCIVERSION	15:0	0100h	This is a two-byte register containing a BCD encoding of the version number of interface to which this host controller interface conforms.

HCSPARAMS – R - 32 bits - [MEM_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
N_PORTS	3:0	5h/4h[1]	This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1H to FH. A 0 in this field is undefined.
Port Power Control (PPC)	4	0b	This field indicates whether the host controller implementation includes port power control. A 1 in this bit indicates the ports have port power switches. A 0 in this bit indicates the port does not have port power switches. The value of this field affects the functionality of the Port Power field in each port status and control register.
Reserved	6:5		These bits are reserved and should be set to 0.

HCSPARAMS – R - 32 bits - [MEM_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
Port Routing Rules	7	0b	This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: 0 = The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. 1 = The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTROUTE array.
Number of Ports per Companion Controller (N_PCC)	11:8	5h/4h*	This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software. For example, if N_PORTS has a value of 6 and N_CC has a value of 2, then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, etc. In the previous example, the N_PCC could have been 4, where the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with N_PORTS and N_CC.
Number of Companion Controller (N_CC)	15:12	1h	This field indicates the number of companion controllers associated with this USB 2.0 host controller. A 0 in this field indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. A value larger than 0 in this field indicates there are companion USB 1.1 host controller(s). Port-ownership hand-offs are supported. High-, Full- and Low-speed devices are supported on the host controller root ports.
Port Indicators (P_INDICATOR)	16	0b	This bit indicates whether the ports support port indicator control. When this bit is a 1, the port status and control registers include a read/writeable field for controlling the state of the port indicator.
Reserved	19:17		These bits are reserved and should be set to 0.
Debug Port Number	23:20	1h	Optional. This register identifies which of the host controller ports is the debug port. The value is the port number (one-based) of the debug port. A non-zero value in this field indicates the presence of a debug port. The value in this register must not be greater than N_PORTS.
Reserved	31:24		These bits are reserved and should be set to 0.

***Note:** USB1 and USB2 support 5 ports each; USB3 supports 4 ports.

HCCPARAMS – R - 32 bits - [MEM_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
64-bit Addressing Capability	0	0b	This field documents the addressing range capability of this implementation. 0: Data structures using 32-bit address memory pointers 1: Data structures using 64-bit address memory pointers
Programmable Frame List Flag	1	1b	If this bit is set to 0, then system software must use a frame list length of 1024 elements with this host controller. The Frame List Size field of the USBCMD register is read-only and should be set to 0. If set to 1, then system software can specify and use a smaller frame list and configure the host controller via the Frame List Size field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
Asynchronous Schedule Park Capability	2	1b	If this bit is set to 1, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
Reserved	3		These bits are reserved and should be set to 0.
Isochronous Scheduling Threshold	7:4	1h	This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit [7] is 0, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures (one or more) before flushing the state. When bit [7] is 1, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
EHCI Extended Capabilities Pointer (EECP)	15:8	A0h	This optional field indicates the existence of a capabilities list. A value of 00h indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain the consistency of the PCI header defined for this class of device.
Reserved	31:16		These bits are reserved and should be set to 0.

Reserved – R – 60 bits - [MEM_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	59:0	-	

2.2.6.2 EHCI Operational Registers

EHCI Memory Map Registers: Host Controller Operational Registers (EHCI_EOR 0x00 ~ 0xCC)

This block of registers is memory-mapped. The base offset, EHCI_EOR, is defined in CAPLENGTH register (MEM_Reg:00h, default value = 20h).

Registers Name	Offset Address
USB Command – USBCMD	EHCI_EOR + 00h
USB Status – USBSTS	EHCI_EOR + 04h
USB Interrupt Enable – USBINTR	EHCI_EOR + 08h
USB Frame Index – FRINDEX	EHCI_EOR + 0Ch
4G Segment Selector – CTRLDSSEGMENT	EHCI_EOR + 10h
Frame List Base Address – PERIODICLISTBASE	EHCI_EOR + 14h
Next Asynchronous List Address – ASYNCLISTADDR	EHCI_EOR + 18h
Reserved	EHCI_EOR + (1Ch~3Fh)
Configured Flag – CONFIGFLAG	EHCI_EOR + 40h
Port Status/Control – PORTSC (1-N_PORTS)	EHCI_EOR + (44h~54h)
Reserved	EHCI_EOR + 80h
Packet Buffer Threshold Values	EHCI_EOR + 84h
USB PHY Status 0	EHCI_EOR + 88h
USB PHY Status 1	EHCI_EOR + 8Ch
Reserved	EHCI_EOR + 90h
UTMI Control	EHCI_EOR + 94h
Loopback Test	EHCI_EOR + 98h
EOR MISC Control	EHCI_EOR + 9Ch
USB Phy Calibration	EHCI_EOR + A0h
USB Common PHY Control	EHCI_EOR + A4h
Reserved	EHCI_EOR + A8h
Reserved	EHCI_EOR + ACh
USB Debug Port	0E0h~0F0h*

*** Note:** The base offset of Debug Port registers is defined directly in DBUG_PRT Control register (EHCI_PCI_CFGxE4[28:16]), regardless of the value in CAPLENGTH register (MEM_Reg:00h), so range is equivalent to EHCI_EOR + (C0h~D0h).

USBCMD – RW - 32 bits - [EOR_Reg:EHCI_EOR+00h]			
Field Name	**Bits**	**Default**	**Description**
Run/Stop (RS)	0	0b	1: Run 0: Stop. When set to 1, the Host Controller proceeds with execution of the schedule. The Host Controller continues execution as long as this bit is set to 1. When this bit is set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears the Run bit. The HC Halted bit in the status register indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a 1 to this field unless the host controller is in the Halted state (i.e. HCHalted in the USBSTS register is a one). Doing so will yield undefined results.

USBCMD – RW - 32 bits - [EOR_Reg:EHCI_EOR+00h]			
Field Name	**Bits**	**Default**	**Description**
Host Controller Reset (HCRESET)	1	0b	This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a 1 to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller in order to return the host controller to an operational state. This bit is set to 0 by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this register. Software should not set this bit to a 1 when the HCHalted bit in the USBSTS register is a 0. Attempting to reset an actively running host controller will result in undefined behavior.
Frame List Size	3:2	00b	This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to 1. This field specifies the size of the frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean: 00b: 1024 elements (4096 bytes) 01b: 512 elements (2048 bytes) 10b: 256 elements (1024 bytes) – for resource-constrained environments 11b: Reserved [Read/Write or Read-only]
Periodic Schedule Enable	4	0b	This bit controls whether the host controller skips processing the Periodic Schedule. 0: Do not process the Periodic Schedule 1: Use the PERIODICLISTBASE register to access the Periodic Schedule.
Asynchronous Schedule Enable	5	0b	This bit controls whether the host controller skips processing the Asynchronous Schedule. 0b: Do not process the Asynchronous Schedule 1b: Use the ASYNCLISTADDR register to access Asynchronous Schedule.
Interrupt on Async Advance Doorbell	6	0b	This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to *ring* the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS register. If the Interrupt on Async Advance Enable bit in the USBINTR register is 1 then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to 0 after it has set the Interrupt on Async Advance status bit in the USBSTS register to 1. Software should not write a 1 to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.
Light Host Controller Reset (Optional)	7	0b	This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or the relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to 0 (retaining port ownership relationships). A host software read of this bit as 0 indicates the Light Host Controller Reset has completed and it is safe for host software to re-initialize the host controller. A host software read of this bit as a 1 indicates the Light Host Controller Reset has not yet completed. If not implemented, a read of this field will always return 0.

USBCMD – RW - 32 bits - [EOR_Reg:EHCI_EOR+00h]			
Field Name	**Bits**	**Default**	**Description**
Asynchronous Schedule Park Mode Count (Optional)	9:8	11b	If the Asynchronous Park Capability bit in the HCCPARAMS register is a 1, then this field defaults to 3h and is R/W. Otherwise it defaults to 0 and is read only. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 1h to 3h. Software must not write a 0 to this bit when Park Mode Enable is a 1, as this will result in undefined behavior. [Read/Write or Read-only]
Reserved	10		This bit is reserved and should be set to 0.
Asynchronous Schedule Park Mode Enable (Optional)	11	1b	If the Asynchronous Park Capability bit in the HCCPARAMS register is a 1, then this bit defaults to a 1h and is R/W. Otherwise the bit must be a 0 and is read-only. Software uses this bit to enable or disable Park mode. When this bit is 1, Park mode is enabled. When this bit is 0, Park mode is disabled. [Read/Write or Read-only]
Reserved	15:12		This bit is reserved and should be set to 0.
Interrupt Threshold Control	23:16	08h	This field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. 00h: Reserved 01h: 1 micro-frame 02h: 2 micro-frames 04h: 4 micro-frames 08h: 8 micro-frames (default, equates to 1 ms) 10h: 16 micro-frames (2 ms) 20h: 32 micro-frames (4 ms) 40h: 64 micro-frames (8 ms) Any other value in this register yields undefined results. Software modifications to this bit while HCHalted bit is equal to 0 results in undefined behavior.
Reserved	31:24		These bits are reserved and should be set to 0s.

USBSTS - RW - 32 bits - [EOR_Reg:EHCI_EOR+04h]			
Field Name	**Bits**	**Default**	**Description**
USBINT	0	0b	USB Interrupt. The host controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).
USBERRINT	1	0b	USB Error Interrupt. The host controller sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and the USBINT bit are set.

USBSTS - RW - 32 bits - [EOR_Reg:EHCI_EOR+04h]			
Field Name	**Bits**	**Default**	**Description**
Port Change Detect	2	0b	The host controller sets this bit to 1 when any port for which the Port Owner bit is set to 0 (see PORTSC, EHCI_EOR+(44h~54h)) has a change bit transition from a 0 to a 1 or a Force Port Resume bit transition from a 0 to a 1 as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Change being set to a 1 after system software has relinquished ownership of a connected port by writing a 0 to a port's Port Owner bit. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, over-current change, enable/disable change and connect status change).
Frame List Rollover	3	0b	The host controller sets this bit to a 1 when the Frame List Index rolls over from its maximum value to 0. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the Frame List Size field of the USBCMD register) is 1024, the Frame Index Register rolls over every time FRINDEX[13] toggles. Similarly, if the size is 512, the host controller sets this bit to a 1 every time FRINDEX[12] toggles.
Host System Error	4	0b	The host controller sets this bit to 1 when a serious error occurs during a host system access involving the host controller module. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the host controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
Interrupt on Async Advance	5	0b	System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
Reserved	11:6		These bits are reserved and should be set to 0.
HCHalted	12	1b	This bit is a 0 whenever the Run/Stop bit is a 1. The host controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the host controller hardware (e.g. internal error). [Read-only]
Reclamation	13	0b	This is a read-only status bit, which is used to detect an empty asynchronous schedule. [Read-only]

USBSTS - RW - 32 bits - [EOR_Reg:EHCI_EOR+04h]			
Field Name	**Bits**	**Default**	**Description**
Periodic Schedule Status	14	0b	The bit reports the current real status of the Periodic Schedule. If this bit is a 0, then the status of the Periodic Schedule is disabled. If this bit is a 1, then the status of the Periodic Schedule is enabled. The host controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, Periodic Schedule is either enabled (1) or disabled (0). [Read-only]
Asynchronous Schedule Status	15	0b	The bit reports the current real status of the Asynchronous Schedule. If this bit is a 0, then the status of the Asynchronous Schedule is disabled. If this bit is a 1, then the status of the Asynchronous Schedule is enabled. The host controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0). [Read-only]
Reserved	31:16		These bits are reserved and should be set to 0.

USBINTR –RW - 32 bits - [EOR_Reg:EHCI_EOR+08h]			
Field Name	**Bits**	**Default**	**Description**
USB Interrupt Enable	0	0b	When this bit is a 1, and the USBINT bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.
USB Error Interrupt Enable	1	0b	When this bit is a 1, and the USBERRINT bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
Port Change Interrupt Enable	2	0b	When this bit is a 1, and the Port Change Detect bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
Frame List Rollover Enable	3	0b	When this bit is a 1, and the Frame List Rollover bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
Host System Error Enable	4	0b	When this bit is a 1, and the Host System Error Status bit in the USBSTS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
Interrupt on Async Advance Enable	5	0b	When this bit is a 1, and the Interrupt on Async Advance bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
Reserved	31:6		These bits are reserved and should be 0

FRINDEX –RW - 32 bits - [EOR_Reg:EHCI_EOR+0Ch]			
Field Name	**Bits**	**Default**	**Description**
Frame Index	13:0	0h	When this bit is a 1, and the Interrupt on Async Advance bit in the USBSTS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
Reserved	31:14		These bits are reserved and should be 0

CTRLDSSEGMENT –RW - 32 bits - [EOR_Reg:EHCI_EOR+10h]			
Field Name	**Bits**	**Default**	**Description**
CTRLDSSEGMENT	31:0	0h	This 32-bit register corresponds to the most significant address bits [63:32] for all EHCI data structures. If the 64-bit Addressing Capability field in HCCPARAMS is a 0, then this register is not used. Software cannot write to it and a read from this register will return 0s. If the 64-bit Addressing Capability field in HCCPARAMS is a 1, then this register is used with the link pointers to construct 64-bit addresses to EHCI control data structures. This register is concatenated with the link pointer from either PERIODICLISTBASE, or ASYNCLISTADDR, or any control data structure link field to construct a 64-bit address. This register allows the host software to locate all control data structures within the same 4 Gigabyte memory segment.

PERIODICLISTBASE –RW - 32 bits - [EOR_Reg:EHCI_EOR+14h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	11:0		These bits are reserved. Must be written as 0s. During runtime, the values of these bits are undefined.
Base Address	31:12	000h	These bits correspond to memory address signals [31:12], respectively.

ASYNCLISTADDR –RW - 32 bits - [EOR_Reg:EHCI_EOR+18h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	4:0		These bits are reserved and their value has no effect on operation.
Link Pointer Low (LPL)	31:5	00h	These bits correspond to memory address signals [31:5], respectively. This field may only reference a Queue Head (QH).

CONFIGFLAG –RW - 32 bits - [EOR_Reg:EHCI_EOR+40h]			
Field Name	**Bits**	**Default**	**Description**
Configure Flag (CF)	0	0b	Host software sets this bit as the last action in its process of configuring the host controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below: 0: Port routing control logic default-routes each port to an implementation dependent classic host controller. 1: Port routing control logic default-routes all ports to this host controller.
Reserved	31:1		These bits are reserved and should be set to 0.

PORTSC (1-N_PORTS) –RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Current Connect Status	0	0b	1: Device is present on port. 0: No device is present. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (bit 1) to be set. This field is 0 if Port Power is 0. [Read-only]
Connect Status Change	1	0b	1: Change in Current Connect Status. 0: No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. This field is 0 if Port Power is 0.
Port Enabled/Disabled	2	0b	1: Enable. 0: Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this field. The host controller will only set this bit to a 1 when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled (0b), downstream propagation of data is blocked on this port, except for reset. This field is 0 if Port Power is 0.
Port Enable/Disable Change	3	0b	1: Port enabled/disabled status has changed. 0: No change. For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2. Software clears this bit by writing a 1 to it. This field is 0 if Port Power is 0.
Over-current Active	4	0b	1: This port currently has an over-current condition. 0: This port does not have an over-current condition. This bit will automatically transition from a 1 to a 0 when the overcurrent condition is removed.

PORTSC (1-N_PORTS) –RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Force Port Resume	6	0b	1: Resume detected/driven on port. 0: No resume (K-state) detected/driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a 1) and software transitions this bit to a 1, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a 1 because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a 1. If software sets this bit to a 1, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a 1. Software must appropriately time the Resume and set this bit to a 0 when the appropriate amount of time has elapsed. Writing a 0 (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a 1 until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a 0. This field is 0 if Port Power is 0.
Suspend	7	0b	1: Port in suspend state. 0: Port not in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: **Bits [Port Enabled, Suspend]** **Port State** 0X Disable 10 Enable 11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of 0 to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a 0 when: - Software sets the Force Port Resume bit to a 0 (from a 1). - Software sets the Port Reset bit to a 1 (from a 0). If host software sets this bit to a 1 when the port is not enabled (i.e. Port Enabled bit is a 0) the results are undefined. This field is 0 if Port Power is 0.

PORTSC (1-N_PORTS) –RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Port Reset	8	0b	1: Port is in Reset. 0: Port is not in Reset. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Note: when software writes this bit to a 1, it must also write a 0 to the Port Enable bit. Note that when software writes a 0 to this bit there may be a delay before the bit status changes to a 0. The bit status will not read as a 0 until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the *Port Enable* bit to a 1). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a 1 to a 0. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a 0. The HCHalted bit in the USBSTS register should be a 0 before software attempts to use this bit. The host controller may hold Port Reset asserted to a 1 when the HCHalted bit is a 1. This field is 0 if Port Power is 0.
Reserved	9		This bit is reserved for future use, and should return a value of 0 when read.
Line Status	11:10		These bits reflect the current logical levels of the D+ (bit [11]) and D- (bit [10]) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is 0 and the current connect status bit is set to 1. The encoding of the bits are: **Bits[11:10] USB State Interpretation** 00b SE0 Not Low-speed device, perform EHCI reset 10b J-state Not Low-speed device, perform EHCI reset 01b K-state Low-speed device, release ownership of port 11b Undefined Not Low-speed device, perform EHCI reset. This value of this field is undefined if Port Power is 0. [Read-only]

PORTSC (1-N_PORTS) –RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Port Power	12		The function of this bit depends on the value of the Port Power Control (PPC) field in the HCSPARAMS register. The behavior is as follows: **PPC PP Operation** 0b 1b RO - Host controller does not have port power control switches. Each port is hard-wired to power. 1b 1b/0b RW - Host controller has port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (i.e., PP = 0), the port is non-functional and will not report attaches, detaches, etc. When an over-current condition is detected on a powered port and PPC = 1, the PP bit in each affected port may be transitioned by the host controller from 1 to 0 (removing power from the port). [Read-write or Read-only]
Port Owner	13	1b	This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is 0. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a 1 to this bit when the attached device is not a high-speed device. A 1 in this bit means that a companion host controller owns and controls the port.

PORTSC (1-N_PORTS) –RW - 32 bits - [EOR_Reg:EHCI_EOR+(44h~54h)]			
Field Name	**Bits**	**Default**	**Description**
Port Indicator Control	15:14	00b	Writing to this bit has no effect if the P_INDICATOR bit in the HCSPARAMS register is 0. If P_INDICATOR is 1, then the bit encodings are as follows: **Bit Value Meaning** 00b Port indicators are off 01b Amber 10b Green 11b Undefined Refer to the USB Specification Revision 2.0 for a description on how these bits are to be used. This field is 0 if Port Power is 0.
Port Test Control	19:16	0000b	When this field is 0, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are as follows: **Bits Test Mode** 0000b Test mode not enabled 0001b Test J_STATE 0010b Test K_STATE 0011b Test SE0_NAK 0100b Test Packet 0101b Test FORCE_ENABLE 0110b - 1111b are reserved
Wake on Connect Enable	20	0	Writing this bit to a 1 enables the port to be sensitive to device connects as wake-up events. This field is 0 if Port Power is 0.
Wake on Disconnect Enable	21	0b	Writing this bit to a 1 enables the port to be sensitive to device disconnects as wake-up events. This field is 0 if Port Power is 0.
Wake on Over-current Enable	22	0b	Writing this bit to a 1 enables the port to be sensitive to over-current conditions as wake-up events. This field is 0 if Port Power is 0.
Reserved	31:23		Reserved

Reserved – RW - 32 bits - [EOR_Reg: EHCI_EOR+80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	Reserved

Packet Buffer Threshold Values – RW - 32 bits - [EOR_Reg:EHCI_EOR+84h]			
Field Name	**Bits**	**Default**	**Description**
IN Threshold	7:0	10h	The PCI transaction starts when threshold of internal FIFO for receive packet is reached. The value represents multiple of 8 bytes – 10h means 128 bytes. The smallest acceptable value is 08h (64 bytes).
Reserved	15:8		Reserved
OUT Threshold	23:16	40h	The transmit packet starts at UTMI interface when threshold of internal FIFO for transmit packet is reached. The value represents multiple of 8 bytes – 10h means 128 bytes. The smallest acceptable value is 08h (64 bytes).
Reserved	31:24		Reserved

USB PHY Status 0 – RW - 32 bits - [EOR_Reg:EHCI_EOR+88h]			
Field Name	**Bits**	**Default**	**Description**
PORT0_PHYStatus	7:0	00h	Read only. PHY Status of Port0
PORT1_PHYStatus	15:8	00h	Read only. PHY Status of Port1
PORT2_PHYStatus	23:16	00h	Read only. PHY Status of Port2
PORT3_PHYStatus	31:24	00h	Read only. PHY Status of Port3

Note: Use the VControlModeSel (UTMI_Control register[7]) to select which group of status should be read back.

USB PHY Status 1 – RW - 32 bits - [EOR_Reg:EHCI_EOR+8Ch]			
Field Name	**Bits**	**Default**	**Description**
PORT4_PHYStatus	7:0	00h	Read only. PHY Status of Port4 *
Reserved	31:8	-	Reserved

*** Note:** This register does not exist in USB3, as USB3 has 4 ports only.

Reserved – RW - 32 bits - [EOR_Reg: EHCI_EOR+90h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	Reserved

UTMI Control – RW - 32 bits - [EOR_Reg:EHCI_EOR+94h]			
Field Name	**Bits**	**Default**	**Description**
VControl	6:0	21h	Control PHY setting **Group-0** (VControlModeSel=0) VControl[6:0] = { CLKOff_disable, DUTYADJ[2:0], HSADJ[2:0]} - HSADJ : HS TX current adjustment – default 001b. Bit 0 adds 5% when set to “1” Bit 1 adds 10% when set to “1” Bit 2 adds 10% when set to “1” We’ll have 000 : 0% **001 : 5%** 010 : 10% 011 : 15%

UTMI Control – RW - 32 bits - [EOR_Reg:EHCI_EOR+94h]			
Field Name	**Bits**	**Default**	**Description**
			100 : 10% 101 : 15% 110 : 20% 111 : 25% - DUTYADJ: adjust clk480 (in analog PHY) duty cycle – default 100b. 000 +8% 001 +3% 010 +5% 011 +2% **100 +1%** 101 -1% 110 -1.6% 111 -5.5% - CLKOFF_disable : to disable UTMICLK gate off function **Group-1** (VControlModeSel =1) VControl[6:0] = {TESTMODE[3:0]} TESTMODE[3:0] Description 0000 Disable Test Mode 0001~ 0111 Enable Analog PHY Test mode, TMODE1 ~ TMODE7 1000 Enable Analog loop back 1001 Enable digital loop back 1110 ~ 1111 Reserved
VControlModeSel	7	0b	The PHY control modes are divided into 2 groups. VcontrolModeSel is used to select the group.
Reserved	11:8		Reserved
VLoadB	12	1b	Update PHY control mode (active load) 0: load the new VControl value to PHY/common block 1: only VControlModeSel value to PHY will be updated for selecting different PHY status group (see PHY status registers, EOR_Reg x88 ~ x90). But VControl[6:0] value inside PHY won't get affected.
Port Number	16:13	0h	Select the corresponding port PHY or common block to load the VControl bits. 0000: port0 0001: port1 0010: port2 …… 0100: port4 0101 ~ 1110: Reserved , no effect 1111: Common block
VBusy	17	0b	Read Only – To block software write to bits[16:8] when port router is updating the field.
Reserved	31:18		Reserved

Loopback Test – RW - 32 bits - [EOR_Reg:EHCI_EOR+98h]			
Field Name	**Bits**	**Default**	**Description**
Received Packet Count	3:0	0h	RX data packet count. This counter defines the number (in power of 16) of RX data packet that should be checked for the loop back test.
Reserved	7:4		Reserved
Enable Loop Back Test	8	0b	Enable external USB port loopback test. The loopback test is to set one port to TX mode (Test Packet mode) and one port to RX mode (Test SE0_NAK). Refer to PORTSC [19:16] for information on the tests.
Loopback Test Status	9	0b	Read Only. 0: CRC error on loopback receiving data 1: Good CRC on loopback receiving data
Loopback Test Done	10	0b	Read Only. Indicates loopback test is done.
Reserved	11	-	Reserved
Good Received Packet Count	19:12	-	Read-Only. The number of good packets that the host controller received during the loopback test mode. These bits will be cleared by clearing bit[8] (Enable Loop Back test).
Enable PHY PowerUp State Checking	20	0b	Enable auto-checking on PHY Power Up State. There is built-in logic to check the PHY default Power Up state to detect manufacturing defects in the PHY macro.
Status of ports for PowerUp State Check	26:21	000000b	Read Only. Status bit to indicate the Power Up state auto-checking result from the individual port. Each bit maps to a corresponding port, from port-0 to port-5, i.e. bit-21 for port-0, bit-22 for port-1, and so on. The value can only be checked when the PHY PowerUp State Checking Done bit is set. 0: PHY Power Up State checking is fail. 1: PHY Power Up State checking is good.
Reserved	31:27	-	Reserved

EOR MISC Control – RW - 32 bits - [EOR_Reg : EHCI_EOR + 9Ch]			
Field Name	**Bits**	**Default**	**Description**
Enable Interrupt on ForcePortResume	0	0b	Enable host controller to generate interrupt on software clear ForcePortResume bit in PORTSC[6].
Interrupt route Control on ForcePortResume	1	0h	Report interrupt status to either USBINT bit or Port Change Detect bit in the USBSTS register on software clear “ForcePortResume” bit. This bit only takes effect when the Enable Interrupt on ForcePortResume bit is set. 0: Report interrupt on USBINT bit in USBSTS register 1: Report interrupt on Port Change Detect bit in USBSTS register
Reserved	3:2	-	Reserved
Inter-packet Gap Adjust Counter	7:4	4h	Counter used to adjust the inter-packet gap for test packet.
Reserved	10:8	-	Reserved
Disable uFrame Babble detection	11	0b	Set to 1 to disable uFrame Babble detection in EHCI controllers. Hardware default is uFrame Babble detection enabled.
EHCI Power Saving Enable	12	1b	Enable power saving clock gating. When enabled, dynamic clock gating is enabled when EHCI is not in operational mode. The clock going to all memory modules will be gated off. Blink clock also gets gated off unless the connection interrupt is detected.
Reserved	23:13	0h	Reserved
Force Txdata [7:0]	31:24	00h	Used to force txdata[7:0] when the port is in TEST_K mode. This can be used to force PHY to generate a desired output pattern for PHY debugging and characterization purposes.

USB Common PHY CAL & Control Register – RW - 32 bits - [EOR_Reg:EHCI_EOR+A0h]			
Field Name	**Bits**	**Default**	**Description**
ComCalBus	6:0		Read Only. Calibration bus value from PHY before adjustment. Default value = Don't care.
Reserved	7	0b	Reserved
NewCalBus	15:8	00h	New calibration bus signed value.
UseCommonCalibration	16	0b	If set, the PHY's calibration value in bits[6:0] is returned to the PHY ports. If cleared, the value after adjustment is returned to the PHY ports.
AddToCommonCalibration	17	1b	If set, the signed NewCalBus is added to the ComCalBus and returned to the PHY ports. Any overflow is clamped to all 1s. Any underflow is clamped to all 0s. If cleared, the signed NewCalBus replaces the ComCalBus and returns to the PHY ports.
Reserved	23:18	0000h	Read as 0.
CommonPhyCalBus	30:24	7Fh	Read Only. Phy Common Calibration Bus
Reserved	31	0b	

Note:

1. The equation for the calibration resistor value is

   Rcal = 1/ [1/59.4 + CalValue/(1.05*3.8k ohm)]

   where CalValue is the final 7 bits of calibration setting sent to PHY.
2. The total termination resistance value for HS USB D+/D- should include another 5 ohm resistance from the FS driver.

USB Common PHY Control – RW - 32 bits - [EOR_Reg:EHCI_EOR+A4h]			
Field Name	**Bits**	**Default**	**Description**
CPADJ *****	3:0	4h	Charge Pump setting for common block PLL.
XREFADJ *****	7:4	1h	External reference bias adjustment for common block.
IREFADJ *****	11:8	1h	Internal reference bias adjustment for common block.
PVI *****	15:12	2h	PLL V-I Converter Control for common block PLL.
DUTYADJ *****	19:16	4h	CLK480 duty cycle control from 40-60% to 60-40%.
PLL Bypass	20	0b	Enable USB Common PLL bypass
Reserved	23:21	0h	Reserved
DLL Control	31:24	A0h	USB PHY DLL control {DLL_VtoI[1:0], DLL_cpump[2:0], DLL_EN_PFDphases, reserved[1:0]} DLL_VtoI: DLL gain control DLL_cpump: DLL charge pump current control DLL_EN_PFDphases: Enable DLL phase-sampling based lock detection
*** Note:** Common block uses 3 bits for each control function, so the 4th bit of the control doesn't have any effect on the common block.			

Reserved – RW - 32 bits - [EOR_Reg: EHCI_EOR+A8h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW - 32 bits - [EOR_Reg: EHCI_EOR+ACh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

2.2.6.3 USB2.0 Debug Port Registers

This block of registers is memory-mapped. The base offset, Dbase, is directly defined in DBUG_PRT Control register (EHCI_PCI_CFG xE4[28:16], default = 0E0h), regardless of the value in register (MEM_Reg:00h).

Registers Name	Offset Address
Control / Status	DBase + 00h
USB PIDs	DBase + 04h
Data Buffer	DBase + (08h~0Ch)
Device Address	DBase + 10h

Control / Status – RW - 32 bits - [DBUG_Reg:DBase+00h]			
Field Name	**Bits**	**Default**	**Description**
Data Length	3:0	0h	For write operations, this field is set by software to indicate to the hardware how many bytes of data in *Data Buffer* are to be transferred to the console when *Write/Read#* is set when software sets *Go*. A value of 0h indicates that a zero-length packet should be sent. A value of 1-8 indicates 1-8 bytes are to be transferred. Values 9-Fh are illegal and how hardware behaves if used is undefined. For read operations, this field is set by hardware to indicate to software how many bytes in *Data Buffer* are valid in response to software setting *Go* when *Write/Read#* is cleared. A value of 0h indicates that a zero length packet was returned. (The state of *Data Buffer* is not defined.) A value of 1-8 indicates 1-8 bytes were received. Hardware is not allowed to return values 9-Fh. The transferring of data always starts with byte 0 in the data area and moves toward byte 7 until the transfer size is reached.
Write/Read#	4	0b	Software sets this bit to indicate that the current request is a write and clears it to indicate a read.
Go	5	0b	Software sets this bit to cause the hardware to perform a request. Writing this bit to a 1 when the bit is already set may result in undefined behavior. Writing a 0 to this bit has no effect. When set, the hardware clears this bit when the hardware sets the *Done* bit. (Completion of a request is indicated by the *Done* bit.)
Error/Good#	6	0b	Read Only Updated by hardware at the same time it sets the *Done* bit. When set it indicates that an error occurred. Details of the error are provided in the *Exception* field. When cleared, it indicates that the request terminated successfully.

Control / Status – RW - 32 bits - [DBUG_Reg:DBase+00h]			
Field Name	**Bits**	**Default**	**Description**
Exception	9:7	000b	Read Only This field indicates the exception when *Error/Good#* is set. This field cannot be cleared by software. Reset default = 000b. **Value** **Meaning** 000b None 001b Transaction error: indicates the USB2 transaction had an error (CRC, bad PID, timeout, etc.) 010b HW error. Request was attempted (or in progress) when port was suspended or reset. 011b-111b Reserved
In Use	10	0	Set by software to indicate that the port is in use. Cleared by software to indicate that the port is free and may be used by other software. (This bit has no affect on hardware.)
Reserved	15:11		Reserved
Done	16	0	RWC This bit is set by HW to indicate that the request is complete. Writing a 1 to this bit will clear it. Writing a 0 to this bit has no effect.
Reserved	27:17		Reserved
Enabled	28	0	This bit is a one if the debug port is enabled for operation. Software can clear this by writing a zero to it. The controller clears the bit for the same conditions where hardware clears the Port Enable/Disable Change bit (in the PORTSC register). (Note: this bit is not cleared when System Software clears the *Port Enabled/Disabled* bit (in the PORTSC register). Software can directly set this bit, if the port is already enabled in the associated Port Status and Control register (this is HW enforced).
Reserved	29		Reserved
Owner	30	0	When debug software writes a one to this bit, the ownership of the debug port is forced to the EHCI controller (i.e. Immediately taken away from the companion controller). If the port was already owned by the EHCI controller, then setting this bit is has no effect. This bit overrides all of the ownership related bits in the standard EHCI registers. Reset default = 0. Note that the value in this bit may not affect the value reported in the *Port Owner* bit in the associated PORTSC register.
Reserved	31		Reserved

USB PIDs – RW - 32 bits - [DBUG_Reg:DBase+04h]			
Field Name	**Bits**	**Default**	**Description**
Token PID	7:0	00h	The debug port controller sends this PID as the Token PID for each USB transaction. Software will typically set this field to either IN, OUT or SETUP PID values. Reset default = undefined.

USB PIDs – RW - 32 bits - [DBUG_Reg:DBase+04h]			
Field Name	**Bits**	**Default**	**Description**
Send PID	15:8	00h	The debug port controller sends this PID to begin the data packet when sending data to USB (i.e. *Write/Read#* is asserted). Software will typically set this field to either DATA0 or DATA1 PID values. Reset default = undefined.
Received PID	23:16	00h	Read Only The debug port controller updates this field with the received PID for transactions in either direction. When the controller is sending data (*Write/Read#* is asserted), this field is updated with the handshake PID that is received from the device. When the host controller is receiving data (*Write/Read#* is not asserted), this field is updated with the data packet PID (if the device sent data), or the handshake PID (if the device NAKs the request). This field is valid when the controller sets the *Done* bit. Reset default = undefined.
Reserved	31:24		Reserved

Data Buffer – RW - 64 bits - [DBug_Reg:DBase+08h/0Ch]			
Field Name	**Bits**	**Default**	**Description**
Data Buffer	63:0	00000000_00000000h	The least significant byte is accessed at offset 08h and the most significant byte is accessed at offset 0Fh. Each byte in *Data Buffer* can be individually accessed. *Data Buffer* must be written with data before software initiates a write request. For a read request, *Data Buffer* contains valid data when *Done* is set, *Error/Good#* is cleared, and *Data Length* specifies the number of bytes that are valid. Reset default = undefined.

Device Address – RW - 32 bits - [DBUG_Reg:DBase+10h]			
Field Name	**Bits**	**Default**	**Description**
USB Endpoint	3:0	1h	4-bit field that identifies the endpoint used by the controller for all Token PID generation.
Reserved	7:4		Reserved
USB Address	14:8	7Fh	7-bit field that identifies the USB device address used by the controller for all Token PID generation.
Reserved	31:15		Reserved

2.3 SMBus Module and ACPI Block (Device 20, Function 0)

2.3.1 PCI Configuration Register Definition

Register Name	Configuration Offset
Vendor ID	00h
Device ID	02h
Command	04h
STATUS	06h
Revision ID/Class Code	08h
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
BIST	0Fh
Base Address 0	10h
Base Address 1	14h
Base Address 2	18h
Base Address 3	1Ch
Base Address 4	20h
Base Address 5	24h
Cardbus CIS Pointer	28h
Subsystem Vendor	2Ch
Subsystem ID	2Eh
Expansion ROM Base Address	30h
Capability Pointer	34h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min_Gnt	3Eh
Max_Lat	3Fh

VendorID - R - 16 bits - [PCI_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
VendorID	15:0	1002h	Vendor Identifier. The vendor ID is 0x1002. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor IDs.

DeviceID - R - 16 bits - [PCI_Reg: 02h]			
Field Name	**Bits**	**Default**	Description
DeviceID	31:16	4385h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.

Command- RW - 16 bits - [PCI_Reg: 04h]			
Field Name	**Bits**	**Default**	Description
I/O Space	0	1b	This bit controls a device's response to I/O space accesses. A value of 1 enables it and a value of 0 disables it. Since this module does claim certain legacy IO cycles, this bit's default value is 1.
Memory Space	1	1b	This bit controls a device's response to memory space accesses. A value of 1 enables it and a value of 0 disables it. Since this module does claim certain memory cycles if BIOS is strapped to the PCI bus, this bit's default value 1.
Bus Master	2	0b	A value of 0 disables the device from generating PCI accesses. A value of 1 allows it to behave as a bus master. ACPI/SMBus does not have PCI master and so the bit is always 0. [Read-only]
Special Cycle	3	0b	A value of 0 causes the devices to ignore all special cycle operations. A value of 1 allows the device to monitor Special Cycle operations. This module does not respond to special cycle and so the bit is hardcoded to 0
Memory Write & Invalidate Enable	4	0b	This bit is an enable bit for using the Memory Write and Invalidate command. This module will not generate this command and so the bit is always 0. [Read-only]
VGA Palette Snoop	5	0b	This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. This does not apply to this module and so the bit is always 0. [Read-only]
Parity Error Response	6	0b	This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device must ignore any parity errors that it detects and continue normal operation.
Wait Cycle Control	7	0b	This bit is used to control whether or not a device does address/data stepping. This module does not use address stepping and so the value is always 0. [Read-only]
SERR# Enable	8	0b	This bit is an enable bit for SERR# driver. A value of 0 disables the SERR# and a value of 1 enables it.
Fast Back-to-Back Enable	9	0b	This bit indicates whether device is fast back-to-back capable. ACPI/SMbus does not support this function and so this bit is always 0. [Read-only]
Reserved	15:10	00h	Reserved

STATUS- RW - 16 bits - [PCI_Reg: 06h]			
Field Name	**Bits**	**Default**	Description
Reserved	3:0	0000b	Reserved
MSI Mapping Capability	4	0b	[Read-only] This bit indicates whether the device can support MSI mapping.
66 MHz Capable	5	1b	This bit indicates whether the device can support 66 MHz. This device is 66 MHz capable. [Read-only]
UDF Supported	6	0b	This bit indicates whether the device supports user-definable feature. This module does not support this feature and so the bit is always 0. [Read-only]
Fast Back-to-Back Capable	7	0b	This bit indicates whether the device is capable of fast back-to-back cycles. This module does not support this feature and so the bit is always 0. [Read-only]
Data Parity Error Detected	8	0b	Set to 1 if the Parity Error Response bit is set and the module has detected PERR# asserted while acting as a PCI master (regardless of whether PERR# was driven by this module).
DEVSEL Timing	10:9	01b	These bits encode the timing of DEVSEL#. This module will always respond in medium timing and so these bits are always 11.
Signaled Target Abort	11	0b	This bit is set by a slave device whenever it terminates a cycle with a Target-Abort.
Received Target Abort	12	0b	This bit is set by a master device whenever its transaction is terminated with a Target-Abort.
Received Master Abort	13	0b	This bit is set by a slave device whenever it terminates its transaction with Master-Abort.
Signaled System Error	14	0b	This bit is set by the device whenever the device asserts SERR#.
Detected Parity Error	15	0b	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled.

Revision ID/Class Code- R - 32 bits - [PCI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
RevisionID	7:0	40h	Revision ID
Class Code	31:8	0C0500h	0C0500h denotes a SMBUS controller.

Cache Line Size- R - 8 bits - [PCI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This register specifies the system cacheline size. This module does not use Memory Write and Invalidate command and so this register is not applicable. It is hardcoded to 0.

Latency Timer- R - 8 bits - [PCI_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Latency Timer	7:0	00h	This register specifies the value of the Latency Timer. This is not used in this module and so it is always 0.

Header Type- R - 8 bits - [PCI_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	80h	This device is a multifunction device.

BIST- R - 8 bits - [PCI_Reg: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
BIST	7:0	00h	The module has no built-in self-test and so this is always 0.

Base Address 0- R - 32 bits - [PCI_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 0	31:0		Not used and is hardcoded to 0.

Base Address 1- R - 32 bits - [PCI_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 1	31:0	000h	Not used and is hardcoded to 0.

Base Address 2- R - 32 bits - [PCI_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 2	31:0	0000_0000h	Not used and is hardcoded to 0.

Base Address 3- R - 32 bits - [PCI_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
Base Address 3	31:0	0000_0000h	Not used and is hardcoded to 0.

Base Address 4- R - 32 bits - [PCI_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 4	31:0	0000_0000h	Not used and is hardcoded to 0.

Base Address 5- R - 32 bits - [PCI_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 5	31:0	0000_0000h	Not used and is hardcoded to 0.

Cardbus CIS Pointer- R - 32 bits - [PCI_Reg: 28h]			
Field Name	**Bits**	**Default**	**Description**
Cardbus CIS Pointer	31:0	0000_0000h	Not used and is hardcoded to 0.

Subsystem Vendor ID- W - 16 bits - [PCI_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	Write once.

Subsystem ID- W - 16 bits - [PCI_Reg: 2Eh]			
Field Name	**Bits**	**Default**	**Description**
Subsystem ID	15:0	0000h	Write once.

Expansion ROM Base Address - R - 8 bits - [PCI_Reg: 30h]			
Field Name	**Bits**	**Default**	**Description**
Expansion ROM Base Address	7:0	00h	Not used and is hardcoded to 0.

Capability Pointer - R - 8 bits - [PCI_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
Capability Pointer	7:0	00	Default value is 00h
Capability Pointer register			

Interrupt Line - R - 8 bits - [PCI_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	This module does not generate interrupt. This register is hardcoded to 0.

Interrupt Pin – R - 8 bits - [PCI_Reg: 3Dh]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin	7:0	00h	This register specifies which interrupt pin the device issues. This module does not generate interrupt but contains the actual interrupt controller. This register is hardcoded to 0.

Min_Gnt - R - 8 bits - [PCI_Reg: 3Eh]			
Field Name	**Bits**	**Default**	**Description**
Min_Gnt	7:0	00h	This register specifies the desired settings for Latency Timer values. Value of 0 indicates that the device has no major requirements for the setting. This register is hardcoded to 0.

Max_Lat - R - 8 bits - [PCI_Reg: 3Fh]			
Field Name	**Bits**	**Default**	**Description**
Max_Lat	7:0	00h	This register specifies the desired settings for Latency Timer values. Value of 0 indicates that the device has no major requirements for the setting. This register is hardcoded to 0.

2.3.2 ACPI Registers

Register Name	Offset Address*
Pm1Status	00h
Pm1Enable	02h
PmControl	00h
Pm2Control	00h
TmrValue/ETmrValue	00h
CLKVALUE	00h
PLvl2	04h
PLvl3	05h
PLvl4	06h
Reserved	00h

Register Name	Offset Address*
EVENT_STATUS	00h
EVENT_ENABLE	04h

*** Note**: The offset addresses listed here for the ACPI registers belong to different apertures/decodes. Check the register descriptions for details.

Pm1Status - RW - 16 bits - [AcpiPmEvtBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
TmrStatus	0	0b	Timer carry status bit. This bit gets set anytime the 31st bit of 32 bit counter changes (whenever the MSB changes from low to high or high to low. While TmrEn and TmrStatus are set, an interrupt event is raised). [Read-only]
Reserved	3:1		
BmStatus	4	0b	Bus master status bit. This bit is set any time a system bus master requests the system bus, and can only be cleared by writing an one to this bit position.
GblStatus	5	0b	This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. This is set by writing 1 to PM_Reg: 0Eh bit [1].
Reserved	7:6		
PwrBtnStatus	8	0b	Power button status bit
Reserved	9		
RtcStatus	10	0b	This bit is set when RTC generates an alarm.
Reserved	13:11		
PciExpWakeStatus	14	0b	This bit is set by hardware to indicate that the system woke due to a PCI Express® wakeup event.
WakeStatus	15	0b	This bit is set when the system is in the sleep state and a wake-up event occurs.

This register is located at the base address defined by AcpiPmEvtBlk.

Pm1Enable - RW - 16 bits - [AcpiPmEvtBlk:02h]			
Field Name	**Bits**	**Default**	**Description**
TmrEn	0	0b	This is the timer carry interrupt enable bit. When this bit is set then an SCI event is generated anytime the TmrStatus is set. When this bit is reset then no interrupt is generated when the TmrStatus bit is set.
Reserved	4:1		
GblEn	5	0b	If this bit is set, SCI is raised whenever both GblEn and GblStatus are true.
Reserved	7:6		
PwrBtnEn	8	0b	If this bit is set, SCI is generated whenever PwrBtnStatus is true.
Reserved	9		
RtcEn	10	0b	RTC enable. If this bit is set, SCI is generated whenever RtcStatus is true.
Reserved	13:11		
PciExpWakeDis	14	1b	This bit disables the inputs to the PciExpWakeStatus from waking the system.
Reserved	15		

This register is located at the base address defined by AcpiPmEvtBlk.

PmControl - RW - 16 bits - [AcpiPm1CntBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
SCI_EN	0	0b	Selects the power management event to be either an SCI or SMI# interrupt for the following events. When this bit is set, then PM events will generate an SCI interrupt; otherwise, it will be SMI#.

PmControl - RW - 16 bits - [AcpiPm1CntBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
BmRld	1	0b	If this bit is set, SCI is raised whenever there is a bus master active
GBL_RLS	2	0b	If PM IO x0E bit[0] is set; write 1 to this bit will generate SMI# and set PM IO x0F bit[0]. This bit will always return 0.
Reserved	9:3		
SLP_TYP	12:10	000b	Defines the sleep state the system enters when the SLP_TYPEn Control bit in PM_Reg: BEh (ResetControl) register and SLP_En bit are set. Five sleep states are supported: S0, S1, S3, S4, and S5. SLP_TYP / Sleep States 000 S0 001 S1 011 S3 100 S4 101 S5
SLP_En	13	0b	This is a write-only bit and reads from it always return zero. Writing 0 to this bit has no effect. Writing 1 to this bit causes the system to sequence into the sleep states as defined in the SLP_TYP field.
Reserved	15:14		

This register is located at the base address defined by AcpiPm1CntBlk.

Pm2Control - RW - 8 bits - [AcpiPm2CntBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
ARB_DIS	0	0b	System arbiter is disabled when this bit is set.
Reserved	7:1		

This register is located at the base address defined by AcpiPm2CntBlk.

TmrValue/ETmrValue – R - 32 bits - [AcpiPmTmrBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
TmrValue	31:0	-	This read-only field returns the running count of the power management timer.

This register is located at the base address defined by AcpiPmTmrBlk.

CLKVALUE - RW - 32 bits - [CpuControl:00h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0		
ClkValue	3:1	000b	These bits define throttle interval for STPCLK# de-assertion 000b: 50% 001b: 12.5% 010b: 25% 011b: 37.5% 100b: 50% 101b: 62.5% 110b: 75% 111b: 87.5%
ThtEn	4	0b	This bit enables clock throttling as set in the ClkValue.
Reserved	31:5		

This register is located at the base address defined by CpuControl.

PLvl2 - R - 8 bits - [CpuControl:04h]			
Field Name	**Bits**	**Default**	**Description**
PLvl2	7:0	00h	Reads to this register return all zeros; writes to this register have no effect. Reads to this register generates a “enter C2 power” to the clock control logic (STPCLK logic).

This register is located at the base address defined by CpuControl.

PLvl3 – R – 8 bits - [CpuControl:05h]			
Field Name	**Bits**	**Default**	**Description**
PLvl3	7:0	00h	Reads to this register return all zeros; writes to this register have no effect. Reads to this register generates a “enter C3 power” to the clock control logic (STPCLK logic).

This register is located at the base address defined by CpuControl.

PLvl4 – R - 8 bits - [CpuControl:06h]			
Field Name	**Bits**	**Default**	**Description**
PLvl4	7:0	00h	Reads to this register return all zeros; writes to this register have no effect. Reads to this register generates a “enter C4 power” to the clock control logic (STPCLK logic).

This register is located at the base address defined by CpuControl.

Reserved - RW - 8 bits - [AcpiSsCntBlk:00h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0		

EVENT_STATUS - RW - 32 bits - [AcpiGpe0Blk:00h]			
Field Name	**Bits**	**Default**	**Description**
EventStatus	31:0		Each bit represents ACPI Event status. Writing 1 to each bit clears it. Each Event status is set when the selected event input equals to the corresponding value in SciTrig.

EVENT_ENABLE - RW - 32 bits - [AcpiGpe0Blk:04h]			
Field Name	**Bits**	**Default**	Description
EventEnable	31:0	32’h0	Each bit controls whether ACP should generate wakeup and SCi interrupt.

SmiCmdPort - RW - 8 bits – [SmiCmdBlk: 00h]			
Field Name	**Bits**	**Default**	**Description**
SmiCmdPort	7:0	00h	Writing the Port can generate Smi.

This register is located at the base address defined by AcpiSmiCmd + offset 0.

SmiCmdStatus - RW - 8 bits – [SmiCmdBlk: 01h]			
Field Name	**Bits**	**Default**	**Description**
SmiCmdStatus	7:0	00h	Used by BIOS and OS

This register is located at the base address defined by AcpiSmiCmd + offset 1.

2.3.3 Power Management (PM) Registers

Hudson-1 supports two ways of accessing the PM registers: by legacy indirect IO access or by direct memory-mapped (or IO-mapped) IO access.

The indirect IO access is through CD6 (index) and CD7 (data) in the IO space. Software first programs the offset into the index register (IO space – 0xCD6) and then reads/writes to the data register (IO space – 0xCD7).

The second way of accessing the PM registers is through the new direct mapping scheme. The direct mapping is disabled at initial power up. Software needs to first program the "AcpiMmioEn" register in PM_reg offset 0x24 by using the indirect IO (CD6/CD7) programming sequence to enable the direct mapping (AcpiMMioDecodeEn) and memory-mapped (or IO-mapped) base address.

Register Name	Offset Address
IsaDecode	00h
IsaControl	04h
PciControl	08h
StpClkSMAF	0Ch
Reserved	10h
Reserved	14h
BiosRamEn	20h
AcpiMMioEn	24h
AsfEn	28h
SmBus0En	2Ch
SmBus0Sel	2Eh
SmBus0SelEn	2Fh
IoApicEn	34h
IoApicClk	38h
SmartVoltEn	3Ch
SmartVolt2En	40h
BootTimerEn	44h
WatchDogTimerEn	48h
WatchDogTimerConfig	4Ch
HPETEn	50h
SerialIrqConfig	54h
RtcControl	56h
VRT_T1	58h
VRT_T2	59h
IntruderControl	5Ah
RtcShawdow	5Bh
Reserved	5Eh
Reserved	5Fh
AcpiPm1EvtBlk	60h
AcpiPm1CntBlk	62h
AcpiPmTmrBlk	64h
P_CNTBlk	66h
AcpiGpe0Blk	68h
AcpiSmiCmdBlk	6Ah
AcpiPm2CntBlk	6Eh
AcpiConfig	74h
WakeIoAddr	78h
C1eWrPortAdr	7Ch
CStateEn	7Eh
BreakEvent	80h
AutoArbEn	84h
CStateControl	88h
StpClkHoldTime	8Ch
PopUpEndTime	8Eh
Reserved	90h
CStateTiming0	94h

Register Name	Offset Address
CStateTiming1	98h
C2Counter	9Ch
C3Counter	9Dh
Reserved	9Eh
MessageCState	A0h
TrafficMonitorEn	A4h
TrafficMonitorIdleTime	A8h
TrafficMonitorIntrTime	AAh
TrafficMonitorTrafficCount	ACh
TrafficMonitorIntrCount	AEh
TrafficMonitorTimeTick	B0h
FidVidControl	B4h
Reserved	B6h
tpreset1b	B7h
Tpreset2	B8h
Reserved	B9h
S_StateControl	BAh
ThrottlingControl	BCh
ResetControl	BEh
S5/Reset Status	C0h
ResetCommand	C4h
Cf9Shadow	C5h
HTControl	C6h
Misc0	C8h
IoDrvSth	CCh
Reserved	D0h
PmioDebug	D2h
IMCGating	D6h
Eprom/EfuseIndex	D8h
Eprom/EfuseData	D9h
SataConfig	DAh
Reserved	DCh
Reserved	DEh
BlinkControl	DFh
ABRegBAR	E0h
Reserved	E6h
PcibConfig	EAh
AzEn	EBh
LpcGating	ECh
UsbGating	EDh
UsbEn	EFh
UsbControl	F0h
UsbDebug	F3h
GecEn	F6h
GecConfig	F8h
TraceMemoryEn	FCh

IsaDecode - RW – 8/16/32 bits - [PM_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Obsolete	0	0b	This is an obsolete function; BIOS should leave it as 0.
Intr_enable	1	1b	Set to 1 to enable PIC interrupt function
tmr_enable	2	1b	Set to 1 to enable 8254 timer function.
pm_enable	3	1b	Set to 1 enable Io CD6/CD7 decoding in internal Isa bus. The bit has to be set all the time
Reserved	5:4	-	
IndexPortEn	6	0b	If set, FCH will decode IO CE0:CE4. These two ports are for debugging purpose only
IsaPmDebugEn	7	0b	Debug function only.

IsaDecode - RW – 8/16/32 bits - [PM_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:8	-	
DmaAddr_En	16	1b	Enable the decoding of I/O Port 0x000:0x01F, 0x080:0x08F, 0x0C0:0xCF, 0x0D0:0x0DF, 0x40B, 0x4D6.
PitAddr_En	17	1b	Enable the decoding of I/O Port 0x40, 0x41, 0x42, 0x43.
NmiAddr_En	18	1b	Enable the decoding of I/O Port 0x61.
RtcAddr_En	19	1b	Enable the decoding of I/O Port 0x70 and 0x71.
Reserved	24:20	-	
PM_Addr_Enable	25	1b	Enable the decoding of I/O Port 0xCD6, xCD7.
Reserved	27:26	0b	Reserved
Reserved	29:28	00b	Spare bits.
Port92Enable	30	1b	Enable the decoding of I/O Port 92.

IsaControl - RW – 8/16/32 bits - [PM_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Dma_limit	6:0	00h	Specify the legacy DMA transfer size.
Dma_limit_en	7	0b	Set to 1 to enable the Dma_limit on the legacy DMA transfer on the LPC bus.
Reserved	9:8	-	.
Debug	10	1b	Debug purpose, always leave it as 1
Bm_req_en	11	0b	Legacy BM_REQ# function enable bit; it is now for debug purpose only.
Reserved	13:12	-	
Reserved	24	-	
PCIB_SReset_En Mask	25	0b	When set, PCIBridge reset control bit PCIB_SReset_En (x3e bit 22 of PCI Bridge) will be writable
Reserved	27:26	-	

PciControl - RW – 8/16/32 bits - [PM_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	-	
DmaVerifyEn	2	0b	Set to1 to enable mimicking of legacy DMA VERIFY function. This is only needed for old LPC driver (such as floppy) that requires VERIFY function
Mask_k8_msg_bmsts_en	3	0b	Set to 1 to enable A20#, IGNNE#, INIT#, NMI, SMI# message delivery.
K8_intr_enable	4	0b	Set to 1 to deliver legacy PIC interrupt as message type.
Mts_set	5	1b	1: Encode PIC interrupt request as Legacy PIC ExtInt message type and NMI request as legacy NMI message type. 0: encode PIC interrupt request as ExtInt message type and NMI request as NMI message type.
Mts_auto	6	0b	Set to 1 to encode PIC Intr request as Legacy PIC ExtInt message type and PIC Nmi request as legacy PIC NMI message type if IOAPIC is enabled and Mts_set is zero.
Force_smaf_match	7	0b	0: Enable comparison with SMAF The SMAF code in the received STPGNT message has to match with the SMAF code in the current StpClk assertion message. (Hardware power up default) 1: Disable comparison with SMAF The SMAF code in the received STPGNT message is not required to match with the SMAF code of the current StpClk assertion message.
Pic_apic_arbiter	8	1b	Set to 1 to arbitrate between PIC request and IOAPIC request
Debug	10	1b	Debug use only, SW should leave this bit as 1
Reserved	11	-	

PciControl - RW – 8/16/32 bits - [PM_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Ext_intr_time	14:12	000b	Specify the extended interrupt time in 2 microsecond intervals. This is used for preventing CPU from re-entering C state right away when it just breaks out from a C state
Reserved	18:15	-	
Ab_stall_en	23	0b	Set to 1 to make ACPI hold bus before completing legacy DMA on the LPC bus. This is only needed for certain old LPC devices.
Force_stpclk_retry	24	1b	Set to 1 to send out STPCLK message before the completion response of the following 3 types of request: 1. I/O write to Slp_typ register 2. I/O write Ldt_stp command 3. C1e cycle Normally it is required to send out STPCLK before completion of the cycles listed above, except for the case of SMI trapping. In that case, this bit should be left as 0
Force_slpstate_retry	25	0b	Set to 1 to send out SMI message before the completion response of IO write to SLP_TYP register. This is to be used conjunction with SMI trapping on write to SLP_TYP register

Note: SLP_TYP is located in AcpiPm1CntBlk offset 00h, bits 10~12.

StpClkSmaf - RW – 8/16/32 bits - [PM_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
S4S5SMAF	2:0	110b	System management action field for S4/5 STPCLK message
C2SMAF	6:4	0h	System management action field for C2 STPCLK message
C3SMAF	10:8	001b	System management action field for C3 STPCLK message
VFSMAF	14:12	010b	System management action field for VFID STPCLK message
S1SMAF	18:16	011b	System management action field for S1 STPCLK message
S3SMAF	22:20	100b	System management action field for S3 STPCLK message
NSSMAF	26:24	101b	System management action field for Normal Throttling STPCLK message
TTSMAF	30:28	101b	System management action field for Thermal Throttling STPCLK message

Reserved - RW – 8/16/32 bits - [PM_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved - RW – 8/16/32 bits - [PM_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

BiosRamEn - RW – 8/16/32 bits - [PM_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
Bios_ram_mem_enable	0	0b	Set to 1 to enable BIOS RAM access.
Bios_ram_mem_Addr	31:8	FED1_00h	Specify the BIOS RAM base address[31:8].

AcpiMmioEn - RW – 8/16/32 bits - [PM_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
AcpiMMioDecodeEn	0	0b	Set to1 to enable AcpiMMio space.
AcpiMMIoSel	1	0b	Set AcpiMMio registers to be memory-mapped or IO-mapped space. 0: Memory-mapped space 1: I/O-mapped space

AcpiMmioEn - RW – 8/16/32 bits - [PM_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
AcpiMMioAddr	31:12	FED8_00h	SBResourceMMIO_Base register Offset 000:0FF SM PCI configuration registers 100:1FF GPIO 200: 2FF SMI 300: 3FF PMIO 400: 4FF PMIO2 500: 5FF BIOS_RAM 600: 6FF CMOS_RAM 700: 7FF CMOS 800: 8FF ACPI 900: 9FF ASF registers A00: AFF Smbus registers B00: BFF WatchDog registers C00: CFF HPET (new) D00: DFF IoMux (new) E00: EFF Misc (new)

AsfEn - RW – 8/16/32 bits - [PM_Reg: 28h]			
Field Name	**Bits**	**Default**	**Description**
AsfEn	0	0b	Set to 1 to enable ASF function and I/O decoding.
AsfClkStretchEn	1	0b	Set to 1 to enable clock stretching support.
AsfSmMasterEn	2	0b	Set to 1 to enable ASF SMBUS master function.
AsfIoBase	15:5	059h	Specify the AsfIoBase[15:5]. By default AsfIoBase is B20h.
AsfClkSel	22:16	00000h	The value controls the frequency of ASF master clock; its definition is: 0: ~100KHz 1: ~200KHz 2: ~300kHz 3:~ 400kHz 4:~ 600kHz 5:~ 800kHz 6:~ 900kHz 7:~1MHz Others: 66.67M/((AsfClkSel + 1) * 2)
AsfClkSwitchEn	23	0b	Set to 1 to change ASF master clock from RTC(32k) to the clock defined in AsfClkSel of the same register.

Smbus0En - RW – 16 bits - [PM_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
SmBus0En	0	0b	Set to 1 to enable SMBUS0 function and decoding.
SmBus0Sel	2:1	00b	SmBus port selection when PM_Reg 2Fh bit 0 is set to 0 00: Port 0 01: Port 2 10: Port 3 11: Port 4
SmBus0_baddr	15:5	058h	Specify the Smbus0IoBase[15:5]. By default Smbus0IoBase is B00h.

Smbus0Sel - RW – 8 bits - [PM_Reg: 2Eh]			
Field Name	**Bits**	**Default**	**Description**
SmBus0Sel	2:1	0b	SmBus port selection when PM_Reg 2Fh bit 0 is set to 1 00: Port 0 01: Port 2 10: Port 3 11: Port 4

Smbus0SelEn - RW – 8 bits - [PM_Reg: 2Fh]			
Field Name	**Bits**	**Default**	**Description**
SmBus0SelEn	0	0b	0: SmBus Port selection is visible in PMIO2C[2:1] 1: SmBus Port selection is visible in PMIO2E[2:1]

IoApicEn - RW – 8/16/32 bits - [PM_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
Ioapic_enable	0	0b	Set to 1 to enable IoApic decoding.
Ioapic_mode	1	1b	XIOAPIC enable; this bit is only valid if bit 0 is set.
Ioapic_m_io_	2	1b	0: I/O space 1: Memory space
Ioapic_id_ext_en	4	1b	Set to1 to extend APIC ID from 4 bits to 8 bits.
IoapicBaseAddr	31:5	07F6000h	Specify the IoApic base address[31:5]. By default it is FEC0_0000h.

SmartVoltEn - RW – 8/16/32 bits - [PM_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
SmartVoltIdleTime	6:0	0h	Amount of “idle” time (in 2us increment) the SmartPower function should wait before it assert SmartVolt.
SmartVoltEnable	7	0b	Enable bit for the SmartPower function. When set, the logic will monitor the logic defined by the “Check*” bits (bit8 ~ bit23). If all of the corresponding modules are idle, an internal SmartVoltEvent will be generated and the corresponding modules can use the SmartVoltEvent to do board level voltage control.
CheckVIN0	8	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN0 has reached or passed the threshold.
CheckVIN1	9	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN1 has reached or passed the threshold.
CheckVIN2	10	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN2 has reached or passed the threshold.
CheckVIN3	11	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN3 has reached or passed the threshold.
CheckVIN4	12	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN4 has reached or passed the threshold.
CheckVIN5	13	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN5 has reached or passed the threshold.
CheckVIN6	14	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN6 has reached or passed the threshold.
CheckVIN7	15	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN7 has reached or passed the threshold.

SmartVoltEn - RW – 8/16/32 bits - [PM_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
CheckC3	16	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if CPU is in C3 state.
Reserved	17	0b	Reserved
CheckSata	18	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if SATA is idle
CheckUsb	19	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if USB is idle.
CheckPciBridge	20	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if HD audio PCIBridge is idle.
Reserved	21	0b	Reserved
CheckAz	22	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if HD audio is idle.
CheckLpc	23	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if LPC is idle.

SmartVolt function is meant to provide a mechanism to control the external power supply in order to reduce additional system power consumption. For example, software can set Smart Power Control1 bit [6] and [7]. Whenever CPU enters C3 state and SATA controller is not active, this function will assert SMARTVOLT/GPIO4. System design can use this signal to control the power supply to reduce the ATA power by 5~10%. Another example is to connect an ambient light sensor to one of the VIN inputs. When the circuit has detected the ambient light is below certain threshold, this function can automatically dim the LCD back light. Note this is an aggressive power management function outside of OS control and it is platform specific.

SmartVolt2En - RW – 8/16/32 bits - [PM_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
SmartVoltIdleTime	6:0	0h	Amount of “idle” time (in 2us increment) the SmartPower function should wait before it assert SmartVolt
SmartVoltEnable	7	0b	Enable bit for the SmartPower function. When set, the logic will monitor the logic defined by the “Check*” bits (bit8 ~ bit23). If all of the corresponding modules are idle, an internal SmartVoltEvent will be generated and the corresponding modules can use the SmartVoltEvent to do board level voltage control.
CheckVIN0	8	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN0 has reached or passed the threshold.
CheckVIN1	9	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN1 has reached or passed the threshold.
CheckVIN2	10	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN2 has reached or passed the threshold.
CheckVIN3	11	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN3 has reached or passed the threshold.
CheckVIN4	12	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN4 has reached or passed the threshold.
CheckVIN5	13	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN5 has reached or passed the threshold.
CheckVIN6	14	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN6 has reached or passed the threshold.

SmartVolt2En - RW – 8/16/32 bits - [PM_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
CheckVIN7	15	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if VIN7 has reached or passed the threshold.
CheckC3	16	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if CPU is in C3 state.
Reserved	17	0b	Reserved
CheckSata	18	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if SATA is idle.
CheckUsb	19	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if USB is idle.
CheckPciBridge	20	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if HD audio PCIBridge is idle.
Reserved	21	0b	Reserved
CheckAz	22	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if HD audio is idle.
CheckLpc	23	0b	If SmartVoltEnable is set and this bit is also set, the SmartPower function will only assert SmartVolt if LPC is idle.

SmartVolt function is meant to provide a mechanism to control the external power supply in order to reduce additional system power consumption. For example, software can set Smart Power Control1 bit [6] and [7]. Whenever CPU enters C3 state and SATA controller is not active, this function will assert SMARTVOLT/GPIO4. System design can use this signal to control the power supply to reduce the ATA power by 5~10%. Another example is to connect an ambient light sensor to one of the VIN inputs. When the circuit has detected the ambient light is below certain threshold, this function can automatically dim the LCD back light. Note this is an aggressive power management function outside of OS control and it is platform specific

BootTimerEn - RW – 32 bits - [PM_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
FailBootTimer	24:0	0000000h	The counter of NB boot timer(14.318MHz), which starts counting when all of the the following conditions are met: 1. Bit[31] of this register is set. 2. PCI reset is not asserted. 3. NBBootTmr Strap is on.
ExpireBootTmr	29	0b	Set to 1 to force boot timer to expire; then, NB PwrGood can be asserted.
FailBootRstSts	30	0b	0: Boot timer has not been fired. 1: Boot timer has been fired. Read only.
BootTmrDisable	31	0b	Set to 1 to disable NB boot timer function.

WatchDogTimerEn - RW – 32 bits - [PM_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
WatchDogDecodeEn	0	0b	Set 1 to enable decoding of WatchDogTimer address. This WatchDogTimer is a standard defined by Microsoft®
WatchDogFuncDisable	1	0b	1: Disable WatchDog function 0. Enable WatchDog function
Reserved	2	-	
WatchDogBase	31:3	0000000h	WatchDogTimer base address

WatchDogTimerConfig - RW – 8 bits - [PM_Reg: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
WatchDogFreq	1:0	11b	This field defines the clock frequency used by the WatchDogTimer. 00: 32KHz 11: 1Hz
Reserved	7:2	000000b	

HPETEn - RW – 8 bits - [PM_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
HPETDecodeEn	0	0b	Set to1 to enable HPET MMIO space decoding.
HPETIRQEn	1	0b	Set to1 to enable HPET IRQ output.
HPET_Timer0_MSI_en	2	0b	Set to1 enable HPET timer0 MSI capability.
HPET_Timer1_MSI_en	3	0b	Set to1 enable HPET timer1 MSI capability.
HPET_Timer2_MSI_en	4	0b	Set to1 enable HPET timer2 MSI capability.
Reserved	7:5	-	
HPETBaseAddress	31:10	3FB400h	HPET MMIO base is FED0_0000h by default.

SerialIrqConfig - RW – 8/16 bits - [PM_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
NumStartBits	1:0	00b	This field defines the number of clocks in the start frame. Start Frame Width = 4 + 2 * NumStartBits
NumSerIrqBits	5:2	0h	Total number of serial IRQ's = 17 + NumSerIrqbits 0: 17 serial IRQ's (15 IRQ, SMI#, + IOCHK#) 1: 18 serial IRQ's (15 IRQ, SMI#, IOCHK#, INTA#) ... 15: 32 serial IRQ's The serial IRQ can support 15 IRQ#, SMI#, IOCHK#, INTA#, INTB#, INTC#, and INTD#. When serial SMI# is used, BIOS will need to check SIO (or device that generates serial SMI#) for status.
SerIrqMode	6	0b	0: Continuous mode 1: Active (quiet) mode
SerialIrqEnable	7	0b	Setting this bit to 1 enable the serial IRQ function.
Reserved	9	0b	
Reserved	10	0b	

RtcControl - RW – 8 bits - [PM_Reg: 56h]			
Field Name	**Bits**	**Default**	**Description**
Rt cProtect38_3F	0	0b	When set, RTC RAM index 38:3Fh will be locked from read/write. This bit can only be written once.
RtcProtectF0_FF	1	0b	When set, RTC RAM index F0:FFh will be locked from read/write. This bit can only be written once.
RtcProtectE0_EF	2	0b	When set, RTC RAM index E0:EFh will be locked from read/write. This bit can only be written once.
RtcProtectD0_DF	3	0b	When set, RTC RAM index D0:DFh will be locked from read/write. This bit can only be written once.
RTCProtectC0_CF	4	0b	When set, RTC RAM index C0:CFh will be locked from read/write. This bit can only be written once.
Rtc_test_en	6	0b	This is the test enable for the RTC 32KHz oscillator control bits (rtc_osc_set0, rtc_osc_set1).
Rtc_osc_set_en	7	0b	This is the latch enable for the RTC 32KHz oscillator control bits (rtc_osc_set0, rtc_osc_set1).
Rtc_osc_set0	8	0b	RTC oscillator control bit
Rtc_osc_set1	9	0b	RTC oscillator control bit
RtcClkDrive	10	1b	0: HIGHDRIVE tied low for RtcClkOut pad 1: HIGHDRIVE tied high for RtcClkOut pad
Mask_rtc_clk_out	11	0b	Set to1 to disable RtcClk output.

RtcControl - RW – 8 bits - [PM_Reg: 56h]			
Field Name	**Bits**	**Default**	**Description**
CenturyEn	12	1b	Enable RTC Century support.
AltCmosMapEn	13	0b	When enabled, bank 1 of CMOS RAM is changed. Index 00:0D will still return the time and alarm settings. Index 0E:7F will return the absolute offset 8E:FF.

VRT_T1 - RW – 8 bits - [PM_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
VRT_T1	7:0	01h	To conserve power, the RTC battery is sampled periodically for checking its state of health. VRT_T1 and VRT_T2 make up the interval of the checking. When VRT_Enable is high, the battery is being sampled. When VRT_enable is low, the battery is not being sampled. This register defines the time of VRT enable being high for RTC battery monitor circuit, in milliseconds.

VRT_T2 - RW – 8 bits - [PM_Reg: 59h]			
Field Name	**Bits**	**Default**	**Description**
VRT_T2	7:0	FFh	This register defines the time of VRT enable being low for the RTC battery monitor circuit, in 4 ms increments.

IntruderControl - RW – 8 bits - [PM_Reg: 5Ah]			
Field Name	**Bits**	**Default**	**Description**
IntruderAlertDis	0	1b	Set to 0 to enable IntruderAlert.
IntruderAlertClr	1	0b	Write 1 to clear the IntruderAlert status bit.
IntruderAlertSts	2	0b	The status bit will be set to 1 if an Intruder alter has been occurred Software need to set bit1 to clear the status bit.
CmosEraseDis	4	1b	Set to1 to disable CMOS Erase.
CmosEraseClr	5	0b	Write to 1 to clear CMOS Erase status.
CmosEraseSts	6	0b	Indicate that a CMOS Erase has been occurred.

RtcShadow - RW – 8 bits - [PM_Reg: 5Bh]			
Field Name	**Bits**	**Default**	Description
Writing to bits[3:0] will set the value onto bits[7:4]. Software should always set bit 2 = 1 for this operation.			
PwrFailShadow (Write only)	1:0	00b	These two bits will determine how system should resume after a power failure. 00: Always off—always power off after power resumes 01: Always on—always power on after power resumes 10: Always off—always power off after power resumes 11: Use previous—resume to same setting when power fails
PowerState (Write only)	2	0b	This bit should be set to 1 by software. If this bit is '0' the Power fail function may not function correctly. Power state indicator. 0: Off 1: On
ForcePwrOn (Write only)	3	0b	0: If RTC AIE = 1, will wakeup when RTC alarm fires after a power failure/resume. (See Note) 1: If RTC AIE =1, will force power on after power resumes regardless of Bit[5:4] setting. (See Note)
The following bits can be written to only by setting the corresponding 3:0 bits. Values written in bits[3:0] will be reflected and be read only in bits[7:4].			

RtcShadow - RW – 8 bits - [PM_Reg: 5Bh]			
Field Name	**Bits**	**Default**	Description
PwrFailShadow (Read only)	5:4	00b	These two bits will determine how the system should resume after a power failure. 00: Always off—always power off after power resumes 01: Always on—always power on after power resumes 10: Always off—always power off after power resumes 11: Use previous—resume to same setting when power fails
PowerState (Read only)	6	0b	This bit should be set to 1 by software. If this bit is '0' the Power fail function may not function correctly. Power state indicator. 0: Off 1: On
Note: Programming of bit 7 will influence the system power-on state only when the Wake source is RTC interrupt. RTC needs to be programmed for a wake event to be triggered with RTC AIE set to 1. RTC AIE is defined in RTC_REG 0Bh bit 5.			
ForcePwrOn (Read only)	7	0b	0: If RTC AIE = 1, will wake up when RTC alarm fires after a power failure/resume. 1: If RTC AIE =1, will force power-on after power resumes regardless of Bit[5:4] setting.

Reserved - RW – 8 bits - [PM_Reg: 5Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

Reserved - RW – 8 bits - [PM_Reg: 5Fh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

AcpiPm1EvtBlk - RW – 8/16 bits - [PM_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
AcpiPm1EvtBlk	15:2	0000h	These bits define the least significant byte of the 16 bit I/O range base address of the ACPI power management Event Block. Bit 2 corresponds to Addr[2] and bit 7 corresponds to Addr[7].

AcpiPm1CntBlk - RW – 8/16 bits - [PM_Reg: 62h]			
Field Name	**Bits**	**Default**	**Description**
AcpiPm1CntBlk	15:1	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management Control block. Bit 1 corresponds to Addr[1] and bit 7 corresponds to Addr[7].

AcpiPmTmrBlk - RW – 8/16 bits - [PM_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
AcpiPmTmrBlk	15:1	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management Timer block. Bit 1 corresponds to Addr[1] and bit 7 corresponds to Addr[7].

P_CNTBlk - RW – 8/16 bits - [PM_Reg: 66h]			
Field Name	**Bits**	**Default**	**Description**
CpuControlLo	15:3	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management CPU Control block. Bit 3 corresponds to Addr[3] and bit 7 corresponds to Addr[7]. Addr[2:0] are ignored because this register block is 6 byte long.

AcpiGpe0Blk - RW – 8/16 bits - [PM_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
AcpiGpe0BlkLo	15:2	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI power management General Purpose Event block. Bit 2 corresponds to Addr[2] and bit 7 corresponds to Addr[7]. Addr[1:0] are ignored because this register block is 4 byte long.

AcpiSmiCmd - RW – 8/16 bits - [PM_Reg: 6Ah]			
Field Name	**Bits**	**Default**	**Description**
AcpiSmiCmd	15:0	0000h	These bits define the least significant byte of the 16 bit I/O base address of the ACPI SMI Command block. Bit 0 corresponds to Addr[0] and bit 7 corresponds to Addr[7]. The address is required to be WORD-aligned (Addr[0]=0)

AcpiPm2CntBlk - RW – 16 bits - [PM_Reg: 6Eh]			
Field Name	**Bits**	**Default**	**Description**
AcpiPm2CntBlk	15:0	0000h	These bits define the most significant byte of the 16 bit I/O base address. Bit 0 corresponds to Addr[8] and bit 7 corresponds to Addr[15].

AcpiConfig - RW – 8/16/32 bits - [PM_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
Decen_acpi	0	0b	Set to 1 to enable decoding of the standard ACPI registers
Gbl_en_en	1	0b	Set to 1 to enable GBL function in the standard ACPI - PmControl register.
Rtc_en_en	2	0b	Set to1 to enable RTC_EN function in the standard ACPI register. This is designed as a backdoor for BIOS to control it.
Slpbtn_en_en	3	0b	Set to1 to enable SLPBTN_EN function in the standard ACPI register. This is designed as a backdoor for BIOS to control it
Tmr_en_en	4	0b	Set to 1 enable TMR_EN function in the standard ACPI register. This is designed as a backdoor for BIOS to control it.
Reserved	5	-	
MaskArbDis	6	0b	Set to1 to disable ArbDis function in the ACPI register. ArbDis is not really used, but it still needs to be accessible by OS.
BIOS_RLS	7	0b	Set to1 to generate SCI. Read always return 0
PCIeNative	24	0b	Setting to 1 will block PCIe GPP PME message and HotPlug message from generating SCI. This is used for supporting ACPI 3.0 specification. If ACPI 3.0 is not supported, this bit should be left as 0
PCIE_WAK_Mask	25	0b	Set to1 to disable PCIE_WAK_STS and PCIE_WAK_DIS function. This is used for supporting ACPI 3.0 specification. If ACPI 3.0 is not supported, this bit should be left as 1
Reserved	26	-	

AcpiConfig - RW – 8/16/32 bits - [PM_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
WakePinAsGevent	27	0b	Set to 1 to treat Wake# pin as Gevent input.

WakeIoAddr - RW – 16 bits - PM_Reg: 78h]			
Field Name	**Bits**	**Default**	**Description**
WakeIoBaseAddress	15:0	FFFFh	The register specifies the wake I/O address. Any I/O write to the I/O address can cause CPU to wake from C state. This is an obsolete function that is not used anymore

HaltCountEn - RW – 16 bits - PM_Reg: 7Ah]			
Field Name	**Bits**	**Default**	**Description**
NumOfCpu	3:0	0000b	Defines the number of CPUs or CPU core pairs in the system. This parameter is used for C state logic.
CountHaltMsgEn	15	0b	When set, FCH will keep track of CPU state by counting HALT entering and exit messages. When all CPUs are in HALT state, FCH will assume the system is in C state.

C1eWrPortAdr - RW – 16 bits - PM_Reg: 7Ch]			
Field Name	**Bits**	**Default**	**Description**
C1eWrPortAdr	15:0	FFFFh	I/O write decoding Base address. This is an obsolete function that is not used anymore

CStateEn - RW – 16 bits - [PM_Reg: 7Eh]			
Field Name	**Bits**	**Default**	**Description**
K8C1eWrSel	1:0	00b	00: C1e write data bit[7:0] is selected 01: C1e write data bit[15:8] is selected 10: C1e write data bit[23:16] is selected 11: C1e write data bit[31:24] is selected
C2ToC3Enable	2	0b	Set to 1 to put CPU into C3 even it is P_LVL2 Io read.
C2EnhanceEn	3	0b	Set to 1 to enable C2 enhancement.
C1eToC2En	4	0b	Set to 1 to put CPU into C2 state in C1e state.
C1eToC3En	5	1b	Set to 1 to put CPU into C3 state in C1e state.
CPopUpEn	6	1b	Set to1 to enable pop up capability, which means going to C2 if there is a traffic and back to C3 after idle for a while. The bit should be set to 0 when AltVid is not enabled.
Reserved	7	-	
oAllowLdtStpAsOut	8	0b	Control the input/output direction of pin AllowLdtStp. 0: (default) AllowLdtStp is input to Hudson-1 driven by NB. 1: AllowLdtStp as output pin to NB to indicate FCH traffic activities.
AllowLdtStpOutputEn	9	0b	Set to 1 to treat AllowLdtStp as output to notify NB that there is potential traffic from FCH
Reserved	14	-	
Mask_intr_en	15	1b	If set, the APIC interrupt will be deferred until the first ACPI access after the system resumes from S state. In additionally, A20M#, IGNNE#, INTR, NMI, INIT# messages will be deferred the same way, but SMI# will not be deferred.

BreakEvent - RW – 32 bits - [PM_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Bm_sts_rd_mask	0	0b	0: BM_STS bit in Pm1a_STS is set to1 if there is any DMA traffic in FCH. 1: Make BM_STS bit in Pm1a_STS always return 0 except for USB 1.1 traffic.

BreakEvent - RW – 32 bits - [PM_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Auto_bm_rld	1	0b	It is used for PopUp and C1e function. Set to 1 to make a break event as long as BM_STS is set.
Auto_clr_bm_sts	2	0b	It is used for PopUp and C1e function. Set to1 to automatically clear BM_STS before entering C state.
Reserved	3	-	
EnableBreak	4	0b	Set to 1 to skip the C state transition if there is break event when entering C state.
Reserved	6:5	-	Reserved.
BmReqEn	7	0b	Set to1 to treat BMREQ# as one source of Break Event
BmReqPopUpEn	8	0b	Set to 1 to allow PopUp if BMREQ# is toggled when PopUp function is enabled.
BusReqHoldEn	9	0b	Set to1 to extend BMREQ# until LDTSTP# is asserted.
MergeBMReqEn	10	0b	When set, the logic merges BMREQ# and AllowLdtStop together internally.
AutoStutterTimerEn	11	0b	This feature is specifically designed for multi-CPUs (as in server applications). Set to 1 to enable a AutoStutterTimer that will automatically count whenever LDTSTOP# is asserted during C3/C1e state. When the timer reaches the threshold (defined by AutoStutterLimit), it will stutter the C state machine. This feature is designed to periodically reconnect the HT link in the case of a long idle time.
AutoStutterTimeSel	12	0b	This bit selects the time increment used by the AutoStutterTimer 0: 2μs increment 1: 1ms increment
ServerCEn	13	0b	When set, FCH will monitor HALT messages coming from CPU(s). When all CPUs are in HALT state, FCH will automatically transition to C3/C1e state. If any CPU exits from HALT state, FCH will exit out from C3/C1e state as well.
Usb11_BmStsEn	16	0b	Set to1 to merge USB 1.1 traffic status into BM_STS.
Usb11_SetBmStsDis	17	0b	Set to1 to not merge Usb 1.1 traffic as source of DMA traffic.
Usb20_SetBmStsDis	18	0b	Set to1 to not merge Usb 2.0 traffic as source of DMA traffic.
Reserved	21:19	-	
AutoStutterLimit	30:24	00h	This defines the limit for the AutoStutterTimer. Time unit is defined by bit 12

AutoArbEn - RW – 8/16/32 bits - [PM_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
AutoArbWaitTime	3:0	0000b	This defines the amount of time (in 2μs increment) that FCH will hold ARB_DIS set after breaking from C3. This is to allow sometime for CPU to resume from C3 before allowing any bus mastering to the memory. This timer has an uncertainty of 2μs. This applies to K8 C1e if AutoArbDisEn is set.
Reserved	7	-	

CStateControl - RW – 32 bits - [PM_Reg: 88h]			
Field Name	**Bits**	**Default**	**Description**
WaitStpGntEnB	0	0b	Set to1 to wait for STPGNT# in ACPI S state.
Reserved	1	0b	
DlySlpEn	2	0b	Set to 1 to delay recognition of STPGNT# until there is no pending read in AB
Reserved	3	0b	
Cc_en	4	0b	C State enable; must be set in order to exercise C state
Slp_en	5	0b	Enable LDTSTOP# as an output
Reserved	11:6	-	.

CStateControl - RW – 32 bits - [PM_Reg: 88h]			
Field Name	**Bits**	**Default**	**Description**
StutterMode	12	0b	Set to 1 to enable stutter mode.
Reserved	31:13	-	Reserved

StpClkHoldTime - RW – 8 bits - [PM_Reg: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
StpClkHoldTime	7:0	9Eh	STPCLK# hold time with respect to LDTSTOP# in number of A-Link clocks.

PopUpEndTime - RW – 8 bits - [PM_Reg: 8Eh]			
Field Name	**Bits**	**Default**	**Description**
PopUpEndTime	7:0	10h	During C1e pop-up, FCH monitors internal DMA traffic. If there has been no traffic for PopUpEndTime, FCH will bring system back to C1e. The time is counted by 14.318MHz clock. This can considered as a minimum LDTSTOP deassertion time; however, this has been combined into LdtStartTime (PMIO_94[23:16]), and is not really required.

Reserved - RW – 8/16/32 bits - [PM_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

CStateTiming0 - RW – 8/16/32 bits - [PM_Reg: 94h]			
Field Name	**Bits**	**Default**	**Description**
StutterTime	7:0	01h	LDTSTP# duration in 1µs increments. This is basically the minimum LDTSTOP assertion time
S_LdtStartTime	15:8	00h	This register defines the delay between SUS_STAT# assertion and LDTSTP# assertion when the system enters ACPI S states, in 1µs increments, with 1µs uncertainty.
LdtStartTime	23:16	10h	LDTSTP# deassertion time (in 1µs increments) in C state
LdtEndTime	25:24	00b	LDTSTP# de-assertion delay select. 00: 0µs 01: 1µs 10: 32µs 11: 64µs This is the delay from deassertion of LDTSTOP# till the deassertion of STPCLK

CStateTiming1 - RW – 8/16/32 bits - [PM_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
StpClkDlyTime	7:0	00h	Additional STPCLK# deassertion delay in number of OSC clocks for S1 resume.
FirstLdtStartTime	15:8	10h	Very first LDTSTOP# assertion delay (in 1µs increments) from reception of STPGNT.
Reserved	25:24	-	

CStateTiming1 - RW – 8/16/32 bits - [PM_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
VidFidTime	30:28	01b	VID/FID LDTSTP# duration select. 000: 1μs 001: 2μs 010: 4μs 011: 8μs 100: 16μs 101: 32μs 110: 64μs 111: 128μs

C2Count - R – 8 bits - [PM_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
C2Count	7:0	00h	The value shows the amount of time the CPU spends in C2. Each increment represents approximately 0.39% (1/256). This register is updated by HW automatically every second.

C3Count - R – 8 bits - [PM_Reg: 9Dh]			
Field Name	**Bits**	**Default**	**Description**
C3Count	7:0	00h	The value shows the amount of time the CPU spends in C3. Each increment represents approximately 0.39% (1/256). This register is updated by HW automatically every second.

Reserved- R – 8 bits - [PM_Reg: 9Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

MessageCState - RW – 8/16/32 bits - [PM_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
oBattModeChgMsgEn	0	0b	When enabled, FCH will automatically send a message to CPU indicating the power mode (AC vs battery). In addition, every time it is changed, FCH will generate a message to indicate the update.
TimerTickChgMsgEn	1	0b	When enabled, FCH will send a message to CPU indicating the latest periodic timer interval. FCH will automatically determine which timer (PIT, RTC, or HPET) is being used.
FusionCEnable	2	0b	Set to1 to enable the FCH Fusion C state coordination logic. Fusion CPU contains the actual C state logic and FCH contains the coordination logic which sends handshake message to CPU to help CPU to decide which C state to go into. This bit should be set only when the ***Cx*** states are enabed.
FusionPerr_en	3	0b	When enabled, FCH C state coordination logic will cause CPU to exit from C state when there is a parity error within the FCH. This bit should be set only when the ***Cx*** states are enabed.
FusionSerr_en	4	0b	When enabled, FCH C state coordination logic will cause CPU to exit from C state when there is a system error within the FCH. This bit should be set only when the ***Cx*** states are enabed.
Reserved	5	0b	Reserved.

MessageCState - RW – 8/16/32 bits - [PM_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
BatteryModeEn	6	0b	When set, a change in power mode (battery vs AC) will cause FCH to tell CPU to exit from C state.
SelfExitEnable	7	0b	When set, FCH will exit to C0 state from non-C0 state when there is a break event and exit to C1 state from non-C0 state when there is traffic.
WakeByImc	8	0b	A static bit that can be written by IMC to cause FCH to generate C state exit message to CPU.
PopUpByImc	9	0b	A static bit that can be written by IMC to cause FCH to pop up C state message to CPU.
ClkIntrTagEn	10	0b	When enabled, FCH will mark the periodic timer interrupt.
ExtendEnable	11	0b	When enabled, FCH will start a timer whenever the C state is exited. The purpose is to prevent CPU from going back to C state before the timer expires.
UsbOhciModeFusion[1:0]	13:12	00b	These bits are to be used with Fusion CPU C state. If bit 0 is set, FCH will stutter the CPU C state whenever USB OHCI has pending traffic. If bit 1 is set, FCH will cause CPU to break out from C state when USB OHCI has pending traffic. These bits affect AltVid entry and should be set to 01 only when AltVid is enabled; otherwise leave at 00.
UsbEhciModeFusion[1:0]	15:14	00b	These bits are to be used with Fusion CPU C state. If bit 0 is set, FCH will stutter the CPU C state whenever USB EHCI has pending traffic. If bit 1 is set, FCH will cause CPU to break out from C state when USB EHCI has pending traffic. These bits affect AltVid entry and should be set to 01 only when AltVid is enabled; otherwise leave at 00.
TmrSelOverride	20:16	00000b	This is to be used with bit TimerTickChgMsgEn. In case FCH auto-timer detection logic is not functioning properly, one can use these bits to override the logic and force the logic to monitor the specific timer. Bit 0 - When set, use HPET Bit 1 - When set, use RTC Bit 2 - if HPET is selected, setting bit 2 will force the logic to monitor HPET timer 0. Bit 3 - if HPET is selected, setting bit 3 will force the logic to monitor HPET timer 1. Bit 4 - if HPET is selected, setting bit 4 will force the logic to monitor HPET timer2.
DebugBus6Sel	21	0b	0: ACPI debug bus 6 is the SMBUS device ID. 1: ACPI debug bus 6 is debug signals from fusion_c logic.
FusionReadState	22	0b	This is for debugging purpose. When set, bits [15:0] of this register will return FusionC state logic signals.
MultiCoreEn	23	0b	When set, C-state control logic inside FCH will assume multi-core CPU configuration. NumOfCpu (PM_Reg x7A) should be programmed accordingly. FCH keeps track of CPU C state by monitoring each core's C state message instead of package state.
ExtendValue	27:24	00000000b	Timer value to be used with ExtendEnable. The value is the number of 66Mhz clocks.

PM_Reg:A4h is TrafficMonitorEn when bit 31 is 0. If bit 31 is 1, then it returns the traffic status of the respective controller

TrafficMonitorEn - RW – 8/16/32 bits - [PM_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
PerfMonEn	0	0b	When set, FCH will monitor the amount of DMA traffic by the individual enable bits (bits 5 through 12) and the number of interrupts within the monitored interval (defined by bits 25:24)

TrafficMonitorEn - RW – 8/16/32 bits - [PM_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
TrafficSciEn	1	0b	When set, FCH will generate a SCI when the amount of traffic is less than idleTimeLimit.
InterruptEn	2	0b	When set, FCH will monitor the number of interrupts occurring within the monitor period. If the number of interrupts is less than the number defined in IntrTimeLimit, FCH will generate a SCI.
CheckInterrupt	3	0b	To be used with bit 2 to monitor interrupts.
CheckC3	4	0b	To be used with bit 1. When set, FCH will only consider the system is in idle state if CPU is in C state.
CheckGec	5	0b	To be used with bit 1. When set, FCH will monitor GMAC traffic.
CheckSata	6	0b	To be used with bit 1. When set, FCH will monitor SATA traffic.
CheckUsb	7	0b	To be used with bit 1. W hen set, FCH will monitor USB traffic.
CheckPcib	8	0b	To be used with bit 1. When set, FCH will monitor PCIBridge traffic.
CheckAz	9	0b	To be used with bit 1. When set, FCH will monitor HD audio traffic.
CheckLpc	10	0b	To be used with bit 1. When set, FCH will monitor LPC traffic.
CheckGpp	11	0b	To be used with bit 1. W hen set, FCH will monitor GPP traffic.
CheckFc	12	0b	To be used with bit 1. W hen set, FCH will monitor FC (NAND flash) traffic.
LanEnergyDetectEn	13	0b	Enable SCI generation due to LAN energy detect status change.
MaskIntrToCState	14	0b	When set, interrupt will be masked off internally and will not cause FCH to generate Exit message to FusionCPU. This function is only applicable to FusionCPU configuration.
Reserved	23:15	0	Reserved.
PerfMonPeriodSel	25:24	00b	Traffic monitor period selection. To be used when PerfMonEn (bit0) is set to enable. 00: 15ns between each count and the monitored interval is ~1ms. 01: 240ns between each count and the monitored interval is 15.67ms. 10: 1.92µs between each count and the monitored interval is 125.3ms. 11: 15.36µs between each count and the monitored interval is ~1 second.
Reserved	30:26	00000b	Reserved.
PMIO_A4_Sel	31	0b	When it is 0, this register (PM_Reg:A4h) is the TrafficMonitorEn register. When it is 1, this register (PM_Reg:A4) is selected to be TrafficStatus register. In both cases, this bit has same definition.

TrafficStatus - RW – 8/16/32 bits - [PM_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	4:0	00000b	Reserved.
GecTrafficStatus	5	-	Indicates whether GEC is active. 0: Inactive 1: Active
SataTrafficStatus	6	-	Indicates whether SATA is active. 0: Inactive 1: Active

TrafficStatus - RW – 8/16/32 bits - [PM_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
UsbTrafficStatus	7	-	Indicates whether USB is active. 0: Inactive 1: Active
PcibTrafficStatus	8	-	Indicates whether PCIBridge is active. 0: Inactive 1: Active
AzTrafficStatus	9	-	Indicates whether HD audio is active. 0: Inactive 1: Active
LpcTrafficStatus	10	-	Indicates whether LPC is active. 0: Inactive 1: Active
GppTrafficStatus	11	-	Indicates whether GPP is active. 0: Inactive 1: Active
FcTrafficStatus	12	-	Indicates whether FC is active. 0: Inactive 1: Active
GecEnergyDetectStatus	13	-	Indicates whether LAN energy detect is active. 0: Inactive 1: Active
FusionCState	15:14	00b	Status of fusion C state monitor
FusionCState0	17:16	00b	Status of fusion C state monitor for core pair 0
FusionCState1	19:18	00b	Status of fusion C state monitor for core pair 1
FusionCState2	21:20	00b	Status of fusion C state monitor for core pair 2
FusionCState3	23:22	00b	Status of fusion C state monitor for core pair 3
Reserved	30:24	0	Reserved.
PMIO_A4_Sel	31	0b	When it is 0, this register (PM_Reg:A4h) is the TrafficMonitorEn register. When it is 1, this register (PM_Reg:A4) is selected to be TrafficStatus register. In both cases, this bit has same definition.

TrafficMonitorIdleTime - RW – 8/16 bits - [PM_Reg: A8h]			
Field Name	**Bits**	**Default**	**Description**
IdleTimeLimit	15:0	0000h	To be used with PerfMonEn. This defines the amount of DMA traffic limit that will cause FCH to generate SCI. Time granularity is defined by PerfMonPeriodSel.

TrafficMonitorIntTime - RW – 8/16 bits - [PM_Reg: AAh]			
Field Name	**Bits**	**Default**	**Description**
IntrTimeLimit	15:0	0000h	To be used with PerfMonEn. This defines the amount of interrupt limit that will cause FCH to generate SCI. Time granularity is defined by PerfMonPeriodSel.

TrafficMonitorTrafficCount - RW – 8/16 bits - [PM_Reg: ACh]			
Field Name	**Bits**	**Default**	**Description**
TrafficCount	15:0	0000h	Actual recorded value of the combined DMA traffic during the monitored period.

TrafficMonitorIntrCount - RW – 8/16 bits - [PM_Reg: AEh]			
Field Name	**Bits**	**Default**	**Description**
IntrCount	15:0	0000h	Actual recorded value of the number of interrupts during the monitored period.

TrafficMonitorTimeTick - RW – 8/16 bits - [PM_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
DeferTimerTickEn	0	0b	When set, FCH will skip a number of timer tick interrupts based on the defined value in DeterTimeTickValue when CPU is in C state. When CPU is not in C state, FCH will not skip any timer tick interrupts.
ForceTmrTickEn	1	0b	If bit 0 is set along with this bit and FCH has skipped a timer tick interrupt, FCH will immediately generate the timer tick interrupt upon C state exit
DeferTimerTickValue	10:8	000b	000: No skipping 001: Skip 1 timer tick 010: Skip 2 timer ticks 011: Skip 3 timer ticks 100: Skip 4 timer ticks 101: Skip 5 timer ticks 110: Skip 6 timer ticks 111: Skip 7 timer ticks

FidVidControl - RW – 8/16 bits - [PM_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
Fid_protect_en	0	0b	Set to 1 to skip C state transition when FID/VID message is received concurrently.
DelayLDTSTP	8	0b	Set to 1 to enable LDTSTP# assertion time
FidVidOption	11:9	000b	Additonal FIDVID exit delay 3’b000: 0ns 3'b001: 140ns 3'b010: 210ns 3'b011: 280ns 3'b110: 350ns 3'b111: 420ns 3'b100: 490ns 3'b101: 560ns

Reserved - RW – 8 bits - [PM_Reg: B6h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

Tpreset1b – RW – 6 bits – [PM_Reg:B7h]			
Field Name	**Bits**	**Default**	**Description**
Tpreset1b	5:0	05h	Timing parameter used for S* -> S0 state transition. This determines the delay between CPU_STP# de-assertion and SUS_STAT# de-assertion, in 8µs increment with 8µs uncertainty.

TPRESET2 - RW – 8 bits - [PM_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
TPRESET2	5:0	08h	Timing parameter used for S* -> S0 state transitions. This register determines the LDTSTOP**#** deassertion delay in 8µs increment with 8µs uncertainty.

Reserved – RW – 8 bits - [PM_Reg: B9h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

S_StateControl - RW – 8/16 bits - [PM_Reg: BAh]			
Field Name	**Bits**	**Default**	**Description**
LongSLPS3	0	0b	Set to 1 to extend SLP_S3# assertion to 1s minimum.
AllowOffset	1	0b	Set to 1 to add extra delay for STPCLK. Only valid if AgpTimeAdj is set.
Reserved	2	-	
PmeMsgEn	3	0b	Set to 1 to enable PmeTurnOff/PmeMsgAck handshake.
Reserved	11:5	-	
AgpTimeAdj	13	0b	If set to 1, S* -> S0 state transitions will use 1ms clock for timing sequence; otherwise, 8µs clock will be used. For K8 system, this bit must be cleared to use 8µs clock.
WakePinEnable	14	0b	Set to 1 to enable wakeup from WAKE# pin.
MaskPmeMsgEn	15	0b	When set (along with PmeMsgEn=1), PmeAck message coming from PCIe® device will be ignored and ACPI S state logic will solely use the timeout mechanism to sequence through the S3 state. This bit is used as an option to guard against multiple PmeAck messages coming from CNB and internal FCH PCIe bridge so FCH S state logic will not sequence into S3 state prematurely.

ThrottlingControl - RW – 16 bits - [PM_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**
AcpiThrotPeriod	1:0	00b	Selects the software clock throttling period 00: 15µs 01: 30µs 10: 244µs 11: Reserved
ThrottleControl	7:4	000b	Bit[4] Enable thermal clock throttle Bit[3:1] Throttle interval for STPCLK# de-assertion 000b: 50% 001b: 12.5% 010b: 25% 011b: 37.5% 100b: 50% 101b: 62.5% 110b: 75% 111b: 87.5%
ThermThrotPeriod	13	0b	Selects the thermal clock throttle period 0: 30µs 1: 244µs
NoWaitStpGntEn	14	0b	0: Wait for STPGNT after asserting STPCLK. 1: Do not wait for STPGNT after asserting STPCLK.
Therm2SecDelay	15	0b	Enable 2 second delay for thermal clock throttle.

ResetControl - RW – 8/16 bits - [PM_Reg: BEh]			
Field Name	**Bits**	**Default**	**Description**
UserResetEnable	0	1b	Set to 1 to enable Reset Button
Kb_pcirst_en	1	1b	Set to 1 to make PCI reset if KBRST# is asserted
CpuRstControl	3:2	0b	00: CpuReset is deasserted after PciReset. 01: CpuReset is deasserted as PciReset. 10: CpuReset is deasserted before PciReset. 11: CpuReset is deasserted after PciReset.
KbRstEn	4	1b	Set to 1 allow KB_RST# to do the PCI reset.

ResetControl - RW – 8/16 bits - [PM_Reg: BEh]			
Field Name	**Bits**	**Default**	**Description**
SLP_TYPEn Control	5	1b	Set to 1 to enable the function of SLP_TYP in PmControl register [AcpiPm1CntBlk:00h]. The SLP_TYP in PmControl register has no effect if this bit is cleared.
HWM_ResetOption	6	1b	0: Hwm function (Pmio2 register block) is reset by RsmRst. 1: Hwm function (Pmio2 register block) is reset by PciRst.
RstToCpuPwrGdEn	7	0b	If set to 1, FCH toggles CPUPG on every reset.
DelayRomRstEn	9	0b	0: ROM_RST functions the same as PciRst# 1: 30ms ahead of deassertion of PciRst#
DelayLanRstEn	10	0b	0: Lan_RST functions the same as PciRst# 1: 20ms ahead of deassertion of PciRst#
Gpio51ShutdownEn	11	0b	Shutdown system if seeing a negative edge on SHUTDOWN#/Gpio51
Bypass_pwr_good	13	0b	If asserted, Southbridge will not wait for deassertion of PWRGOOD to monitor wakeup events.
PwrGoodOut	14	0b	Output data for PwrGood pin
PwrGoodEnB	15	0b	Output enable for PwrGood pin (active low)

S5/Reset Status - RW – 16 bits - [PM_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
ThermalTrip	0	0b	Write 1 to clear.
4SecondPwrBtn	1	0b	Write 1 to clear.
Shutdown	2	0b	Write 1 to clear.
ThermalTripFromTemp	3	0b	Write 1 to clear.
RemotePowerDownFromASF	4	0b	Write 1 to clear.
ShutDownFan0	5	0b	Write 1 to clear.
ShutDownFan1	6	0b	Write 1 to clear.
ShutDownFan2	7	0b	Write 1 to clear.
ShutDownFan3	8	0b	Write 1 to clear.
ShutDownFan4	9	0b	Write 1 to clear.
DisableLdtPwrGood	12	0b	LdtPwrGood Control. Set this bit to 1 to disable the LdtPwrGood assertion along with NBPwrGood.
DisSbToNbPG	13	0b	Set to1 to disable NBPwrGood.
PmeTurnOffTime	15:14	00b	00: 1ms 01: 2ms 10: 4ms 11: 8ms
UserRst	16	0b	Write 1 to clear.
Soft_pcirst	17	0b	Write 1 to clear.
Do_k8_init	18	0b	Write 1 to clear.
Do_k8_reset	19	0b	Write 1 to clear.
Do_k8_full_reset	20	0b	Write 1 to clear.
UsrRst2NbPwrGdDis	21	0b	SYS_RESET# is an externally generated signal that will reset the SB when asserted. For external clock mode configuration, when this signal is asserted, NB PWRGD should be de-asserted. This can be done by an external circuit or by clearing this bit. (Note this requirement only applies to external clock mode configuration. For internal clock mode configuration, this bit should be set to 1, and there is no need for an external circuit to force NB PWRGD.) 0: Force NBPwrGood to be de-asserted if SYS_RESET# goes low. 1: Do not force NBPwrGood to be de-asserted if SYS_RESET# goes low.
Kb_reset	22	0b	Write 1 to clear.

S5/Reset Status - RW – 16 bits - [PM_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
Lt_reset	23	0b	Write 1 to clear.
FailBootRst	24	0b	Write 1 to clear.
WatchDogIssueReset	25	0b	Write 1 to clear.
RemoteResetFromASF	26	0b	Write 1 to clear.
Sync_flood	27	0b	Write 1 to clear.
Hang_reset	28	0b	Write 1 to clear.
IMC_WatchDogRst	29	0b	Write 1 to clear.
Reserved	31:30		Reserved

MiscFixReg * - RW – 32 bits - [PM_Reg: C0h]			
Field Name	**Bits**	**Default**	Description
Reserved	2:0		Reserved
ClrAllStsInThermalEvent	3	0b	Set to 1 to allow ASF remote power down/power cycle, Thermal event, Fan slow event to clear all the Gevent status and enabled bits. The bit should be set to 1 all the time.
UsbGoodClkDlyEn	4	0b	Set to 1 to delay de-assertion of USB clk by 6 Osc clk. The bit should be set to 1 all the time.
ForceNBCPUPwr	5	0b	Set to 1 to force CPU pwrGood to be toggled along with NB pwrGood.
MergeUsbPerReq	6	0b	Set to 1 to merge USB periodical traffic into USB request as one of break events.
IMCWatchDogRstEn	7	0b	Set to 1 to allow IMC watchdog timer to reset entire ACPI block. The bit should be set to 1 when IMC is enabled.
GeventStsFixEn	8	0b	1: Gevent status is not reset by its enable bit. 0: Gevent status is reset by its enable bit.
PmeTimerFixEn	9	0b	Set to 1 to reset Pme Timer when going to sleep state.
UserRst2ImcEn	10	0b	Set to 1 to route user reset event to IMC. The bit should be set to 1 when IMC is enabled.
Reserved	15:11		Reserved
RTC_STSEnOnSlp	19:16	0000	Set to 1000 to allow RTC_STS to be set only in non-G0 state.
GateSBGppPme	20	0	Set to 1 to gate off the pme message from FCH GPP in non-S0 state.
UsrRst2NbPwrGdDis	21	0	0: NB_PWRGD output will be asserted when SYS_RESET# is asserted (default setting for external clock configuration) 1: NB_PWRGD output will ***NOT*** be asserted when SYS_RESET# is asserted (bit is required to be set for internal clock configuration)
PcieResetEn	22	0	Set to 1 to allow PCIe® to be reset by software.
Reserved	29:23		Reserved
Smbus0ClkStretchEn	30	0b	Set to 1 to enable SMBus0 controller clock stretch support.
Reserved	31		Reserved
***Note:** This register can be either “S5/Reset Status” or “MiscFixReg”, depending on the select bit “ShowMiscFixReg” in PM_Reg C4[2]. The default setting (ShowMiscFixReg=0) selects this register as “S5/Reset Status”; software needs to set ShowMiscFixReg=1 to select this register as MiscFixReg.			

ResetCommand - RW – 8 bits - [PM_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Reset	0	0b	Writing 1 to do a PCI reset
MemRstDisable	1	0b	When set, the memory reset function at DDR_RST# pin will be disabled.
SelectDebug	2	0b	0: Select the PM_Reg C0 to be S5/Reset Status register. 1: Select the PM_Reg C0 to be a debug status register.

ResetCommand - RW – 8 bits - [PM_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
UsrRst2Pll	3	1b	Set to 1 to stop Pll when reset button is pressed.
ResetButtonEnForIMC	5	1b	If it is set to 1, when IMC is enabled, reset from reset button can reset entire ACPI block; otherwise, only part of ACPI block can be reset.
ResetAllAcpi	6	0b	Writing 1 to emulate a Reset Button event.
ResetEn	7	0b	0: Not allow to write bit 0 1: Allow to write bit 0.

CF9Shadow – RW – 8 bits – [PM_Reg:C5h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0		Reserved
SysRst	1	0b	0: Send INIT HT message 1: Reset as specified by bit3
RstCmd	2	0b	Write with 1 to generate reset as specified by bit[3,1]. Write only. Always read as 0.
FullRst	3	0b	0: Assert reset signals only 1: Place system in S5 state for 3 to 5 seconds
Reserved	7:4		Reserved

HTControl - RW – 16 bits - [PM_Reg: C6h]			
Field Name	**Bits**	**Default**	**Description**
HtIdleInterval	2:0	00b	This registers define the idle time between the two LDTSTP# assertions.
HtBistStart	6	0b	This bit is write only. Always return 0 when read. Writing to this bit will start the K8 BIST. Basically FCH will assert LDTSTP# for an interval defined by HT_AssertInterval, wait for an interval defined by HT_TimeInterval, then assert LDTSTP# again.
HtTimeInterval	7	0b	This bit defines HTIdle Interval. 0: Microsecond 1: Millisecond
HtAssertInterval	10:8	0b	This field defines the assertion time.
HtDelayStartTime	13:12	00b	This field defines the delay start time associated with the function in C6[6]h. The values are in microseconds. This is to allow the write to C6h[6] to be complete before FCH execute the test function.

Misc - RW – 32 bits - [PM_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
CPU_IO_PullDownDrvStrength	0	0b	When set, the integrated pull-down drive strength of all CPU IOs are increased by 50%.
BG1RESDIV0_SEL	1	0b	This bit controls the CPU receiver Vref 0: Vref = Vcpu / 2 1: Vref = Vbandgap / 2 = 0.6v (recommended)
TFATAL_EN	2	1b	This bit enables both the soft PCIRST and the THRMTRIP function.
TDeadEn	3	1b	When set, GEVENT2 takes up the THRMTRIP function. When THRMTRIP pin is low and TFATAL_EN(bit2 of the same register) is set, hardware will switch the system to S5 automatically.
oUseAcpiStraps	4	0b	When set, it will use the config bits from index D8h and D9h to override the EpromStraps.

Misc - RW – 32 bits - [PM_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
Eprom/EFuseIndex Select	5	0b	If this bit is 0, PMIO D8h and D9h are for accessing the EPROM strap bits. When this bit is set to 1, PMIO D8h and D9h is for accessing the Efuse bits.
TwarnEn	6	0b	If set, it enables TALLERT pin to affect ACPI functions. This register controls the action of the TALLERT# (GPIO176) pin of the FCH. The pin is used to indicate high temperature condition of the external device.
DisablePciRom	7	0b	Set to 1 to disable PCI from strap.
Temp_polarity	9:8	00b	Temperature polarity control for THRMTRIP and TALERT respectively. 0: Active low 1: Active high
LLB_En	10	0b	If set, LLB function is enabled, and system won't wakeup from ACPI S state until LLB# is de-asserted.
WriteBackEnable	11	0b	AZ write back enable. If set, the WakeOnRing status bit will be written back to HD Audio controller upon system power up.
S5ResetOverride	12	0b	Set to 1 to mask off internet PCI reset used in ACPI.
Id_change_en	13	0b	Setting this bit will allow the software to change the DeviceID and RevisionID.
SmBarHid	14	1b	Set to1 to hide scratch registers in SMBus PCI cfg space.
HideSmbus	15	0b	Set to1 to hide SMBus PCI cfg space and Lpc bridge is promoted to function 0.
BypassRomSel	17:16	00b	These two bits will override the two ROM strap pins. 00: LPC ROM 10: FWH ROM 11: SPI ROM 01: Reserved
UseBypassRom	18	0b	When this bit is set, it will override the ROM straps and use bits 3:2 of this register to determine which type of ROM to use. This is for BIOS debugging purpose or for system having multiple BIOSes on board.
UseCpuRst	19	1b	If this bit is not set, system reset will cause INIT# instead of CPURST#.
ProcHotStsEn	20	0b	Set to enable PROCHOT# to generate TwarnStatus and thermal throttle.
SpiDrvStr	21	1b	Set to 1 to enhance SPIHoldB drive strength.
ClkIntrVectorOrdEn	22	0b	When set, the system timer interrupt in the IOAPIC will be tagged with a value defined by ClkIntrVectorOrd
ClkIntrVectorOrd	31:24	00000000b	Specify the value used to indentify the clock interrupt.

IoDrvSth - RW – 8/16/32 bits - [PM_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
IoDrvSth_AD	2:0	111b	I/O drive strength* for AD[31:0], CBE0#, CBE1#, CBE2#, CBE3# , PAR, FRAME#, IRDY#, DEVSEL#, TRDY#, LOCK#, STOP#, PERR#, SERR#, CLKRUN#, and PCIRST#.
IoDrvSth_GNT	5:3	111b	I/O drive strength* for GNT#[4:0] pads.
IoDrvSth_ClkGrpA	8:6	111b	I/O drive strength* for PCICLK0 pads. The recommended setting for single load is 000b.

IoDrvSth - RW – 8/16/32 bits - [PM_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
IoDrvSth_ClkGrpB	11:9	111b	I/O drive strength* for PCICLK[4:1] pads. The recommended setting for single load is 000b.
IoDrvSth_LPC	14:12	111b	I/O drive strength* for LPC LAD, LFRAME# pads. The recommended setting for single load is 111b.
IoDrvSth_Int	17:15	111b	I/O drive strength* for INTA#, INTB#, INTC#, INTD#, INTE#, INTF#, INTG#, and INTH# pads.
IoDrvSth_Req	20:18	111b	I/O drive strength* for REQ[3:0]# when they are configured as GPIO.
IoDrvSth_GpioA	23:21	111b	I/O drive strength* for BMREQ#, GPIO[0, 2, 4, 5, 7, 8, 9, 13, 37, 38, 39, 40], GPOC[0, 1] pads.
IoDrvSth_GpioB	26:24	111b	I/O drive strength* for GPIO3, and GPIO[48:52] pads.
IoDrvSth_Misc	29:27	111b	I/O drive strength* for GA20, KBRST#, SERIRQ, and SATA_ACT# pads.
IoDrvSth_IDE	31:30	11b	I/O drive strength* for IDE interface.

***Note:** IO Drive Strength: Each three bit field controls the number of P and N transistors enabled in the final stage of the output driver for the designated pads. By controlling the number of transistors enabled, the designer can optimize the drive characteristics of signals based on the topology of their specific design.

Reserved - RW – 8 bits - [PM_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	-	

PmioDebug - RW – 8 bits - [PM_Reg: D2h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	-	
LpcClkDrvSth	5:4	00b	Drive strength control for LpcClk[1:0] respectively. 0: Clock output will be 4mA 1: Clock output will be 8mA
IsaPmEn	7	0b	Set to 1 to allow legacy method of IO CD6/CD7 to access Pm register block.

IMCGating - RW – 8/16 bits - [PM_Reg: D6h]			
Field Name	**Bits**	**Default**	**Description**
IMC_GA20_Enable	0	0b	Set to1 to enable IMC A20# request.
IMC_KBRST_Enable	1	0b	Set to1 to enable IMC KBRST# request.
IMC_IRQ1_Enable	2	0b	Set to1 to enable IMC IRQ1 request.
IMC_IRQ12_Enable	3	0b	Set to1 to enable IMC IRQ12 request.

Eprom/EfuseIndex - RW – 8 bits - [PM_Reg: D8h]			
Field Name	**Bits**	**Default**	**Description**
Eprom/EfuseIndex	7:0	00h	Index register to access Eprom setting (PM_regxC8[5]=0) or Efuse bits (PM_regxC8[5]=1). Write to this port sets the initial value of the index. Writing to the EpromStrapData port will auto-increment this index. Programming through the index/data port will not take effect until the next reset. This register is used as the index register to read the value of efuse when PM_regxC8[5] is set to 1.

Eprom/EfuseData - RW – 8 bits - [PM_Reg: D9h]			
Field Name	**Bits**	**Default**	**Description**
Eprom/EfuseData	7:0	00h	Data register to access Eprom bits (PM_regxC8[5] =0) or Efuse bits (PM_regxC8[5]=1). Writing to the EpromStrapData port will auto-increment the index at PMIO_CCh. Programming through the index/data port will not take effect until the next reset. This register is used as the data register to read the value of efuse when PM_regxC8[5] is set to 1.

SataConfig - RW – 16 bits - [PM_Reg: DAh]			
Field Name	**Bits**	**Default**	**Description**
SataEnable	0	1b	**0**: SATA controller is disabled **1**: SATA controller is enabled
channel_sel	1	0b	**0**: SATA Port4 and Port5 utilizing Primary IDE channel **1**: SATA Port4 and Port5 utilizing Secondary IDE channel
SetMaxGen2	2	0b	**0**: SATA controller supports 1.5Gb/s, 3.0Gb/s and 6.0 Gb/s speeds. **1**: SATA controller supports 1.5 Gb/s and 3.0 Gb/s speeds. This option can be used if the system configuration will not support Gen3 (6.0 Gbs SATA devices). Internal PLL power consumption will be lower than that with option set to support Gen3 devices.
HiddenIDE	3	0b	**0**: IDE controller is exposed and Combined Mode is enabled. SATA controller has control over Port0 through Port3, IDE controller has control over Port4 and Port5 **1**: IDE controller is hidden and Combined Mode is disabled, SATA controller has full control of all 6 Ports when operating in non-IDE mode
Ref_Clk_Sel	5:4	00b	This is CP_PLL_REFCLK_SEL, the reference clock source selection for SATA PLL. **00/10**: Reference clock from crystal oscillator via PAD_XTALI and PAD_XTALO **01**: Reference clock from internal clock through CP_PLL_REFCLK_P and CP_PLL_REFCLK_N via RDL **11**: same as 01
Ref_Div_Sel	7:6	00b	This is CP_PLL_CLKR, the reference clock divider setting. **00**: Divide by 1 (25MHz reference clock) **01**: Divide by 2 **10**: Divide by 4 (100MHz reference clock) **11**: same as 10.
Reserved	15:8	-	

Reserved - RW – 8bits - [PM_Reg: DCh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	6:0	-	
GPIO160 control0	7	1	Enables GPIO160 1 = disable 0 = Enable

Reserved - RW – 16bits - [PM_Reg: DEh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	-	

BlinkControl - RW – 8bits - [PM_Reg: DFh]			
Field Name	**Bits**	**Default**	**Description**
BlinkControl	1:0	00b	B-Link interval select 00: Always off (*see Note) 01: 1sec on, 3 sec off, repeating 10: 2 sec on, 2 sec off, repeating 11: Always on Note: B-Link is not supported as per erratum # 2. Also, B-Link is multiplexed with Gevent18. If Gevent18 Function is used, B-Link must be disabled by programming '00'.
Reserved	7:2	-	

ABRegBar - RW – 32 bits - [PM_Reg: E0h]			
Field Name	**Bits**	**Default**	**Description**
ABRegBar	31:0	00000000h	IO Base address of UMI register.

Reserved - RW – 16bits - [PM_Reg: E6h]			
Field Name	**Bits**	**Default**	**Description**
GPIO160 Control1	0	0	Enables GPIO160 0 = disable 1 = Enable
GPIO160 Control2	1	1	Enables GPIO160 0 = Enable 1 = Disable
Reserved	15:2	-	

PcibConfig - RW – 8 bits - [PM_Reg: EAh]			
Field Name	**Bits**	**Default**	**Description**
PCIDisable	0	0b	Set to 1 to disable P2P bridge from monitoring the PCI interface input I/O and enable PCI interface pins to function as GPIO {GPIO 35:0}
PciBridgeMIoOverride	1	0b	When set, PCIBridge (Device 20h, function 4) memory and I/O enable is always true, even if the bits are set to 0.

AzEn - RW – 8 bits - [PM_Reg: EBh]			
Field Name	**Bits**	**Default**	**Description**
AzEnable	0	1b	0: Disable HD audio controller 1: Enable HD audio controller
AzNoSnoopEnable	1	0b	When set, HD AUDIO data transfer will not cause the BM_STS bit to be set and to wake up the CPU from C3 state.

LpcGating - RW – 8 bits - [PM_Reg: ECh]			
Field Name	**Bits**	**Default**	**Description**
Lpc_enable	0	1b	Set to 1 to enable LPC bridge
Lpc_a20en	1	0b	Set to1 to enable A20# input.

UsbGating - RW – 8 bits - [PM_Reg: EDh]			
Field Name	**Bits**	**Default**	**Description**
Usb_a20_en	0	0b	Set to 1 to enable USB A20#.
Usb_irq_en	1	0b	Set to1 to route IRQ1/IRQ12 from usb to PIC/IIOAPIC.
Usb_smi_en	4	0b	Set to 1 to enable USB SMI#.

UsbEnable – RW – 8 bits – [PM_Reg:EFh]			
Field Name	**Bits**	**Default**	**Description**
USB1 OHCI Enable	0	1b	Enable bit for USB1 OHCI controller (device-18).
USB1 EHCI Enable	1	1b	Enable bit for USB1 EHCI controller (device-18).
USB2 OHCI Enable	2	1b	Enable bit for USB2 OHCI controller (device-19).
USB2 EHCI Enable	3	1b	Enable bit for USB2 EHCI controller (device-19).
USB3 OHCI Enable	4	1b	Enable bit for USB3 OHCI controller (device-22).
USB3 EHCI Enable	5	1b	Enable bit for USB3 EHCI controller (device-22).
USB4 OHCI Enable	6	1b	Enable bit for USB4 OHCI controller (device-20).
Reserved	7	1b	Reserved

UsbControl - RW – 16 bits - [PM_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
UsbPhyS5PwrDwnEnable	0	0b	Setting this bit to '1' will enable the PHY to be powered down in S4/S5 state. (Assuming the power to the PHY is connected to S5 rail the PHY will not consume power with this bit set.) If the system requirments are to have the system wake from USB devices, then this bit should be left at the default value of '0'. Powering down the PHY will prevent the device to initiate wake to the system. Hardware power-up default is 0b. For ASIC revision A11 (non-production and sample parts only) this bit has different polarity, i.e., set to 1 to disable S4/S5 USB PHY power-down support and to enable S4 USB wake-up support.
Reserved	1	-	
UsbKbResetEnable	2	1b	Set to 1 to enable resetting USB on KB reset.
UsbS5ResetEnable	3	1b	Set to 1 to enable USB reset on S4/S5 resume detection.
Usb11PdResistorEnable	4	1b	Set to 0 to disconnect pull-down resistors on stand-alone USB1.1 pads.
Reserved	5	0b	Reserved
Reserved	6	-	
UsbResumeEnable	7	1b	Set to 1 to enable S3 wakeup on USB device resume.

UsbControl - RW – 16 bits - [PM_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
UsbSleepCtrl	10:8	011b	Control on USB advanced async sleep function. Setting of 000b:100b are for the advanced async sleep. Default is standard async sleep. 000b: Standard 10µs sleep 001b: Advanced sleep up to 2 uframes 010b: Advanced sleep up to 4 uframes **011b: Advanced sleep up to 6 uframes (default)** 100b: Advanced sleep up to next uframe 0 101b, 110b: Reserved 111b, EHCI will stop fetching descriptor once it has completed the list while CPU is in C state
Reserved	15:11	00000b	Reserved

UsbDebug - RW – 8 bits - [PM_Reg: F3h]			
Field Name	**Bits**	**Default**	**Description**
ForceReset2USB	2:0	00h	These are software control bits that can be used to force resetting of USB host controllers. Each bit corresponds to one USB major function.
ForcePHYPwrDown	3	0b	Forces USB PHY into power down mode.
ForcePHYPLLReset	4	0b	Forces USB PHY PLL reset.
ForcePHYDLLreset	5	0b	Forces USB PHY DLL reset.
ForcePHYEarlyReset	6	0b	Forces USB PHY early reset.
ForcePHYPortReset	7	0b	Forces USB PHY port reset.

GecEn - RW – 8/16 bits - [PM_Reg: F6h]			
Field Name	**Bits**	**Default**	**Description**
GecDisable	0	0b	Set to 1 to disable Gec.
TstGecMiiMode	1	0b	Reserved for testing only.
GecSpiDebugEn	2	0b	If set, this will route the GEC's flash interface directly onto FCH's SPI interface. Note under this scenario, platform should use LPC flash for BIOS so there is no contention between BIOS and the integrated GEC MAC
GecSerialDebugEn	3	0b	If set, this will enable the serial debug port for the integrated GEC
Reserved	4	0b	Reserved
GecManualRst	5	0b	Setting this bit will force the integrated Ethernet MAC to be in reset state.
GecGpioDrvStr	6	0b	Drive strength control for MDCK, MDIO, PHY_RESET#, PHY_PD, and LED0 pins. 0: 4mA 1: 8 mA
Reserved	10:8	001b	Reserved
Reserved	12:11	00b	Reserved
Reserved	15:13	001b	Reserved.

GecConfig – RW – 8/16/32 bits – [PM_Reg: F8h]			
Field Name	**Bits**	**Default**	**Description**
GecBypassClkSel	0	0b	Set to1 to enable Gec bypass clock.
GecRxTerm	1	0b	Enable RX termination This bit must be set to 0 (disable RX termination)
GecTxDrvMode	2	0b	1b = RGMII output driver in CMOS mode This bit must be set to 1
GecRxRec33_25	3	1b	Set to 1 to enable RX receivers in CMOS mode This bit must be set to 1

GecConfig – RW – 8/16/32 bits – [PM_Reg: F8h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	4	0b	Reserved
GecPwrPolicy	6:5	11b	BIOS should set these two bits according to the platform configuration. These configuration bits are used for internal power-domain-crossing logic. When GEC is powered down, signals from GEC power domain are gated off in the S5 power domain 00b: GEC is powered down in S3 and S5. 01b: GEC is powered down only in S5. 10b: GEC is powered down only in S3. 11b: GEC is never powered down.
GecShadowRomIntrSel	7	0b	0: Generate SMI# when GEC shadow ROM is updated 1: Generate interrupt to IMC when GEC shadow ROM is updated
GecDrvStrP2	10:8	001b	RGMII output driver drive strength control 000b: Weakest 001b: 011b: 111b: Strongest
Reserved	12:11	00b	Reserved
Reserved	15:13	001b	Reserved
GecRef	18:16	100b	VREF setting for RX receivers. These bits must be set to 000b.

TraceMemoryEn – RW – 8/16/32 bits – [PM_Reg: FCh]			
Field Name	**Bits**	**Default**	**Description**
TraceMemoryEn	0	0b	Set to 1 to enable trace memory decoding
TraceMemoryBaseAddr	31:20	000h	The base address of trace memory. It is 1M memory space.

2.3.4 Power Management Block 2 (PM2) Registers

PM2 registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from "AcpiMMioAddr" + 0x400 to "AcpiMMioAddr" + 0x4FF.

The base address "AcpiMMioAddr" is defined in PM_reg x24, with the default base address at "FED8_0000."

Register Name	Offset Address
Fan0InputControl	00h
Fan0Control	01h
Fan0Freq	02h
LowDuty0	03h
MedDuty0	04h
Multiplier0	05h
LowTemp0Lo	06h
LowTemp0Hi	07h
MedTemp0Lo	08h
MedTemp0Hi	09h
HighTemp0Lo	0Ah
HighTemp0Hi	0Bh
LinearRange0	0Ch
LinearHoldCount0	0Dh

Register Name	Offset Address
Fan1InputControl	10h
Fan1Control	11h
Fan1Freq	12h
LowDuty1	13h
MedDuty1	14h
Multiplier1	15h
LowTemp1Lo	16h
LowTemp1Hi	17h
MedTemp1Lo	18h
MedTemp1Hi	19h
HighTemp1Lo	1Ah
HighTemp1Hi	1Bh
LinearRange1	1Ch
LinearHoldCount1	1Dh
Fan2InputControl	20h
Fan2Control	21h
Fan2Freq	22h
LowDuty2	23h
MedDuty2	24h
Multiplier2	25h
LowTemp2Lo	26h
LowTemp2Hi	27h
MedTemp2Lo	28h
MedTemp2Hi	29h
HighTemp2Lo	2Ah
HighTemp2Hi	2Bh
LinearRange2	2Ch
LinearHoldCount2	2Dh
FanInputControl3	30h
Fan3Control	31h
Fan3Freq	32h
LowDuty3	33h
MedDuty3	34h
Multiplier3	35h
LowTemp3Lo	36h
LowTemp3Hi	37h
MedTemp3Lo	38h
MedTemp3Hi	39h
HighTemp3Lo	3Ah
HighTemp3Hi	3Bh
LinearRange3	3Ch
LinearHoldCount3	3Dh
Fan4InputControl	40h
Fan4Control	41h
Fan4Freq	42h
LowDuty4	43h
MedDuty4	44h
Multiplier4	45h
LowTemp4Lo	46h
LowTemp4Hi	47h
MedTemp4Lo	48h
MedTemp4Hi	49h
HighTemp4Lo	4Ah

Register Name	Offset Address
HighTemp4Hi	4Bh
LinearRange4	4Ch
LinearHoldCount4	4Dh
FanStatus	60h
FanINTRouteLo	61h
FanINTRouteHi	62h
SampleFreqDiv	63h
FanDebounceCounterLo	64h
FanDebounceCounterHi	65h
Fan0DetectorControl	66h
Fan0SpeedLimitLo	67h
Fan0SpeedLimitHi	68h
Fan0SpeedLo	69h
Fan0SpeedHi	6Ah
Fan1DetectorControl	6Bh
Fan1SpeedLimitLo	6Ch
Fan1SpeedLimitHi	6Dh
Fan1SpeedLo	6Eh
Fan1SpeedHi	6Fh
Fan2DetectorControl	70h
Fan2SpeedLimitLo	71h
Fan2SpeedLimitHi	72h
Fan2SpeedLo	73h
Fan2SpeedHi	74h
Fan3DetectorControl	75h
Fan3SpeedLimitLo	76h
Fan3SpeedLimitHi	77h
Fan3SpeedLo	78h
Fan3SpeedHi	79h
Fan4DetectorControl	7Ah
Fan4SpeedLimitLo	7Bh
Fan4SpeedLimitHi	7Ch
Fan4SpeedLo	7Dh
Fan4SpeedHi	7Eh
TempStatus	90h
TempControl0	91h
TempControl1	92h
TempINTRoute0	93h
TempINTRoute1	94h
IntTempLo	95h
IntTempHi	96h
IntTempLimitLo	97h
IntTempLimitHi	98h
Temp0Lo	99h
Temp0Hi	9Ah
Temp0LimitLo	9Bh
Temp0LimitHi	9Ch
Temp1Lo	9Dh
Temp1Hi	9Eh
Temp1LimitLo	9Fh
Temp1LimitHi	A0h
Temp2Lo	A1h
Temp2Hi	A2h

Register Name	Offset Address
Temp2LimitLo	A3h
Temp2LimitHi	A4h
Temp3Lo	A5h
Temp3Hi	A6h
Temp3LimitLo	A7h
Temp3LimitHi	A8h
VoltageStatus	B0h
VoltageControl0	B2h
VoltageControl1	B3h
VoltageINTRout0	B5h
VoltageINTRout1	B6h
Voltage0Lo	B8h
Voltage0Hi	B9h
Voltage0LimitLo	Bah
Voltage0LimitHi	BBh
Voltage1Lo	BCh
Voltage1Hi	BDh
Voltage1LimitLo	BEh
Voltage1LimitHi	BFh
Voltage2Lo	C0h
Voltage2Hi	C1h
Voltage2LimitLo	C2h
Voltage2LimitHi	C3h
Voltage3Lo	C4h
Voltage3Hi	C5h
Voltage3LimitLo	C6h
Voltage3LimitHi	C7h
Voltage4Lo	C8h
Voltage4Hi	C9h
Voltage4LimitLo	CAh
Voltage4LimitHi	CBh
Voltage5Lo	CCh
Voltage5Hi	CDh
Voltage5LimitLo	CEh
Voltage5LimitHi	CFh
Voltage6Lo	D0h
Voltage6Hi	D1h
Voltage6LimitLo	D2h
Voltage6LimitHi	D3h
Voltage7Lo	D4h
Voltage7Hi	D5h
Voltage7LimitLo	D6h
Voltage7LimitHi	D7h
AlertThermaltripStatus	E0h
AlertLimitLo	E1h
AlertLimitHi	E2h
ThermalTripLimitLo	E3h
ThermalTripLimitHi	E4h
AlertThermaltripControl	E5h
HwmControl	E6h
VoltageReadFreq	E7h
TempReadFreq	E8h
VoltageReadAverage	E9h

Register Name	Offset Address
Hwm_VoltCalib	EAh
TempReadAverage	EBh
HwmStatus	ECh
VoltageReadStatus	EDh
TempReadStatus	EEh
HwmClkControl	EFh
ADC_PDBTime	F0h
ADC_StartUp	F1h
ADC_Delay	F2h
SAX_CTL_VTime	F3h
SAX_CTL_TTime	F4h
BGADJ	F5h
AFEcfg_Clkdiv	F6h
Hwm_DebugSel	F7h
VoltageSampleSel	F8h
TempSampleSel	F9h
HwmVoltage_div0	FAh
HwmVoltage_div1	FBh
Adc_Gain_Adj	FCh
Adc_cfg	FDh
Test_cntl	FEh
HwmMiscControl	FFh

Fan0InputControl - RW – 8 bits - [PM2_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut0 is enabled and temperature input is from internal diode. 001: FanOut0 is enabled and temperature input is from Temp0. 010: FanOut0 is enabled and temperature input is from Temp1. 011: FanOut0 is enabled and temperature input is from Temp2. 100: FanOut0 is enabled and temperature input is from Temp3. 101: FanOut0 is disabled. 110: FanOut0 is enabled and temperature input is 0. 111: FanOut0 is disabled.

Fan0InputControl - RW – 8 bits - [PM2_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Notes: When the fan control is not in AutoMode, the active fan duty cycle is set by LowDuty register. When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function. (a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duly cycle. (b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below: When Actual Temperature < LowTemp, DutyCycle = 0 When Actual Temperature > LowTemp and Actual Temperature < MedTemp; DutyCycle = LowDuty When Actual Temperature > MedTemp and Actual Temperature < HighTemp DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty When Actual Temperature > HighTemp DutyCycle = max or 100% In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.			

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Fan0Control - RW – 8 bits - [PM2_Reg: 01h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut0 controlled by the temperature input; controlled by LowDuty0 otherwise.
LinearMode	1	0b	0: Use step function. 1: Use Linear function.
FanPolarity	2	0b	0: FanOut0 drives low. 1: FanOut0 drives high.
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under Linear mode.

Fan0Freq - RW – 8 bits - [PM2_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
FanFreq	7:0	00h	FanOut0 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7: Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally, 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz

LowDuty0 - RW – 8 bits - [PM2_Reg: 03h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	Fan0 Duty number when temperature is more than lowTemp0 and lower than MedTemp0. There are 256 time slots in one Fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

MedDuty0 - RW – 8 bits - [PM2_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	Fan0 Duty number when temperature is more than MedTemp0 and lower than HighTemp0. There are 256 time slots in one Fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot0 ~ slotN, and stops from slot(N+1) ~ slot255. 00: Always stop … FF: Full speed run

Multiplier0 - RW – 8 bits - [PM2_Reg: 05h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when Fan0 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp0Lo – RW – 8 bits - [PM2_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp0[7:0]. Lower bits of low temperature threshold.

LowTemp0Hi - RW – 8 bits - [PM2_Reg: 07h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp0[15:8]. Higher bits of low temperature threshold.

MedTemp0Lo - RW – 8 bits - [PM2_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp0[7:0]. Lower bits of medium temperature threshold.

MedTemp0Hi - RW – 8 bits - [PM2_Reg: 09h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp0[15:8]. Higher bits of medium temperature threshold.

HighTemp0Lo - RW – 8 bits - [PM2_Reg: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp0[7:0]. Lower bits of high temperature threshold.

HighTemp0Hi - RW – 8 bits - [PM2_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp0[15:8]. Higher bits of high temperature threshold.

LinearRange0 - RW – 8 bits - [PM2_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that Fan0 can tolerate. Fan0 will not be affected if temperature varies within this range.

LinearHoldCount0 - RW – 8 bits - [PM2_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan cycle to be waited before duty cycle can be changed.

Fan1InputControl - RW – 8 bits - [PM2_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut1 is enabled and temperature input is from Internal diode. 001: FanOut1 is enabled and temperature input is from Temp0. 010: FanOut1 is enabled and temperature input is from Temp1. 011: FanOut1 is enabled and temperature input is from Temp2. 100: FanOut1 is enabled and temperature input is from Temp3. 101: FanOut1 is disabled. 110: FanOut1 is enabled and temperature input is 0. 111: FanOut1 is disabled.

Notes:

When the fan control is not in AutoMode the active fan duty cycle is set by LowDuty register.

When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function.

(a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duty cycle.

(b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below:

When Actual Temperature < LowTemp,

DutyCycle = 0

When Actual Temperature > LowTemp and Actual Temperature < MedTemp;

DutyCycle = LowDuty

When Actual Temperature > MedTemp and Actual Temperature < HighTemp

DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty

When Actual Temperature > HighTemp

DutyCycle = max or 100%

In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.

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Fan1Control - RW – 8 bits - [PM2_Reg: 11h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut1 controlled by the temperature input; controlled by LowDuty1 otherwise.
LinearMode	1	0b	0: Use step function. 1: Use Linear function.
FanPolarity	2	0b	0: FanOut1 drives low. 1: FanOut1 drives high.
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under Linear mode.

Fan1Freq - RW – 8 bits - [PM2_Reg: 12h]			
Field Name	**Bits**	**Default**	**Description**
FanFreq	7:0	00h	FanOut1 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7 Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz.

LowDuty1 - RW – 8 bits - [PM2_Reg: 13h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	Fan0 Duty number when temperature is more than lowTemp1 and lower than MedTemp0. There are 256 time slots in one Fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop .. FF: Full speed run

MedDuty1 - RW – 8 bits - [PM2_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	Fan0 Duty number when temperature is more than MedTemp0 and lower than HighTemp1. There are 256 time slots in one Fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

Multiplier1 - RW – 8 bits - [PM2_Reg: 15h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when FanOut1 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp1Lo – RW – 8 bits - [PM2_Reg: 16h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp1[7:0]. Lower bits of low temperature threshold.

LowTemp1Hi - RW – 8 bits - [PM2_Reg: 17h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp1[15:8]. Higher bits of low temperature threshold.

MedTemp1Lo - RW – 8 bits - [PM2_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp1[7:0]. Lower bits of medium temperature threshold.

MedTemp1Hi - RW – 8 bits - [PM2_Reg: 19h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp1[15:8]. Higher bits of medium temperature threshold.

HighTemp1Lo - RW – 8 bits - [PM2_Reg: 1Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp1[7:0]. Lower bits of high temperature threshold.

HighTemp1Hi - RW – 8 bits - [PM2_Reg: 1Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp1[15:8]. Higher bits of high temperature threshold.

LinearRange1 - RW – 8 bits - [PM2_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that FanOut1 can tolerate. FanOut1 will not be affected if temperature varies within this range.

LinearHoldCount1 - RW – 8 bits - [PM2_Reg: 1Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan Cycle to be waited before duty cycle can be changed.

Fan2InputControl - RW – 8 bits - [PM2_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut2 is enabled and temperature input is from Internal diode 001: FanOut2 is enabled and temperature input is from Temp0. 010: FanOut2 is enabled and temperature input is from Temp1. 011: FanOut2 is enabled and temperature input is from Temp2. 100: FanOut2 is enabled and temperature input is from Temp3. 101: FanOut2 is disabled. 110: FanOut2 is enabled and temperature input is 0. 111: FanOut2 is disabled.

Notes:

When the fan control is not in AutoMode, the active fan duty cycle is set by LowDuty register.

When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function.

(a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duty cycle.

(b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below:

When Actual Temperature < LowTemp,

DutyCycle = 0

When Actual Temperature > LowTemp and Actual Temperature < MedTemp;

DutyCycle = LowDuty

When Actual Temperature > MedTemp and Actual Temperature < HighTemp

DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty

When Actual Temperature > HighTemp

DutyCycle = max or 100%

In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.

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Fan2Control - RW – 8 bits - [PM2_Reg: 21h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut2 controlled by the temperature input; controlled by LowDuty2 otherwise.
LinearMode	1	0b	0: Use step function 1: Use Linear function
FanPolarity	2	0b	0: FanOut2 drives low 1: FanOut2 drives high
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under Linear mode.

Fan2Freq - RW – 8 bits - [PM2_Reg: 22h]			
Field Name	**Bits**	**Default**	**Description**
FanFreq	7:0	00h	FanOut2 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7: Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz

LowDuty2 - RW – 8 bits - [PM2_Reg: 23h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	Fan0 Duty number when temperature is more than lowTemp2 and lower than MedTemp2. There are 256 time slots in one fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

MedDuty2 - RW – 8 bits - [PM2_Reg: 24h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	FanOut2 Duty number when temperature is more than MedTemp2 and lower than HighTemp2. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

Multiplier2 - RW – 8 bits - [PM2_Reg: 25h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when FanOut2 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp2Lo – RW – 8 bits - [PM2_Reg: 26h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp2[7:0]. Lower bits of low temperature threshold.

LowTemp2Hi - RW – 8 bits - [PM2_Reg: 27h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp2[15:8]. Higher bits of low temperature threshold.

MedTemp2Lo - RW – 8 bits - [PM2_Reg: 28h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp2[7:0]. Lower bits of medium temperature threshold.

MedTemp2Hi - RW – 8 bits - [PM2_Reg: 29h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp2[15:8]. Higher bits of medium temperature threshold.

HighTemp2Lo - RW – 8 bits - [PM2_Reg: 2Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp2[7:0]. Lower bits of high temperature threshold.

HighTemp2Hi - RW – 8 bits - [PM2_Reg: 2Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp2[15:8]. Higher bits of high temperature threshold.

LinearRange2 - RW – 8 bits - [PM2_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that FanOut2 can tolerate. FanOut2 will not be affected if temperature varies within this range.

LinearHoldCount2 - RW – 8 bits - [PM2_Reg: 2Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan Cycle to be waited before duty cycle can be changed.

Fan3InputControl - RW – 8 bits - [PM2_Reg: 30h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut3 is enabled and temperature input is from Internal diode. 001: FanOut3 is enabled and temperature input is from Temp0. 010: FanOut3 is enabled and temperature input is from Temp1. 011: FanOut3 is enabled and temperature input is from Temp2. 100: FanOut3 is enabled and temperature input is from Temp3. 101: FanOut3 is disabled. 110: FanOut3 is enabled and temperature input is 0. 111: FanOut3 is disabled.

Notes:

When the fan control is not in AutoMode, the active fan duty cycle is set by LowDuty register.

When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function.

(a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duty cycle.

(b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below:

When Actual Temperature < LowTemp,

DutyCycle = 0

When Actual Temperature > LowTemp and Actual Temperature < MedTemp;

DutyCycle = LowDuty

When Actual Temperature > MedTemp and Actual Temperature < HighTemp

DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty

When Actual Temperature > HighTemp

DutyCycle = max or 100%

In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.

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Fan3Control - RW – 8 bits - [PM2_Reg: 31h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut3 controlled by the temperature input; controlled by LowDuty3 otherwise.
LinearMode	1	0b	0: Use step function 1: Use Linear function
FanPolarity	2	0b	0: FanOut3 drives low 1: FanOut3 drives high
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under Linear mode.

Fan3Freq - RW – 8 bits - [PM2_Reg: 32h]			
Field Name	**Bits**	**Default**	Description
FanFreq	7:0	00h	FanOut3 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7: Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz

LowDuty3 - RW – 8 bits - [PM2_Reg: 33h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	FanOut3 Duty number when temperature is more than lowTemp2 and lower than MedTemp2. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop ... FF: Full speed run

MedDuty3 - RW – 8 bits - [PM2_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	FanOut3 Duty number when temperature is more than MedTemp3 and lower than HighTemp3. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

Multiplier3 - RW – 8 bits - [PM2_Reg: 35h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when FanOut3 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp3Lo – RW – 8 bits - [PM2_Reg: 36h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp3[7:0]. Lower bits of low temperature threshold.

LowTemp3Hi - RW – 8 bits - [PM2_Reg: 37h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp3[15:8]. Higher bits of low temperature threshold.

MedTemp3Lo - RW – 8 bits - [PM2_Reg: 38h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp3[7:0]. Lower bits of medium temperature threshold.

MedTemp3Hi - RW – 8 bits - [PM2_Reg: 39h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp3[15:8]. Higher bits of medium temperature threshold.

HighTemp3Lo - RW – 8 bits - [PM2_Reg: 3Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp3[7:0]. Lower bits of high temperature threshold.

HighTemp3Hi - RW – 8 bits - [PM2_Reg: 3Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp3[15:8]. Higher bits of high temperature threshold.

LinearRange3 - RW – 8 bits - [PM2_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that FanOut3 can tolerate. FanOut3 will not be affected if temperature varies within this range.

LinearHoldCount3 - RW – 8 bits - [PM2_Reg: 3Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan Cycle to be waited before duty cycle can be changed.

Fan4InputControl - RW – 8 bits - [PM2_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
FanInputControl	2:0	000	000: FanOut4 is enabled and temperature input is from Internal diode. 001: FanOut4 is enabled and temperature input is from Temp0. 010: FanOut4 is enabled and temperature input is from Temp1. 011: FanOut4 is enabled and temperature input is from Temp2. 100: FanOut4 is enabled and temperature input is from Temp3. 101: FanOut4 is disabled. 110: FanOut4 is enabled and temperature input is 0. 111: FanOut4 is disabled.

Notes:

When the fan control in not in AutoMode, the active fan duty cycle is set by LowDuty register.

When the fan is set to be controlled by the Temp* input and set to AutoMode, the active duty cycle is controlled by the hardware automatically; either in step or linear function.

(a) Step function: If step function is selected, then whenever Temp* reaches the temperature defined by LowTemp but is less than MedTemp, the fan will be running at a duty cycle equal to LowDuty. When the temperature reaches MedTemp but is below HighTemp, the fan will be running at MedDuty. When it reaches above HighTemp, the fan will simply be running 100% duty cycle.

(b) Linear function: If linear mode is selected, the duty cycle is determined by the equations below:

When Actual Temperature < LowTemp,

DutyCycle = 0

When Actual Temperature > LowTemp and Actual Temperature < MedTemp;

DutyCycle = LowDuty

When Actual Temperature > MedTemp and Actual Temperature < HighTemp

DutyCycle = ((Actual Temperature – LowTemp) * (Multiplier[5:0] + 1) >> Multiplier[7:6]) + LowDuty

When Actual Temperature > HighTemp

DutyCycle = max or 100%

In Automode, hysteresis limit (LinearRange) is applied to keep the fan from oscillating erratically.

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Fan4Control - RW – 8 bits - [PM2_Reg: 41h]			
Field Name	**Bits**	**Default**	**Description**
AutoMode	0	0b	Set to 1 to make FanOut4 controlled by the temperature input; controlled by LowDuty4 otherwise.
LinearMode	1	0b	0: Use step function 1: Use linear function
FanPolarity	2	0b	0: FanOut4 drives low 1: FanOut4 drives high
LinearAdjust	7:3	00h	Additional offset to effective duty cycle under linear mode.

Fan4Freq - RW – 8 bits - [PM2_Reg: 42h]			
Field Name	**Bits**	**Default**	**Description**
FanFreq	7:0	00h	FanOut4 frequency is programmed as follows: 00: 28.64KHz 01: 25.78KHz 02: 23.44KHz 03: 21.48KHz 04: 19.83KHz 05: 18.41KHz Any value > 05h and < F7 Freq = 1/(FreqDiv * 2048 * 15ns) F7: 100Hz F8: 87Hz F9: 58Hz FA: 44Hz FB: 35Hz FC: 29Hz FD: 22Hz FE: 14Hz FF: 11Hz Normally 4-wire fan runs at 25KHz and 3-wire fan runs at 100Hz.

LowDuty4 - RW – 8 bits - [PM2_Reg: 43h]			
Field Name	**Bits**	**Default**	**Description**
LowDuty	7:0	00h	FanOut4 Duty number when temperature is more than lowTemp4 and lower than MedTemp4. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop. … FF: Full speed run.

MedDuty4 - RW – 8 bits - [PM2_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
MedDuty	7:0	00h	FanOut4 Duty number when temperature is more than MedTemp4 and lower than HighTemp4. There are 256 time slots in one Fan cycle. Duty number N represents (N+1)th time slot. Fan actively spins in time slot0~ slotN, and stops from slot-N+1 ~ slot-255. 00: Always stop … FF: Full speed run

Multiplier4 - RW – 8 bits - [PM2_Reg: 45h]			
Field Name	**Bits**	**Default**	**Description**
Multiplier	5:0	00h	Factor to calculate duty number when FanOut4 is set to auto/linear mode.
DutySel	7:6	00b	Select part of duty to be fed into fan.

LowTemp4Lo – RW – 8 bits - [PM2_Reg: 46h]			
Field Name	**Bits**	**Default**	**Description**
LowTempLo	7:0	00h	LowTemp4[7:0]. Lower bits of low temperature threshold.

LowTemp4Hi - RW – 8 bits - [PM2_Reg: 47h]			
Field Name	**Bits**	**Default**	**Description**
LowTempHi	7:0	00h	LowTemp4[15:8]. Higher bits of low temperature threshold.

MedTemp4Lo – RW – 8 bits - [PM2_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
MedTempLo	7:0	00h	MedTemp4[7:0]. Lower bits of medium temperature threshold.

MedTemp4Hi - RW – 8 bits - [PM2_Reg: 49h]			
Field Name	**Bits**	**Default**	**Description**
MedTempHi	7:0	00h	MedTemp4[15:8]. Higher bits of medium temperature threshold.

HighTemp4Lo - RW – 8 bits - [PM2_Reg: 4Ah]			
Field Name	**Bits**	**Default**	**Description**
HighTempLo	7:0	00h	HighTemp4[7:0]. Lower bits of high temperature threshold.

HighTemp4Hi - RW – 8 bits - [PM2_Reg: 4Bh]			
Field Name	**Bits**	**Default**	**Description**
HighTempHi	7:0	00h	HighTemp4[15:8]. Higher bits of high temperature threshold.

LinearRange4 - RW – 8 bits - [PM2_Reg: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
LinearRange	7:0	00h	Variable range that FanOut4 can tolerate. FanOut4 will not be affected if temperature varies within this range.

LinearHoldCount4 - RW – 8 bits - [PM2_Reg: 4Dh]			
Field Name	**Bits**	**Default**	**Description**
LinearHoldCount	7:0	00h	Fan Cycle to be waited before duty cycle can be changed.

FanStatus – RW - [PM2_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
Fan0SpeedTooSlow	0	0b	Indicates whether Fan0 runs slower than the value in the Fan0SpeedLimit. Write to 1 to clear.
Fan1SpeedTooSlow	1	0b	Indicates whether Fan1 runs slower than the value in the Fan1SpeedLimit. Write to 1 to clear.
Fan2SpeedTooSlow	2	0b	Indicates whether Fan2 runs slower than the value in the Fan2SpeedLimit.Write to 1 to clear.
Fan3SpeedTooSlow	3	0b	Indicates whether Fan3 runs slower than the value in the Fan3SpeedLimit. Write to 1 to clear.
Fan4SpeedTooSlow	4	0b	Indicates whether Fan4 runs slower than the value in the Fan4SpeedLimit. Write to 1 to clear.
Reserved	7:5	000b	Reserved

FanINTRouteLo - RW – 8 bits - [PM2_Reg: 61h]			
Field Name	**Bits**	**Default**	**Description**
Fan0INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: no SCI/SMI generated
Fan1INTRoute	3:2	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: no SCI/SMI generated
Fan2INTRoute	5:4	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: no SCI/SMI generated
Fan3INTRoute	7:6	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: no SCI/SMI generated

FanINTRouteHi - RW – 8 bits - [PM2_Reg: 62h]			
Field Name	**Bits**	**Default**	**Description**
Fan4INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT13 routing Others: no SCI/SMI generated
Reserved	7:2	000000b	

SampleFreqDiv – RW – 8 bits - [PM2_Reg: 63h]			
Field Name	**Bits**	**Default**	**Description**
SampleFreqDiv	1:0	00b	These bits determine the sampling rate of Fan Speed 00: Base(22.72KHz) 01: Base(22.72KHz)/2 10: Base(22.72KHz)/4 11: Base(22.72KHz)/8
Reserved	7:2	000000b	Reserved

FanDebounceCounterLo - RW – 8 bits - [PM2_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
FanDebounceCounterLo	7:0	00h	Specify low 8 bits of the debounced counter when measuring Fan Speed

FanDebounceCounterHi - RW – 8 bits - [PM2_Reg: 65h]			
Field Name	**Bits**	**Default**	**Description**
FanDebounceCounterHi	7:0	00h	Specify high 8 bits of the debounced counter when measuring Fan Speed

Fan0DetectorControl- RW – 8 bits - [PM2_Reg: 66h]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan0 speed measurement 1: Enable Fan0 speed measurement
UseAverage	1	0b	0: Not to average Fan0 speed 1: Average Fan0 speed
Reserved	3:2	00b	Reserved
ShutDownEnable	4	00b	If set to, the machine can be shutdown if the Fan0 Status remains for more than 4 seconds.
Reserved	7:5		Reserved

Fan0SpeedLimitLo- RW – 8 bits - [PM2_Reg: 67h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan0SpeedLimit to set threshold when Fan0 speed is below it.

Fan0SpeedLimitHi- RW – 8 bits - [PM2_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan0SpeedLimit to set threshold when Fan0 speed is below it.

Fan0SpeedLo- R – 8 bits - [PM2_Reg: 69h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:1	00h	Fan0Speed [7:0]

Fan0SpeedHi- R – 8 bits - [PM2_Reg: 6Ah]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:0	00h	Fan0Speed[15:8]

Fan1DetectorControl- RW – 8 bits - [PM2_Reg: 6Bh]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan1 speed measurement 1: Enable Fan1 speed measurement
UseAverage	1	0b	0: Not to average Fan1 speed 1: Average Fan1 speed
Reserved	3:2	00b	Reserved
ShutDownEnable	4	00b	If set to 1, the machine can be shutdown if the Fan1 Status remains for more than 4 seconds.
Reserved	7:5		Reserved

Fan1SpeedLimitLo- RW – 8 bits - [PM2_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan1SpeedLimit to set threshold when Fan1 speed is below it.

Fan1SpeedLimitHi- RW – 8 bits - [PM2_Reg: 6Dh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan1SpeedLimit to set threshold when Fan1 speed is below it.

Fan1SpeedLo- R – 8 bits - [PM2_Reg: 6Eh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:1	00h	Fan1Speed[7:0]

Fan1SpeedHi- R – 8 bits - [PM2_Reg: 6Fh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:0	00h	Fan1Speed[15:8]

Fan2DetectorControl- RW – 8 bits - [PM2_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan2 speed measurement 1: Enable Fan2 speed measurement
UseAverage	1	0b	0: Not to average Fan2 speed 1: Average Fan2 speed
Reserved	3:2	00b	
ShutDownEnable	4	00b	If set to, the machine can be shutdown if the Fan2 Status remains for more than 4 seconds.
Reserved	7:5		Reserved

Fan2SpeedLimitLo- RW – 8 bits - [PM2_Reg: 71h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan2SpeedLimit to set threshold when Fan2 speed is below it.

Fan2SpeedLimitHi- RW – 8 bits - [PM2_Reg: 72h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan2SpeedLimit to set threshold when Fan2 speed is below it.

Fan2SpeedLo- R – 8 bits - [PM2_Reg: 73h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:1	00h	Fan2Speed[7:0]

Fan2SpeedHi- R – 8 bits - [PM2_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:0	00h	Fan2Speed[15:8]

Fan3DetectorControl- RW – 8 bits - [PM2_Reg: 75h]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan3 speed measurement 1: Enable Fan3 speed measurement
UseAverage	1	0b	0: Not to average Fan3 speed 1: Average Fan3 speed
Reserved	3:2	00b	
ShutDownEnable	4	00b	If set to, the machine can be shutdown if the Fan3 Status remains for more than 4 seconds.
Reserved	7:5		

Fan3SpeedLimitLo- RW – 8 bits - [PM2_Reg: 76h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan3SpeedLimit to set threshold when Fan3 speed is below it.

Fan3SpeedLimitHi- RW – 8 bits - [PM2_Reg: 77h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan3SpeedLimit to set threshold when Fan3 speed is below it.

Fan3SpeedLo- R – 8 bits - [PM2_Reg: 78h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:1	00h	Fan3Speed[7:0]

Fan3SpeedHi- R – 8 bits - [PM2_Reg: 79h]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:0	00h	Fan3Speed[15:8]

Fan4DetectorControl- RW – 8 bits - [PM2_Reg: 7Ah]			
Field Name	**Bits**	**Default**	**Description**
FanDetectorEnable	0	0b	0: Disable Fan4 speed measurement 1: Enable Fan4 speed measurement
UseAverage	1	0b	0: Not to average Fan4 speed 1: Average Fan4 speed
Reserved	3:2	00b	Reserved
ShutDownEnable	4	00b	If set to, the machine can be shutdown if the Fan4 Status remains for more than 4 seconds.
Reserved	7:5		Reserved

Fan4SpeedLimitLo- RW – 8 bits - [PM2_Reg: 7Bh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Lower 8 bits of Fan4SpeedLimit to set threshold when Fan4 speed is below it.

Fan4SpeedLimitHi- RW – 8 bits - [PM2_Reg: 7Ch]			
Field Name	**Bits**	**Default**	**Description**
FanSpeedLimit	7:0	00h	Higher 8 bits of Fan4SpeedLimit to set threshold when Fan4 speed is below it.

Fan4SpeedLo- R – 8 bits - [PM2_Reg: 7Dh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:1	00h	Fan4Speed[7:0]

Fan4SpeedHi- R – 8 bits - [PM2_Reg: 7Eh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed	7:0	00h	Fan4Speed[15:8]

TempStatus – RW - [PM2_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
IntTempStatus	0	0b	Indicate whether internal Temp is out of the limit. Write to 1 to clear.
Temp0Status	1	0b	Indicate whether Temp0 is out of the limit. Write to 1 to clear.
Temp1Status	2	0b	Indicate whether Temp1 is out of the limit. Write to 1 to clear.
Temp2Status	3	0b	Indicate whether Temp2 is out of the limit. Write to 1 to clear.
Temp3Status	4	0b	Indicate whether Temp3 is out of the limit. Write to 1 to clear.
Reserved	7:5	000b	Reserved

TempControl0- RW – 8 bits - [PM2_Reg: 91h]			
Field Name	**Bits**	**Default**	**Description**
IntTempControl	1:0	00b	Values other than 00 indicate that IntTemp sensor is enabled. 00: Disable 01: Set IntTempStatus to 1 if IntTemp is higher than IntTempLimit. 10: Set IntTempStatus to 1 if IntTemp is lower than IntTempLimit. 11: Set IntTempStatus to 1 if IntTempHi is higher than IntTempLimitLo or lower than IntTempLimitHi.
Temp0Control	3:2	00b	Values other than 00 indicate that Temp0 sensor is enabled. 00: Disable 01: Set Temp0Status to 1 if Temp0 is higher than Temp0Limit 10: Set Temp0Status to 1 if Temp0 is lower than Temp0Limit. 11: Set Temp0Status to 1 if Temp0Hi is higher than Temp0LimitLo or lower than Temp0LimitHi.
Temp1Control	5:4	00b	Values other than 00 indicate that Temp1 sensor is enabled. 00: Disable 01: Set Temp1Status to 1 if Temp1 is higher than Temp1Limit 10: Set Temp1Status to 1 if Temp1 is lower than Temp1Limit. 11: Set Temp1Status to 1 if Temp1Hi is higher than Temp1LimitLo or lower than Temp1LimitHi.
Temp2Control	7:6	00b	Values other than 00 indicate that Temp2 sensor is enabled. 00: Disable 01: Set Temp2Status to 1 if Temp2 is higher than Temp2Limit 10: Set Temp2Status to 1 if Temp2 is lower than Temp2Limit. 11: Set Temp2Status to 1 if Temp2Hi is higher than Temp2LimitLo or lower than Temp2LimitHi.

TempControl1- RW – 8 bits - [PM2_Reg: 92h]			
Field Name	**Bits**	**Default**	**Description**
Temp3Control	1:0	00b	Values other than 00 indicate that Temp3 sensor is enabled. 00: Disable 01: Set Temp3Status to 1 if Temp3 is higher than Temp3Limit 10: Set Temp3Status to 1 if Temp3 is lower than Temp3Limit. 11: Set Temp3Status to 1 if Temp3Hi is higher than Temp3LimitLo or lower than Temp3LimitHi.
Reserved	7:2	000000b	Reserved

TempINTRoute0 - RW – 8 bits - [PM2_Reg: 93h]			
Field Name	**Bits**	**Default**	**Description**
IntTempINTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing others: no SCI/SMI generated
Temp0INTRoute	3:2	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing others: no SCI/SMI generated
Temp1INTRoute	5:4	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing others: no SCI/SMI generated
Temp2INTRoute	7:6	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing others: no SCI/SMI generated

TempINTRoute1 - RW – 8 bits - [PM2_Reg: 94h]			
Field Name	**Bits**	**Default**	**Description**
Temp3INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing others: no SCI/SMI generated
Reserved	7:2	000000b	Reserved

IntTempLo- R – 8 bits - [PM2_Reg: 95h]			
Field Name	**Bits**	**Default**	**Description**
IntTempLo	7:0	00h	IntTemp[7:0]

IntTempHi- R – 8 bits - [PM2_Reg: 96h]			
Field Name	**Bits**	**Default**	**Description**
IntTempHi	7:0	00h	IntTemp[15:8]

IntTempLimitLo- RW – 8 bits - [PM2_Reg: 97h]			
Field Name	**Bits**	**Default**	**Description**
IntTempLimitLo	7:0	00h	IntTempLimit[7:0]

IntTempLimitHi- RW – 8 bits - [PM2_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
IntTempLimitHi	7:0	00h	IntTempLimit[15:8]

Temp0Lo- R – 8 bits - [PM2_Reg: 99h]			
Field Name	**Bits**	**Default**	**Description**
Temp0Lo	7:0	00h	Temp0[7:0]

Temp0Hi- R – 8 bits - [PM2_Reg: 9Ah]			
Field Name	**Bits**	**Default**	**Description**
Temp0Hi	7:0	00h	Temp0[15:8]

Temp0LimitLo- RW – 8 bits - [PM2_Reg: 9Bh]			
Field Name	**Bits**	**Default**	**Description**
Temp0LimitLo	7:0	00h	Temp0Limit[7:0]

Temp0LimitHi- RW – 8 bits - [PM2_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
Temp0LimitHi	7:0	00h	Temp0Limit[15:8]

Temp1Lo- R – 8 bits - [PM2_Reg: 9Dh]			
Field Name	**Bits**	**Default**	**Description**
Temp1Lo	7:0	00h	Temp1[7:0]

Temp1Hi- R – 8 bits - [PM2_Reg: 9Eh]			
Field Name	**Bits**	**Default**	**Description**
Temp1Hi	7:0	00h	Temp1[15:8]

Temp1LimitLo- RW – 8 bits - [PM2_Reg: 9Fh]			
Field Name	**Bits**	**Default**	**Description**
Temp1LimitLo	7:0	00h	Temp1Limit[7:0]

Temp1LimitHi- RW – 8 bits - [PM2_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
Temp1LimitHi	7:0	00h	Temp1Limit[15:8]

Temp2Lo- R – 8 bits - [PM2_Reg: A1h]			
Field Name	**Bits**	**Default**	**Description**
Temp2Lo	7:0	00h	Temp2[7:0]

Temp2Hi- R – 8 bits - [PM2_Reg: A2h]			
Field Name	**Bits**	**Default**	**Description**
Temp2Hi	7:0	00h	Temp2[15:8]

Temp2LimitLo- RW – 8 bits - [PM2_Reg: A3h]			
Field Name	**Bits**	**Default**	**Description**
Temp2LimitLo	7:0	00h	Temp2Limit[7:0]

Temp2LimitHi- RW – 8 bits - [PM2_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
Temp2LimitHi	7:0	00h	Temp2Limit[15:8]

Temp3Lo- R – 8 bits - [PM2_Reg: A5h]			
Field Name	**Bits**	**Default**	**Description**
Temp3Lo	7:0	00h	Temp3[7:0]

Temp3Hi- R – 8 bits - [PM2_Reg: A6h]			
Field Name	**Bits**	**Default**	**Description**
Temp3Hi	7:0	00h	Temp3[15:8]

Temp3LimitLo- RW – 8 bits - [PM2_Reg: A7h]			
Field Name	**Bits**	**Default**	**Description**
Temp3LimitLo	7:0	00h	Temp3Limit[7:0]

Temp3LimitHi- RW – 8 bits - [PM2_Reg: A8h]			
Field Name	**Bits**	**Default**	**Description**
Temp3LimitHi	7:0	00h	Temp3Limit[15:8]

VoltageStatus- R – 8 bits - [PM2_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0Status	0	0b	1 means that Vin0 is out of VoltageLimit0
Voltage1Status	1	0b	1 means that Vin1 is out of VoltageLimit1
Voltage2Status	2	0b	1 means that Vin2 is out of VoltageLimit2
Voltage3Status	3	0b	1 means that Vin3 is out of VoltageLimit3
Voltage4Status	4	0b	1 means that Vin4 is out of VoltageLimit4
Voltage5Status	5	0b	1 means that Vin5 is out of VoltageLimit5
Voltage6Status	6	0b	1 means that Vin6 is out of VoltageLimit6
Voltage7Status	7	0b	1 means that Vin7 is out of VoltageLimit7

VoltageControl0- RW – 8 bits - [PM2_Reg: B2h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0Control	1:0	00b	Values other than 00 indicate that Voltage0 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 5Ah and 59h) against Voltage0Limit (combined value from registers 5Ch and 5Bh); set Voltage0Status bit if is greater than Voltage0Limit 10: Monitor current value (combined value from registers 5Ah and 59h) against Voltage0Limit (combined value from registers 5Ch and 5Bh); set Voltage0Status bit if it is lower than Voltage0Limit 11: Monitor Voltage0Hi against the limits. Set Voltage0Status when it is more than Voltage0LimitLo [7:0] or Lower than Voltage0LimitHi [15:8]
Voltage1Control	3:2	00b	Values other than 00 indicate that Voltage1 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 5Eh and 5Dh) against Voltage1Limit (combined value from registers 60h and 5Fh); set Voltage1Status bit if is greater than Voltage1Limit 10: Monitor current value (combined value from registers 5Eh and 5Dh) against Voltage1Limit (combined value from registers 60h and 5Fh); set Voltage1Status bit if it is lower than Voltage1Limit 11: Monitor Voltage1Hi against the limits. Set Voltage1 Status when it is more than Voltage1LimitLo [7:0] or Lower than Voltage1LimitHi [15:8]
Voltage2Control	5:4	00b	Values other than 00 indicate that Voltage2 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 62h and 61h) against Voltage2Limit (combined value from registers 64h and 63h); set Voltage2Status bit if is greater than Voltage2Limit 10: Monitor current value (combined value from registers 62h and 61h) against Voltage2Limit (combined value from registers 64h and 63h); set Voltage2Status bit if it is lower than Voltage2Limit 11: Monitor Voltage2Hi against the limits. Set Voltage2Status when it is more than Voltage2LimitLo [7:0] or Lower than Voltage2LimitHi [15:8]
Voltage3Control	7:6	00b	Values other than 00 indicate that Voltage3 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 66h and 65h) against Voltage3Limit (combined value from registers 68h and 67h); set Voltage3Status bit if is greater than Voltage3Limit 10: Monitor current value (combined value from registers 66h and 65h) against Voltage3Limit (combined value from registers 68h and 67h); set Voltage3Status bit if it is lower than Voltage3Limit 11: Monitor Voltage3Hi against the limits. Set Voltage3Status when it is more than Voltage3LimitLo [7:0] or lower than Voltage3LimitHi [15:8]

VoltageControl1- RW – 8 bits - [PM2_Reg: B3h]			
Field Name	**Bits**	**Default**	**Description**
Voltage4Control	1:0	00b	Values other than 00 indicate that Voltage4 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 6Ah and 69h) against Voltage4Limit (combined value from registers 6Ch and 6Bh); set Voltage4Status bit if is greater than Voltage4Limit 10: Monitor current value (combined value from registers 6Ah and 69h) against Voltage4Limit (combined value from registers 6Ch and 6Bh); set Voltage4Status bit if it is lower than Voltage4Limit 11: Monitor Voltage4Hi against the limits. Set Voltage4Status when it is more than Voltage4LimitLo [7:0] or lower than Voltage4LimitHi [15:8]
Voltage5Control	3:2	00b	Values other than 00 indicate that Voltage5 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 6Eh and 6Dh) against Voltage5Limit (combined value from registers 70h and 6Fh); set Voltage5Status bit if is greater than Voltage5Limit 10: Monitor current value (combined value from registers 6Eh and 6Dh) against Voltage5Limit (combined value from registers 70h and 6Fh); set Voltage5Status bit if it is lower than Voltage5Limit 11: Monitor Voltage5Hi against the limits. Set Voltage5Status when it is more than Voltage5LimitLo [7:0] or lower than Voltage5LimitHi [15:8]
Voltage6Control	5:4	00b	Values other than 00 indicate that Voltage6 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 72h and 71h) against Voltage6Limit (combined value from registers 74h and 73h); set Voltage6Status bit if is greater than Voltage6Limit 10: Monitor current value (combined value from registers 72h and 71h) against Voltage6Limit (combined value from registers 74h and 73h); set Voltage6Status bit if it is lower than Voltage6Limit 11: Monitor Voltage6Hi against the limits. Set Voltage6Status when it is more than Voltage6LimitLo [7:0] or lower than Voltage6LimitHi [15:8]
Voltage7Control	7:6	00b	Values other than 00 indicate that Voltage7 sensor is enabled. 00: Disable 01: Monitor current value (combined value from registers 76h and 75h) against Voltage7Limit (combined value from registers 78h and 77h); set Voltage7Status bit if is greater than Voltage7Limit 10: Monitor current value (combined value from registers 76h and 75h) against Voltage7Limit (combined value from registers 78h and 77h); set Voltage7Status bit if it is lower than Voltage7Limit 11: Monitor Voltage7Hi against the limits. Set Voltage7Status when it is more than Voltage7LimitLo [7:0] or lower than Voltage7LimitHi [15:8]

AnalogINTRoute0 - RW – 8 bits - [PM2_Reg: B5h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage1INTRoute	3:2	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage2INTRoute	5:4	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage3INTRoute	7:6	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated

AnalogINTRoute1 - RW – 8 bits - [PM2_Reg: B6h]			
Field Name	**Bits**	**Default**	**Description**
Voltage4INTRoute	1:0	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage5INTRoute	3:2	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage6INTRoute	5:4	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated
Voltage7INTRoute	7:6	00b	01: SMI 10: SMI or SCI according GEVENT 13 INT routing Others: no SCI/SMI generated

Voltage0Lo- R – 8 bits - [PM2_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0Lo	7:0	00h	Voltage0 [7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage0Hi- R – 8 bits - [PM2_Reg: B9h]			
Field Name	**Bits**	**Default**	**Description**
Voltage0Hi	7:0	00h	Voltage0 [15:8]

Voltage0LimitLo- RW – 8 bits - [PM2_Reg: BAh]			
Field Name	**Bits**	**Default**	**Description**
Voltage0LimitLo	7:0	00h	Voltage0Limit[7:0]

Voltage0LimitHi- RW – 8 bits - [PM2_Reg: BBh]			
Field Name	**Bits**	**Default**	**Description**
Voltage0LimitHi	7:0	00h	Voltage0Limit[15:8]

Voltage1Lo- R – 8 bits - [PM2_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**
Voltage1Lo	7:0	00h	Voltage1 [7:0]

Voltage1Lo- R – 8 bits - [PM2_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage1Hi- R – 8 bits - [PM2_Reg: BDh]			
Field Name	**Bits**	**Default**	**Description**
Voltage1Hi	7:0	00h	Voltage1 [15:8]

Voltage1LimitLo- RW – 8 bits - [PM2_Reg: BEh]			
Field Name	**Bits**	**Default**	**Description**
Voltage1LimitLo	7:0	00h	Voltage1Limit[7:0]

Voltage1LimitHi- RW – 8 bits - [PM2_Reg: BFh]			
Field Name	**Bits**	**Default**	**Description**
VoltageLimit1Hi	7:0	00h	Voltage1Limit[15:8]

Voltage2Lo- R – 8 bits - [PM2_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
Voltage2Lo	7:0	00h	Voltage2[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage2Hi- R – 8 bits - [PM2_Reg: C1h]			
Field Name	**Bits**	**Default**	**Description**
Voltage2Hi	7:0	00h	Voltage2[15:8]

Voltage2LimitLo- RW – 8 bits - [PM2_Reg: C2]			
Field Name	**Bits**	**Default**	**Description**
Voltage2LimitLo	7:0	00h	Voltage2Limit[7:0]

Voltage2LimitHi- RW – 8 bits - [PM2_Reg: C3h]			
Field Name	**Bits**	**Default**	**Description**
Voltage2LimitHi	7:0	00h	Voltage2Limit[15:8]

Voltage3Lo- R – 8 bits - [PM2_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Voltage3Lo	7:0	00h	Voltage3[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage3Hi- R – 8 bits - [PM2_Reg: C5h]			
Field Name	**Bits**	**Default**	**Description**
Voltage3Hi	7:0	00h	Voltage3[15:8]

Voltage3LimitLo- RW – 8 bits - [PM2_Reg: C6]			
Field Name	**Bits**	**Default**	**Description**
Voltage3LimitLo	7:0	00h	Voltage3Limit[7:0]

Voltage3LimitHi- RW – 8 bits - [PM2_Reg: C7h]			
Field Name	**Bits**	**Default**	**Description**
Voltage3LimitHi	7:0	00h	Voltage3Limit[15:8]

Voltage4Lo- R – 8 bits - [PM2_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
Voltage4Lo	7:0	00h	Voltage4[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage4Hi- R – 8 bits - [PM2_Reg: C9h]			
Field Name	**Bits**	**Default**	**Description**
Voltage4Hi	7:0	00h	Voltage4[15:8]

Voltage4LimitLo- RW – 8 bits - [PM2_Reg: CA]			
Field Name	**Bits**	**Default**	**Description**
Voltage4LimitLo	7:0	00h	Voltage4Limit[7:0]

Voltage4LimitHi- RW – 8 bits - [PM2_Reg: CBh]			
Field Name	**Bits**	**Default**	**Description**
Voltage4LimitHi	7:0	00h	Voltage4Limit[15:8]

Voltage5Lo- R – 8 bits - [PM2_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
Voltage5Lo	7:0	00h	Voltage5[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage5Hi- R – 8 bits - [PM2_Reg: CDh]			
Field Name	**Bits**	**Default**	**Description**
Voltage5Hi	7:0	00h	Voltage5[15:8]

Voltage5LimitLo- RW – 8 bits - [PM2_Reg: CE]			
Field Name	**Bits**	**Default**	**Description**
Voltage5LimitLo	7:0	00h	Voltage5Limit[7:0]

Voltage5LimitHi- RW – 8 bits - [PM2_Reg: CFh]			
Field Name	**Bits**	**Default**	**Description**
Voltage5LimitHi	7:0	00h	Voltage5Limit[15:8]

Voltage6Lo- R – 8 bits - [PM2_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Voltage6Lo	7:0	00h	Voltage6[7:0]

Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage6Hi- R – 8 bits - [PM2_Reg: D1h]			
Field Name	**Bits**	**Default**	**Description**
Voltage6Hi	7:0	00h	Voltage6[15:8]

Voltage6LimitLo- RW – 8 bits - [PM2_Reg: D2]			
Field Name	**Bits**	**Default**	**Description**
Voltage6LimitLo	7:0	00h	Voltage6Limit[7:0]

Voltage6LimitHi- RW – 8 bits - [PM2_Reg: D3h]			
Field Name	**Bits**	**Default**	**Description**
Voltage6LimitHi	7:0	00h	Voltage6Limit[15:8]

Voltage7Lo- R – 8 bits - [PM2_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
Voltage7Lo	7:0	00h	Voltage7[7:0]

Note: Voltage0Lo and Voltage0Hi returns the read value from VIN0 input.

Voltage7Hi- R – 8 bits - [PM2_Reg: D5h]			
Field Name	**Bits**	**Default**	**Description**
Voltage7Hi	7:0	00h	Voltage7[15:8]

Voltage7LimitLo- RW – 8 bits - [PM2_Reg: D6]			
Field Name	**Bits**	**Default**	**Description**
Voltage7LimitLo	7:0	00h	Voltage7Limit[7:0]

Voltage7LimitHi- RW – 8 bits - [PM2_Reg: D7h]			
Field Name	**Bits**	**Default**	**Description**
Voltage7LimitHi	7:0	00h	Voltage7Limit[15:8]

AlertThermaltripStatus- R – 8 bits - [PM2_Reg: E0h]			
Field Name	**Bits**	**Default**	**Description**
AlertStatus	0	0b	Read only. 0: Current temperature is not above AlertLimit 1: Current temperature is above AlertLimit
ThermalTripStatus	1	0b	Read only. 0: Current temperature is not above ThermalTripLimit 1: Current temperature is above ThermalTripLimit
Reserved	7:2		Reserved

AlertLimitLo- RW – 8 bits - [PM2_Reg: E1h]			
Field Name	**Bits**	**Default**	**Description**
AlertLimit	7:0	00h	AlertLimit[7:0]

AlertLimitHi- RW – 8 bits - [PM2_Reg: E2h]			
Field Name	**Bits**	**Default**	**Description**
AlertLimit	7:0	00h	AlertLimit[15:8]

ThermalTripLimitLo- RW – 8 bits - [PM2_Reg: E3h]			
Field Name	**Bits**	**Default**	**Description**
ThermalTripLimit	7:0	00h	ThermalTripLimit [7:0]

ThermalTripLimitHi- RW – 8 bits - [PM2_Reg: E4h]			
Field Name	**Bits**	**Default**	Description
ThermalTripLimit	7:0	00h	ThermalTripLimit [15:8]

AlertThermaltripControl- RW – 8 bits - [PM2_Reg: E5h]			
Field Name	**Bits**	**Default**	**Description**
AlertControl	1:0	00b	Bit 0: Enable TAlert on the selected Temp input Bit 1: Enable ThermalTrip on the selected Temp input
TempSelAlert	7:5	000b	Select temperature sensor as event source 000: Temp0 001: Temp1 010: Temp2 011: Temp3 100: Temp4 Others: Temp0 This register converts the Temp* pin into either TAlert or ThermalTrip function.

HwmControl- R/W – 8 bits - [PM2_Reg: E6h]			
Field Name	**Bits**	**Default**	**Description**
HostReadSensor	0	0b	Writing to1 forces HWM to do a read.
AutoReadSensor	1	0b	Set to 1 to enable periodical reading of voltage/temperature sensors
FastReadEnable	2	0	Set to1 to keep HWM reading sensors repeatedly.
PDAlways	3	0	0: Power on the HWM only when doing a sensor reading. 1: Power on the HWM all the time.
Reserved	6:4	000	.
ResetSensor	7	0	0: Running state 1: Put the HWM into reset state.

VoltageReadFreq - R/W – 8 bits - [PM2_Reg: E7h]			
Field Name	**Bits**	**Default**	**Description**
VoltSensorReadFreq	1:0	00b	00: 100 Hz 01: 200 Hz 10: 300 Hz 11: 500 Hz
Reserved	6:2	00000b	
VoltReadus	7	0b	1: Voltage read period in µs 0: Voltage read period in ms

TempReadFreq - R/W – 8 bits - [PM2_Reg: E8h]			
Field Name	**Bits**	**Default**	**Description**
TempSensorReadFreq	1:0	00b	00: 100ms 01: 200ms 10: 300ms 11: 500ms
Reserved	7:2	000000b	Reserved

VoltageReadAverage – R/W – 8 bits - [PM2_Reg: E9h]			
Field Name	**Bits**	**Default**	**Description**
Volateg0_Average	0	0b	Set to 1 to enable cumulative averaging of Vin0.
Volateg1_Average	1	0b	Set to 1 to enable cumulative averaging of Vin1.
Volateg2_Average	2	0b	Set to 1 to enable cumulative averaging of Vin2.
Volateg3_Average	3	0b	Set to 1 to enable cumulative averaging of Vin3.
Volateg4_Average	4	0b	Set to 1 to enable cumulative averaging of Vin4.
Volateg5_Average	5	0b	Set to 1 to enable cumulative averaging of Vin5.
Volateg6_Average	6	0b	Set to 1 to enable cumulative averaging of Vin6.
Volateg7_Average	7	0b	Set to 1 to enable cumulative averaging of Vin7.

Hwm_VoltCalib – R – 8 bits - [PM2_Reg: EAh]			
Field Name	**Bits**	**Default**	**Description**
Voltage_calibration	6:0	0000000b	Hwm calibration value
Voltage_calibrationValid	7	0b	1: Voltage_calibration in this register is valid. 0: Voltage_calibration in this register is invalid.

TempReadAverage – R/W – 8 bits - [PM2_Reg: EBh]			
Field Name	**Bits**	**Default**	**Description**
IntTemp_Average	0	1b	Set to 1 to enable cumulative averaging of Internal Temp.
Temp0_Average	1	0b	Set to 1 to enable cumulative averaging of Temp0.
Temp1_Average	2	0b	Set to 1 to enable cumulative averaging of Temp1.
Temp2_Average	3	1b	Set to 1 to enable cumulative averaging of Temp2.
Temp3_Average	4	1b	Set to 1 to enable cumulative averaging of Temp3.
Reserved	7:5	000b	Reserved

HwmStatus – R – 8 bits - [PM2_Reg: ECh]			
Field Name	**Bits**	**Default**	**Description**
SensorIdle	0	0b	0: HWM is idle. 1: HWM is doing the sensor reading.
Reserved	6:1	000000b	Reserved
HostReadSts	7	0b	0: No host read is pending. 1: Host read is pending.

VoltageReadStatus – R – 8 bits - [PM2_Reg: EDh]			
Field Name	**Bits**	**Default**	**Description**
Voltage0ReadStatus	0	0b	0: No Voltage0 reading is pending. 1: Voltage0 reading is pending.
Voltage1ReadStatus	1	0b	0: No Voltage1 reading is pending. 1: Voltage1 reading is pending.
Voltage2ReadStatus	2	0b	0: No Voltage2 reading is pending. 1: Voltage2 reading is pending.
Voltage3ReadStatus	3	0b	0: No Voltage3 reading is pending. 1: Voltage3 reading is pending.
Voltage4ReadStatus	4	0b	0: No Voltage4 reading is pending. 1: Voltage4 reading is pending.
Voltage5ReadStatus	5	0b	0: No Voltage5 reading is pending. 1: Voltage5 reading is pending.
Voltage6ReadStatus	6	0b	0: No Voltage6 reading is pending. 1: Voltage6 reading is pending.
Voltage7ReadStatus	7	0b	0: No Voltage7 reading is pending. 1: Voltage7 reading is pending.

TempReadStatus – R – 8 bits - [PM2_Reg: EEh]			
Field Name	**Bits**	**Default**	**Description**
IntTempReadStatus	0	0b	0: No Internal Temp reading is pending. 1: Internal Temp reading is pending.
Temp0ReadStatus	1	0b	0: No Temp0 reading is pending. 1: Temp0 reading is pending.
Temp1ReadStatus	2	0b	0: No Temp1 reading is pending. 1: Temp1 reading is pending.
Temp2ReadStatus	3	0b	0: No Temp2 reading is pending. 1: Temp2 reading is pending.
Temp3ReadStatus	4	0b	0: No Temp3 reading is pending. 1: Temp3 reading is pending.
Reserved	7:5	000b	Reserved

HwmClkControl – R/W – 8 bits - [PM2_Reg: EFh]			
Field Name	**Bits**	**Default**	**Description**
SensorClkDiv	3:0	0000b	To set the Hwm_Clk (sampling clock rate) frequency. Hwm_Clk = 66.67MHz / (2 * (SensorClkDiv+2)) For example, Hwm_Clk = 16.67MHz when the SensorClkDiv is set to value of 0000 Hwm_Clk = 11.11MHz when the SensorClkDiv is set to value of 0001 The recommended value is 1010b
Reserved	7:4	0000b	Reserved

ADC_PDBTime – R/W – 8 bits - [PM2_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
ADC_PDBTime	4:0	11001b	Control the time between HWM_PDB and ADC_PDB. Its unit is µs. Default is 25 µs.
Reserved	7:5	000b	Reserved

ADC_StartUp – R/W – 8 bits - [PM2_Reg: F1h]			
Field Name	**Bits**	**Default**	**Description**
ADC_StartUp	3:0	1010b	Control the time between ADC_RESET and sensor reading. Its unit is µs. Default is 10 µs.
Reserved	7:4	0000b	Reserved

ADC_Delay – R/W – 8 bits - [PM2_Reg: F2h]			
Field Name	**Bits**	**Default**	**Description**
ADC_StartUp	3:0	0010b	Control the delay time between two back to back reading. Its unit is us. Default is 2 µs.
Reserved	7:4	0000b	Reserved

SAX_CTL_VTime – R/W – 8 bits - [PM2_Reg: F3h]			
Field Name	**Bits**	**Default**	**Description**
SAX_CTL_VTime	3:0	0101b	Control the assertion time of SAX_CTL_V. Default is 5 µs.
Reserved	7:4	0000b	Reserved

SAX_CTL_TTime – R/W – 8 bits - [PM2_Reg: F4h]			
Field Name	**Bits**	**Default**	**Description**
SAX_CTL_TTime	7:0	11001000b	Control the assertion time of SAX_CTL_T. Default is 200 µs.

BGADJ – R/W – 8 bits - [PM2_Reg: F5h]			
Field Name	**Bits**	**Default**	**Description**
BGADJ	5:0	100000b	HWM tuning parameter
Reserved	7:6	00b	Reserved

AFEcfg_Clkdiv – R/W – 8 bits - [PM2_Reg: F6h]			
Field Name	**Bits**	**Default**	**Description**
AFE_cfg	1:0	00b	HWM tuning parameter
Reserved	5:2	0000b	Reserved
Clk_div	7:6	10b	HWM tuning parameter

Hwm_DebugSel – R/W – 8 bits - [PM2_Reg: F7h]			
Field Name	**Bits**	**Default**	**Description**
Hwm_Macro_DebugSel	3:0	0000b	HWM tuning parameter
Reserved	7:4	0000b	Reserved

VoltageSampleSel – R/W – 8 bits - [PM2_Reg: F8h]			
Field Name	**Bits**	**Default**	**Description**
Num_Samples_ForVolt	2:0	000b	Specify number of samples per voltage reading. Default value is 1 sample per reading. 000 : 1 sample (default) 001 : 2 samples 010 : 4 samples 011 : 8 samples 100 : 16 samples 101 : 32 samples 110 : 64 samples
Reserved	7:3	00000b	Reserved

TempSampleSel – R/W – 8 bits - [PM2_Reg: F9h]			
Field Name	**Bits**	**Default**	**Description**
Num_Samples_ForTemp	2:0	100b	Specify number of samples per Temp reading. Default value is 16 samples per reading 000 : 1 sample 001 : 2 samples 010 : 4 samples 011 : 8 samples 100 : 16 samples (default) 101 : 32 samples 110 : 64 samples
Reserved	7:3	00000b	Reserved

HwmVoltage_div0 – R/W – 8 bits - [PM2_Reg: FAh]			
Field Name	**Bits**	**Default**	**Description**
Volt0_div	1:0	00b	Specify voltage0 read range.
Volt1_div	3:2	00b	Specify voltage1 read range.
Volt2_div	5:4	00b	Specify voltage2 read range.
Volt3_div	7:6	00b	Specify voltage3 read range.

HwmVoltage_div1 – R/W – 8 bits - [PM2_Reg: FBh]			
Field Name	**Bits**	**Default**	**Description**
Volt4_div	1:0	00b	Specify voltage4 read range.
Volt5_div	3:2	00b	Specify voltage5 read range.
Volt6_div	5:4	00b	Specify voltage6 read range.
Volt7_div	7:6	00b	Specify voltage7 read range.

Adc_Gain_Adj – R/W – 8 bits - [PM2_Reg: FCh]			
Field Name	**Bits**	**Default**	**Description**
Adc_Gain_Adj	3:0	1000b	HWM tuning parameter.
Reserved	7:4	0000b	Reserved

Adc_cfg – R/W – 8 bits - [PM2_Reg: FDh]			
Field Name	**Bits**	**Default**	**Description**
Adc_cfg	3:0	1000b	HWM tuning parameter
Reserved	7:4	0000b	Reserved

Test_cntl – R/W – 8 bits - [PM2_Reg: FEh]			
Field Name	**Bits**	**Default**	**Description**
Test_cntl	3:0	000b	HWM tuning parameter
Reserved	7:4	0000b	Reserved

HwmMiscContro – R/W – 8 bits - [PM2_Reg: FFh]			
Field Name	**Bits**	**Default**	**Description**
Aport_mode	1:0	00b	HWM tuning parameter
Reserved	2	0b	Reserved
Gpio_A_Cntrl	3	0b	HWM tuning parameter
Offset_Can_En	4	0b	HWM tuning parameter
Cycle_en	5	0b	HWM tuning parameter
Hi_Cur_ratio	6	0b	HWM tuning parameter
Hi_Cur_en	7	0b	HWM tuning parameter

2.3.5 SMI Registers

SMI registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from "AcpiMMioAddr" + 0x200 to "AcpiMMioAddr" + 0x2FF.

The base address "AcpiMMioAddr" is defined in PM_reg x24, with the default base address at "FED8_0000."

Register Name	Configuration Offset
EventStatus	00h
EventEnable	04h
SciTrig	08h
SciLevl	0Ch
SmiSciStatus	10h
SmiSciEn	14h
SwSciEn	18h
SwSciData	1Ch
SciSleepDisable	20h
SciMap0	40h
SciMap1	44h
SciMap2	48h
SciMap3	4Ch
SciMap4	50h
SciMap5	54h
SciMap6	58h
SciMap7	5Ch
SciMap8	60h
SciMap9	64h
SciMap10	68h
SciMap11	6Ch
SciMap12	70h
Reserved	74h
Reserved	78h
Reserved	7Ch
SmiStatus	80h
SmiPointer	94h
SmiShortTimer/SmiLongTimer	96h
GeventTrig	98h
IrqTrig	9Ch
SmiControl0	A0h
SmiControl1	A4h
SmiControl2	A8h
SmiControl3	Ach
SmiControl4	B0h
SmiControl5	B4h
SmiControl6	B8h
SmiControl7	BCh
SmiControl8	C0h
SmiControl9	C4h
IoTrapping0	C8h
IoTrapping1	CAh
IoTrapping2	CCh
IoTrapping3	CEh
MemTrappingAdr0	D0h
MemRdOvrData0	D4h
MemTrappingAdr1	D8h
MemRdOvrData1	DCh
MemTrappingAdr2	E0h
MemRdOvrData2	E4h
MemTrappingAdr3	E8h
MemRdOvrData3	ECh
CfgTrappingAdr0	F0h

Register Name	Configuration Offset
CfgTrappingAdr1	F4h
CfgTrappingAdr2	F8h
CfgTrappingAdr3	FCh

Event_Status -R/W – 8/16/32 bits - [SMI_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
EventStatus	31:0		This is a mirror register of the standard ACPI EVENT_STATUS register. Writing 1 to each bit clears the corresponding status bit. Each Event status is set when the selected event input equals to the corresponding value in SciTrig.

Event_Enable -RW – 32 bits - [SMI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
EventEnable	31:0	32'h0	This is the mirror register of the standard ACPI EVENT_ENABLE register. Each bit controls whether ACP should generate wakeup and SCi interrupt.

SciTrig -RW – 32 bits - [SMI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
SciTrig0	0	1b	The bit controls the way to set Event_Status bit 0 0: Active low 1: Active high
SciTrig1	1	1b	The bit controls the way to set Event_Status bit 1 0: Active low 1: Active high
SciTrig2	2	1b	The bit controls the way to set Event_Status bit 2 0: Active low 1: Active high
SciTrig3	3	1b	The bit controls the way to set Event_Status bit 3 0: Active low 1: Active high
SciTrig4	4	1b	The bit controls the way to set Event_Status bit 4 0: Active low 1: Active high
SciTrig5	5	1b	The bit controls the way to set Event_Status bit 5 0: Active low 1: Active high
SciTrig6	6	1b	The bit controls the way to set Event_Status bit 6 0: Active low 1: Active high
SciTrig7	7	1b	The bit controls the way to set Event_Status bit 7 0: Active low 1: Active high
SciTrig8	8	1b	The bit controls the way to set Event_Status bit 8 0: Active low 1: Active high
SciTrig9	9	1b	The bit controls the way to set Event_Status bit 9 0: Active low 1: Active high
SciTrig10	10	1b	The bit controls the way to set Event_Status bit 10 0: Active low 1: Active high

SciTrig -RW – 32 bits - [SMI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
SciTrig11	11	1b	The bit controls the way to set Event_Status bit 11 0: Falling edge 1: Active high
SciTrig12	12	1b	The bit controls the way to set Event_Status bit 12 0: Active low 1: Active high
SciTrig13	13	1b	The bit controls the way to set Event_Status bit 13 0: Active low 1: Active high
SciTrig14	14	1b	The bit controls the way to set Event_Status bit 14 0: Active low 1: Active high
SciTrig15	15	1b	The bit controls the way to set Event_Status bit 15 0: Active low 1: Active high
SciTrig16	16	1b	The bit controls the way to set Event_Status bit 16 0: Active low 1: Active high
SciTrig17	17	1b	The bit controls the way to set Event_Status bit 17 0: Active low 1: Active high
SciTrig18	18	1b	The bit controls the way to set Event_Status bit 18 0: Active low 1: Active high
SciTrig19	19	1b	The bit controls the way to set Event_Status bit 19 0: Active low 1: Active high
SciTrig20	20	1b	The bit controls the way to set Event_Status bit 20 0: Active low 1: Active high
SciTrig21	21	1b	The bit controls the way to set Event_Status bit 21 0: Active low 1: Active high
SciTrig22	22	1b	The bit controls the way to set Event_Status bit 22 0: Active low 1: Active high
SciTrig23	23	1b	The bit controls the way to set Event_Status bit 23 0: Active low 1: Active high
SciTrig24	24	1b	The bit controls the way to set Event_Status bit 24 0: Active low 1: Active high
SciTrig25	25	1b	The bit controls the way to set Event_Status bit 25 0: Active low 1: Active high
SciTrig26	26	1b	The bit controls the way to set Event_Status bit 26 0: Active low 1: Active high
SciTrig27	27	1b	The bit controls the way to set Event_Status bit 27 0: Active low 1: Active high
SciTrig28	28	1b	The bit controls the way to set Event_Status bit 28 0: Active low 1: Active high
ScTrig29	29	1b	The bit controls the way to set Event_Status bit 29 0: Active low 1: Active high

SciTrig -RW – 32 bits - [SMI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
SciTrig30	30	1b	The bit controls the way to set Event_Status bit 30 0: Active low 1: Active high
SciTrig31	31	1b	The bit controls the way to set Event_Status bit 31 0: Active low 1: Active high

SciLevl -RW –32 bits - [SMI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
SciLevl0	0	0	This register defines the trigger mode for each of the Event_Status: 0: Edge trigger 1: Level trigger
SciLevl1	1	0	0: Edge trigger 1: Level trigger
SciLevl2	2	0	0: Edge trigger 1: Level trigger
SciLevl3	3	0	0: Edge trigger 1: Level trigger
SciLevl4	4	0	0: Edge trigger 1: Level trigger
SciLevl5	5	0	0: Edge trigger 1: Level trigger
SciLevl6	6	0	0: Edge trigger 1: Level trigger
SciLevl7	7	0	0: Edge trigger 1: Level trigger
SciLevl8	8	0	0: Edge trigger 1: Level trigger
SciLevl9	9	0	0: Edge trigger 1: Level trigger
SciLevl10	10	0	0: Edge trigger 1: Level trigger
SciLevl11	11	0	0: Edge trigger 1: Level trigger
SciLevl12	12	0	0: Edge trigger 1: Level trigger
SciLevl13	13	0	0: Edge trigger 1: Level trigger
SciLevl14	14	0	0: Edge trigger 1: Level trigger
SciLevl15	15	0	0: Edge trigger 1: Level trigger
SciLevl16	16	0	0: Edge trigger 1: Level trigger
SciLevl17	17	0	0: Edge trigger 1: Level trigger
SciLevl18	18	0	0: Edge trigger 1: Level trigger
SciLevl19	19	0	0: Edge trigger 1: Level trigger
SciLevl20	20	0	0: Edge trigger 1: Level trigger
SciLevl21	21	0	0: Edge trigger 1: Level trigger
SciLevl22	22	0	0: Edge trigger 1: Level trigger

SciLevl -RW –32 bits - [SMI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
SciLevl23	23	0	0: Edge trigger 1: Level trigger
SciLevl24	24	0	0: Edge trigger 1: Level trigger
SciLevl25	25	0	0: Edge trigger 1: Level trigger
SciLevl26	26	0	0: Edge trigger 1: Level trigger
SciLevl27	27	0	0: Edge trigger 1: Level trigger
SciLevl28	28	0	0: Edge trigger 1: Level trigger
SciLevl29	29	0	0: Edge trigger 1: Level trigger
SciLevl30	30	0	0: Edge trigger 1: Level trigger
SciLevl31	31	0	0: Edge trigger 1: Level trigger

SmiSciStatus - RW – 32 bits - [SMI_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
SmiSciStatus	31:0	32'h0	Each bit indicates the corresponding SmiSci status. The input of each bit is controlled by the corresponding SciTrig bit. Each status bit can be cleared to 0 by writing 1. Note this function can be considered as a superset of Event_Status. When one of this bit is set (and its SmiSciEn is also set), it will trigger a SMI to call the BIOS. After the BIOS has serviced the SMM and clears its status, the internal logic will automatically set the corresponding Event_Status bit and thereby triggering a SCI.

SmiSciEn – RW – 32 bits - [SMI_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
SmiSciEn	31:0	32'h0	Each bit controls if SMI message will be generated when the corresponding SmiSciStatus bit is set to 1. 0: Not to send SMI message when the corresponding SmiSciStatus bit is set 1: Send SMI message when the corresponding SmiSciStatus bit is set

SwSciEn - RW – 32 bits - [SMI_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
SwSciEn	31:0	32'h0	When set, software can write to SwSciData and set the corresponding Event_Status bit (note the setting of this bit will need to match with SciTrig and SciLevl in order to set the status bit). This register is meant as a software mechanism to trigger SCI.

SwSciData - RW – 32 bits - [SMI_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
SwSciData	31:0	32'h0	This is the software data path to set the corresponding Event_Status when SwSciEn is set

SciSleepDisable - RW – 32 bits - [SMI_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
SciSleepDisable	31:0	32'h0	When set, the corresponding Event_Status bit will be masked off whenever the system goes to S3 or higher sleep state. This is meant for ignoring EVENT pins that are powered in the main power domain (instead of aux. power domain).

SciMap0 - RW – 32 bits - [SMI_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_0	4:0	0000b	Mapping of GEVENT0 to one of 32 Event_Status. 0000: map event source 0 to the input of Event_Status bit 0 0001: map event source 0 to the input of Event_Status bit 1 … 1111: map input event0 to the input of Event_Status bit 31
SciMap_1	12:8	0000b	Mapping of GEVENT1 to one of 32 Event_Status. 0000: map event source 1 to the input of Event_Status bit 0 0001: map event source 1 to the input of Event_Status bit 1 … 1111: map event source 1 to the input of Event_Status bit 31
SciMap_2	20:16	0000b	Mapping of GEVENT2 to one of 32 Event_Status. 0000: map event source 2 to the input of Event_Status bit 0 0001: map event source 2 to the input of Event_Status bit 1 … 1111: map event source 2 to the input of Event_Status bit 31
SciMap_3	28:24	0000b	Mapping of GEVENT3 to one of 32 Event_Status. 0000: map event source 3 to the input of Event_Status bit 0 0001: map event source 3 to the input of Event_Status bit 1 … 1111: map event source 3 to the input of Event_Status bit 31

SciMap1 - RW – 32 bits - [SMI_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_4	4:0	0000b	Mapping of GEVENT4 to one of 32 Event_Status. 0000: map event source 4 to the input of Event_Status bit 0 0001: map event source 4 to the input of Event_Status bit 1 … 1111: map event source 4 to the input of Event_Status bit 31
SciMap_5	12:8	0000b	Mapping of GEVENT5 to one of 32 Event_Status. 0000: map event source 5 to the input of Event_Status bit 0 0001: map event source 5 to the input of Event_Status bit 1 … 1111: map event source 5 to the input of Event_Status bit 31
SciMap_6	20:16	0000b	Mapping of GEVENT6 to one of 32 Event_Status. 0000: map event source 6 to the input of Event_Status bit 0 0001: map event source 6 to the input of Event_Status bit 1 … 1111: map event source 6 to the input of Event_Status bit 31
SciMap_7	28:24	0000b	Mapping of GEVENT7 to one of 32 Event_Status. 0000: map event source 7 to the input of Event_Status bit 0 0001: map event source 7 to the input of Event_Status bit 1 … 1111: map event source 7 to the input of Event_Status bit 31

SciMap2 - RW – 32 bits - [SMI_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_8	4:0	0000b	Mapping of GEVENT8 to one of 32 Event_Status. 0000: map event source 8 to the input of Event_Status bit 0 0001: map event source 8 to the input of Event_Status bit 1 … 1111: map event source 8 to the input of Event_Status bit 31
SciMap_9	12:8	0000b	Mapping of GEVENT9 to one of 32 Event_Status. 0000: map event source 9 to the input of Event_Status bit 0 0001: map event source 9 to the input of Event_Status bit 1 … 1111: map event source 9 to the input of Event_Status bit 31
SciMap_10	20:16	0000b	Mapping of GEVENT10 to one of 32 Event_Status. 0000: map event source 10 to the input of Event_Status bit 0 0001: map event source 10 to the input of Event_Status bit 1 … 1111: map event source 10 to the input of Event_Status bit 31
SciMap_11	28:24	0000b	Mapping of GEVENT11 to one of 32 Event_Status. 0000: map event source 11 to the input of Event_Status bit 0 0001: map event source 11 to the input of Event_Status bit 1 … 1111: map event source 11 to the input of Event_Status bit 31

SciMap3 - RW – 32 bits - [SMI_Reg: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
SciMap_12	4:0	0000b	Mapping of GEVENT12 to one of 32 Event_Status. 0000: map event source 12 to the input of Event_Status bit 0 0001: map event source 12 to the input of Event_Status bit 1 … 1111: map event source 12 to the input of Event_Status bit 31
SciMap_13	12:8	0000b	Mapping of GEVENT13 to one of 32 Event_Status. 0000: map event source 13 to the input of Event_Status bit 0 0001: map event source 13 to the input of Event_Status bit 1 … 1111: map event source 13 to the input of Event_Status bit 31
SciMap_14	20:16	0000b	Mapping of GEVENT14 to one of 32 Event_Status. 0000: map event source 14 to the input of Event_Status bit 0 0001: map event source 14 to the input of Event_Status bit 1 … 1111: map event source 14 to the input of Event_Status bit 31
SciMap_15	28:24	0000b	Mapping of GEVENT15 to one of 32 Event_Status. 0000: map event source 15 to the input of Event_Status bit 0 0001: map event source 15 to the input of Event_Status bit 1 … 1111: map event source 15 to the input of Event_Status bit 31

SciMap4 - RW – 32 bits - [SMI_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_16	4:0	0000b	Mapping of GEVENT16 to one of 32 Event_Status. 0000: map event source 16 to the input of Event_Status bit 0 0001: map event source 16 to the input of Event_Status bit 1 … 1111: map event source 16 to the input of Event_Status bit 31

SciMap4 - RW – 32 bits - [SMI_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_17	12:8	0000b	Mapping of GEVENT17 to one of 32 Event_Status. 0000: map event source 17 to the input of Event_Status bit 0 0001: map event source 17 to the input of Event_Status bit 1 … 1111: map event source 17 to the input of Event_Status bit 31
SciMap_18	20:16	0000b	Mapping of GEVENT18 to one of 32 Event_Status. 0000: map event source 18 to the input of Event_Status bit 0 0001: map event source 18 to the input of Event_Status bit 1 … 1111: map event source 18 to the input of Event_Status bit 31
SciMap_19	28:24	0000b	Mapping of GEVENT19 to one of 32 Event_Status. 0000: map event source 19 to the input of Event_Status bit 0 0001: map event source 19 to the input of Event_Status bit 1 … 1111: map event source 19 to the input of Event_Status bit 31

SciMap5 - RW – 32 bits - [SMI_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_20	4:0	0000b	Mapping of GEVENT20 to one of 32 Event_Status. 0000: map event source 20 to the input of Event_Status bit 0 0001: map event source 20 to the input of Event_Status bit 1 … 1111: map event source 20 to the input of Event_Status bit 31
SciMap_21	12:8	0000b	Mapping of GEVENT21 to one of 32 Event_Status. 0000: map event source 21 to the input of Event_Status bit 0 0001: map event source 21 to the input of Event_Status bit 1 … 1111: map event source 21 to the input of Event_Status bit 31
SciMap_22	20:16	0000b	Mapping of GEVENT22 to one of 32 Event_Status. 0000: map event source 22 to the input of Event_Status bit 0 0001: map event source 22 to the input of Event_Status bit 1 … 1111: map event source 22 to the input of Event_Status bit 31
SciMap_23	28:24	0000b	Mapping of GEVENT23 to one of 32 Event_Status. 0000: map event source 23 to the input of Event_Status bit 0 0001: map event source 23 to the input of Event_Status bit 1 … 1111: map event source 23 to the input of Event_Status bit 31

SciMap6 - RW – 32 bits - [SMI_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_24	4:0	0000b	Mapping of USB_PME (device 18) to one of 32 Event_Status. 0000: map event source 24 to the input of Event_Status bit 0 0001: map event source 24 to the input of Event_Status bit 1 … 1111: map event source 24 to the input of Event_Status bit 31
SciMap_25	12:8	0000b	Mapping of USB_PME (device 19) to one of 32 Event_Status. 0000: map event source 25 to the input of Event_Status bit 0 0001: map event source 25 to the input of Event_Status bit 1 … 1111: map event source 25 to the input of Event_Status bit 31
SciMap_26	20:16	0000b	Mapping of USB_PME (device 22) to one of 32 Event_Status. 0000: map event source 26 to the input of Event_Status bit 0 0001: map event source 26 to the input of Event_Status bit 1 … 1111: map event source 26 to the input of Event_Status bit 31
SciMap_27	28:24	0000b	Mapping of USB_PME (device 20) to one of 32 Event_Status. 0000: map event source 27 to the input of Event_Status bit 0 0001: map event source 27 to the input of Event_Status bit 1 … 1111: map event source 27 to the input of Event_Status bit 31

SciMap7 - RW – 32 bits - [SMI_Reg: 5Ch]			
Field Name	**Bits**	**Default**	**Description**
SciMap_28	4:0	0000b	Mapping of GPP_PME (device 21, function 0) to one of 32 Event_Status. 0000: map event source 28 to the input of Event_Status bit 0 0001: map event source 28 to the input of Event_Status bit 1 … 1111: map event source 28 to the input of Event_Status bit 31
SciMap_29	12:8	0000b	Mapping of GPP_PME (device 21, function 1) to one of 32 Event_Status. 0000: map event source 29 to the input of Event_Status bit 0 0001: map event source 29 to the input of Event_Status bit 1 … 1111: map event source 29 to the input of Event_Status bit 31
SciMap_30	20:16	0000b	Mapping of GPP_PME (device 21, function 2) to one of 32 Event_Status. 0000: map event source 30 to the input of Event_Status bit 0 0001: map event source 30 to the input of Event_Status bit 1 … 1111: map event source 30 to the input of Event_Status bit 31

SciMap7 - RW – 32 bits - [SMI_Reg: 5Ch]			
Field Name	**Bits**	**Default**	**Description**
SciMap_31	28:24	0000b	Mapping of GPP_PME (device 21, function 3) to one of 32 Event_Status. 0000: map event source 7 to the input of Event_Status bit 0 0001: map event source 7 to the input of Event_Status bit 1 … 1111: map event source 7 to the input of Event_Status bit 31

SciMap8 - RW – 32 bits - [SMI_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_32	4:0	0000b	Mapping of GPP_HotPlug (device 21, function 0) to one of 32 Event_Status. 0000: map event source 32 to the input of Event_Status bit 0 0001: map event source 32 to the input of Event_Status bit 1 … 1111: map event source 32 to the input of Event_Status bit 31
SciMap_33	12:8	0000b	Mapping of GPP_HotPlug (device 21, function 1) to one of 32 Event_Status. 0000: map event source 33 to the input of Event_Status bit 0 0001: map event source 33 to the input of Event_Status bit 1 … 1111: map event source 33 to the input of Event_Status bit 31
SciMap_34	20:16	0000b	Mapping of GPP_HotPlug (device 21, function 2) to one of 32 Event_Status. 0000: map event source 34 to the input of Event_Status bit 0 0001: map event source 34 to the input of Event_Status bit 1 … 1111: map event source 34 to the input of Event_Status bit 31
SciMap_35	28:24	0000b	Mapping of GPP_HotPlug (device 21, function 3) to one of 32 Event_Status. 0000: map event source 35 to the input of Event_Status bit 0 0001: map event source 35 to the input of Event_Status bit 1 … 1111: map event source 35 to the input of Event_Status bit 31

SciMap9 - RW – 32 bits - [SMI_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_36	4:0	0000b	Mapping of HD_Audio_PME to one of 32 Event_Status. 0000: map event source 36 to the input of Event_Status bit 0 0001: map event source 36 to the input of Event_Status bit 1 … 1111: map event source 36 to the input of Event_Status bit 31
SciMap_37	12:8	0000b	Mapping of SATA0_PME to one of 32 Event_Status. 0000: map event source 37 to the input of Event_Status bit 0 0001: map event source 37 to the input of Event_Status bit 1 … 1111: map event source 37 to the input of Event_Status bit 31

SciMap9 - RW – 32 bits - [SMI_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_38	20:16	0000b	Mapping of SATA1_PME to one of 32 Event_Status. 0000: map event source 38 to the input of Event_Status bit 0 0001: map event source 38 to the input of Event_Status bit 1 … 1111: map event source 38 to the input of Event_Status bit 31
SciMap_39	28:24	0000b	Mapping of GEC_PME to one of 32 Event_Status. 0000: map event source 39 to the input of Event_Status bit 0 0001: map event source 39 to the input of Event_Status bit 1 … 1111: map event source 39 to the input of Event_Status bit 31

SciMap10 - RW – 32 bits - [SMI_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_40	4:0	0000b	Mapping of EC0_PME to one of 32 Event_Status. 0000: map event source 40 to the input of Event_Status bit 0 0001: map event source 40 to the input of Event_Status bit 1 … 1111: map event source 40 to the input of Event_Status bit 31
SciMap_41	12:8	0000b	Mapping of EC1_PME to one of 32 Event_Status. 0000: map event source 41 to the input of Event_Status bit 0 0001: map event source 41 to the input of Event_Status bit 1 … 1111: map event source 41 to the input of Event_Status bit 31
SciMap_42	20:16	0000b	Mapping of CIR_PME to one of 32 Event_Status. 0000: map event source 42 to the input of Event_Status bit 0 0001: map event source 42 to the input of Event_Status bit 1 … 1111: map event source 42 to the input of Event_Status bit 31
SciMap_43	28:24	0000b	Mapping of WAKE# pin to one of 32 Event_Status. 0000: map event source 43 to the input of Event_Status bit 0 0001: map event source 43 to the input of Event_Status bit 1 … 1111: map event source 43 to the input of Event_Status bit 31

SciMap11 - RW – 32 bits - [SMI_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
SciMap_44	4:0	0000b	Mapping of internal FAN/THERMAL event to one of 32 Event_Status. 0000: map event source 44 to the input of Event_Status bit 0 0001: map event source 44 to the input of Event_Status bit 1 … 1111: map event source 44 to the input of Event_Status bit 31
SciMap_45	12:8	0000b	Mapping of ASF Master Interrupt event to one of 32 Event_Status. 0000: map event source 45 to the input of Event_Status bit 0 0001: map event source 45 to the input of Event_Status bit 1 … 1111: map event source 45 to the input of Event_Status bit 31

SciMap11 - RW – 32 bits - [SMI_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
SciMap_46	20:16	0000b	Mapping of ASF slave Interrupt event to one of 32 Event_Status. 0000: map event source 46 to the input of Event_Status bit 0 0001: map event source 46 to the input of Event_Status bit 1 … 1111: map event source 46 to the input of Event_Status bit 31
SciMap_47	28:24	0000b	Mapping of SMBUS0 Interrupt event to one of 32 Event_Status. 0000: map event source 47 to the input of Event_Status bit 0 0001: map event source 47 to the input of Event_Status bit 1 … 1111: map event source 47 to the input of Event_Status bit 31

SciMap12 - RW – 32 bits - [SMI_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
SciMap_48	4:0	0000b	Mapping of TWARN pin to one of 32 Event_Status. 0000: map event source 48 to the input of Event_Status bit 0 0001: map event source 48 to the input of Event_Status bit 1 … 1111: map event source 48 to the input of Event_Status bit 31
SciMap_49	12:8	0000b	Mapping of internal traffic monitor to one of 32 Event_Status. 0000: map event source 49 to the input of Event_Status bit 0 0001: map event source 49 to the input of Event_Status bit 1 … 1111: map event source 49 to the input of Event_Status bit 31
Reserved	28:16	-	

Reserved - RW – 32 bits - [SMI_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved - RW – 32 bits - [SMI_Reg: 78h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved - RW – 32 bits - [SMI_Reg: 7Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

SmiStatus0 - RW – 32 bits - [SMI_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Gevent0Status_event0	0	0b	Status of Gevent0; write 1 to clear it to 0.
Gevent1Status_event1	0	0b	Status of Gevent1; write 1 to clear it to 0.
Gevent2Status_event2	0	0b	Status of Gevent2; write 1 to clear it to 0.
Gevent3Status_event3	0	0b	Status of Gevent3; write 1 to clear it to 0.
Gevent4Status_event4	0	0b	Status of Gevent4; write 1 to clear it to 0.
Gevent5Status_event5	0	0b	Status of Gevent5; write 1 to clear it to 0.
Gevent6Status_event6	0	0b	Status of Gevent6; write 1 to clear it to 0.
Gevent7Status_event7	0	0b	Status of Gevent7; write 1 to clear it to 0.

SmiStatus0 - RW – 32 bits - [SMI_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Gevent8Status_event8	0	0b	Status of Gevent8; write 1 to clear it to 0.
Gevent9Status_event9	0	0b	Status of Gevent9; write 1 to clear it to 0.
Gevent10Status_event10	0	0b	Status of Gevent10; write 1 to clear it to 0.
Gevent11Status_event11	0	0b	Status of Gevent11; write 1 to clear it to 0.
Gevent12Status_event12	0	0b	Status of Gevent12; write 1 to clear it to 0.
Gevent13Status_event13	0	0b	Status of Gevent13; write 1 to clear it to 0.
Gevent14Status_event14	0	0b	Status of Gevent14; write 1 to clear it to 0.
Gevent15Status_event15	0	0b	Status of Gevent15; write 1 to clear it to 0.
Gevent16Status_event16	0	0b	Status of Gevent16; write 1 to clear it to 0.
Gevent17Status_event17	0	0b	Status of Gevent17; write 1 to clear it to 0.
Gevent18Status_event18	0	0b	Status of Gevent18; write 1 to clear it to 0.
Gevent19Status_event19	0	0b	Status of Gevent19; write 1 to clear it to 0.
Gevent20Status_event20	0	0b	Status of Gevent20; write 1 to clear it to 0.
Gevent21Status_event21	0	0b	Status of Gevent21; write 1 to clear it to 0.
Gevent22Status_event22	0	0b	Status of Gevent22; write 1 to clear it to 0.
Gevent23Status_event23	0	0b	Status of Gevent23; write 1 to clear it to 0.
Usbwakup0_event24	24	0b	Status of USB device 18 Pme; write 1 to clear it to 0.
Usbwakup1_event25	25	0b	Status of USB device 19 Pme; write 1 to clear it to 0.
Usbwakup2_event26	26	0b	Status of USB device 22 Pme; write 1 to clear it to 0.
Usbwakup3_event27	27	0b	Status of USB device 20 Pme; write 1 to clear it to 0.
SBGppPme0_event28	28	0b	Status of FCH GPP(dev21, function0) PME; write 1 to clear it to 0.
SBGppPme1_event29	29	0b	Status of FCH GPP(dev21, function1) PME; write 1 to clear it to 0.
SBGppPme2_event30	30	0b	Status of FCH GPP(dev21, function2) PME; write 1 to clear it to 0.
SBGppPme3_event31	31	0b	Status of FCH GPP(dev21, function3) PME; write 1 to clear it to 0.

SmiStatus1 - RW – 32 bits - [SMI_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
SBGppHp0_event32	0	0b	Status of FCH GPP(dev21, function0) HP; write 1 to clear it to 0.
SBGppHp1_event33	1	0b	Status of FCH GPP(dev21, function1) HP; write 1 to clear it to 0.
SBGppHp2_event34	2	0b	Status of FCH GPP(dev21, function2) HP; write 1 to clear it to 0.
SBGppHp3_event35	3	0b	Status of FCH GPP(dev21, function3) HP; write 1 to clear it to 0.
AzaliaPme_event36	4	0b	Status of FCH HD Audio PME; write 1 to clear it to 0.
SataGevent0_event37	5	0b	Status of FCH SataGevent0; write 1 to clear it to 0.
SataGevent1_event38	6	0b	Status of FCH SataGevent1; write 1 to clear it to 0.
GecPme_event39	7	0b	Status of FCH Gec Pme; write 1 to clear it to 0.
ECGevent0_event40	8	0b	Status of FCH ECGevent0; write 1 to clear it to 0.
ECGevent1_event41	9	0b	Status of FCH ECGevent1; write 1 to clear it to 0.
CIRPme_event42	10	0b	Status of FCH CIR Pme; write 1 to clear it to 0.
WakePinGevent_event43	11	0b	Status of FCH Wake#; write 1 to clear it to 0.
FanThermalGevent_event 44	12	0b	Status of FCH FanThermal; write 1 to clear it to 0.
ASFMasterIntr_event45	13	0b	Status of FCH ASF Master interrupt; write 1 to clear it to 0.
ASFSlaveIntr_event46	14	0b	Status of FCH ASF Slave interrupt; write 1 to clear it to 0.
SMBUS0_event47	15	0b	Status of FCH SMBUS0 Master interrupt; write 1 to clear it to 0.
TWARN_event48	16	0b	Status of FCH TWARN; write 1 to clear it to 0.
TrafficMonitorIntr_event49	17	0b	Status of FCH Traffic Monitor Interrupt; write 1 to clear it to 0.
iLLB_event50	18	0b	Status of iLLB# assertion; write 1 to clear it to 0.
PwrButton_event51	19	0b	Status of PwrButton (rising edge) writing 1 to clear it to 0.

SmiStatus1 - RW – 32 bits - [SMI_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
ProcHot_event52	20	0b	Status of ProcHot event; write 1 to clear it to 0.
NBHwAssertion_event53	21	0b	Status of NB Hw assertion; write 1 to clear it to 0.

SmiStatus2 - RW – 32 bits - [SMI_Reg:88h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved
Slp_Type_event65	1	0b	Status of writing Slp_Typ; write 1 to clear it to 0.
GecRomSmi_event66	2	0b	Status of Gec Shadow ram Smi request; write 1 to clear it to 0
iSata_Ahci_smi_event67	3	0b	Status of Sata AHCI Smi request; write 1 to clear it to 0
NBGppPme_event68	4	0b	Status of NB Gpp Pme message; write 1 to clear it to 0
NBGppHp_event69	5	0b	Status of NB HP message; write 1 to clear it to 0
Rtc_Irq_event70	6	0b	Status of Rtc IRQ; write 1 to clear it to 0
ACPITimer_event71	7	0b	Status of Acpi Pm timer rollover interrupt; write 1 to clear it to 0
GBL_RLS_event72	8	0b	Status of GBL event; write 1 to clear it to 0
BIOS_RLS_event73	9	0b	Status of BIOS_RLS; write 1 to clear it to 0
PWRBTN_event74	10	0b	Status of Power Button being pressed; write 1 to clear it to 0
SmiCmdPort_event75	11	0b	Status of Writing Smi Command Port; write 1 to clear it to 0
UsbSmi_event76	12	0b	Status of Usb Smi request; write 1 to clear it to 0
SerialIrqSMi_event77	13	0b	Status of Smi request from Serial IRQ; write 1 to clear it to 0
SMBUS0Intr_event78	14	0b	Status of SMBUS0 interrupt request; write 1 to clear it to 0
IMCSmi0_event79	15	0b	Status of IMC Smi request ; write 1 to clear it to 0
IMCSmi1_event80	16	0b	Status of IMC2 Smi request; write 1 to clear it to 0
IntruderAlertSts_event81	17	0b	Status of Intruder Alert event; write 1 to clear it to 0
VBATLow_event82	18	0b	Status of VBAT low; write 1 to clear it to 0
ProtHot_event83	19	0b	Status of ProtHot event; write 1 to clear it to 0
PciSerr_event84	20	0b	Status of Serr assertion on Pci bus; write 1 to clear it to 0
SBGppSerr0_event85	21	0b	SERR error from FCH GPP device 21, function 0; write 1 to clear it to 0
SBGppSerr1_event86	22	0b	SERR error from FCH GPP device 21, function 1; write 1 to clear it to 0
SBGppSerr2_event87	23	0b	SERR error from FCH GPP device 21, function 2; write 1 to clear it to 0
SBGppSerr3_event88	24	0b	SERR error from FCH GPP device 21, function 3; write 1 to clear it to 0
ThermalTrip_event89	25	0b	Status of ThermalTrip event; write 1 to clear it to 0
Emulate64_event90	26	0b	Status of Emulation Io Port 60/64h; write 1 to clear it to 0
Usb_FLR_event91	27	0b	Status of Usb FLR event; write 1 to clear it to 0
Sata_FLR_event92	28	0b	Status of Sata FLR event; write 1 to clear it to 0
Az_FLR_event93	29	0b	Status of Azalia FLR event; write 1 to clear it to 0
Gec_FLR_event94	30	0b	Status of Gec FLR event; write 1 to clear it to 0
CmosEraseSts_event95	31	0b	Status of Cmos Erase event; write 1 to clear it to 0

SmiStatus3- RW – 32 bits - [SMI_Reg: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
IRQ0Trapping_event96	0	0b	Status of IRQ0 request; write 1 to clear it to 0
IRQ1Trapping_event97	1	0b	Status of IRQ1 request; write 1 to clear it to 0
IRQ2Trapping_event98	2	0b	Status of IRQ2 request; write 1 to clear it to 0
IRQ3Trapping_event99	3	0b	Status of IRQ3 request; write 1 to clear it to 0
IRQ4Trapping_event100	4	0b	Status of IRQ4 request; write 1 to clear it to 0
IRQ5Trapping_event101	5	0b	Status of IRQ5 request; write 1 to clear it to 0
IRQ6Trapping_event102	6	0b	Status of IRQ6 request; write 1 to clear it to 0
IRQ7Trapping_event103	7	0b	Status of IRQ7 request; write 1 to clear it to 0

SmiStatus3- RW – 32 bits - [SMI_Reg: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
IRQ8Trapping_event104	8	0b	Status of IRQ8 request; write 1 to clear it to 0
IRQ9Trapping_event105	9	0b	Status of IRQ9 request; write 1 to clear it to 0
IRQ10Trapping_event106	10	0b	Status of IRQ10 request; write 1 to clear it to 0
IRQ11Trapping_event107	11	0b	Status of IRQ11 request; write 1 to clear it to 0
IRQ12Trapping_event108	12	0b	Status of IRQ12 request; write 1 to clear it to 0
IRQ13Trapping_event109	13	0b	Status of IRQ13 request; write 1 to clear it to 0
IRQ14Trapping_event110	14	0b	Status of IRQ14 request; write 1 to clear it to 0
IRQ15Trapping_event111	15	0b	Status of IRQ15 request; write 1 to clear it to 0
IRQ16Trapping_event112	16	0b	Status of IRQ16 request; write 1 to clear it to 0
IRQ17Trapping_event113	17	0b	Status of IRQ17 request; write 1 to clear it to 0
IRQ18Trapping_event114	18	0b	Status of IRQ18 request; write 1 to clear it to 0
IRQ19Trapping_event115	19	0b	Status of IRQ19 request; write 1 to clear it to 0
IRQ20Trapping_event116	20	0b	Status of IRQ20 request; write 1 to clear it to 0
IRQ21Trapping_event117	21	0b	Status of IRQ21 request; write 1 to clear it to 0
IRQ22Trapping_event118	22	0b	Status of IRQ22 request; write 1 to clear it to 0
IRQ23Trapping_event119	23	0b	Status of IRQ23 request; write 1 to clear it to 0
VIn0Sts_event120	24	0b	Status of Vin0 event; write 1 to clear it to 0
VIn1Sts_event121	25	0b	Status of Vin1 event; write 1 to clear it to 0
VIn2Sts_event122	26	0b	Status of Vin2 event; write 1 to clear it to 0
VIn3Sts_event123	27	0b	Status of Vin3 event; write 1 to clear it to 0
VIn4Sts_event124	28	0b	Status of Vin4 event; write 1 to clear it to 0
VIn5Sts_event125	29	0b	Status of Vin5 event; write 1 to clear it to 0
VIn6Sts_event126	30	0b	Status of Vin6 event; write 1 to clear it to 0
VIn7Sts_event127	31	0b	Status of Vin7 event; write 1 to clear it to 0

SmiStatus4- RW – 32 bits - [SMI_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
Temp0Sts_event128	0	0b	Status of Temp0 event; write 1 to clear it to 0
Temp1Sts_event129	1	0b	Status of Temp1 event; write 1 to clear it to 0
Temp2Sts_event130	2	0b	Status of Temp2 event; write 1 to clear it to 0
Temp3Sts_event131	3	0b	Status of Temp3 event; write 1 to clear it to 0
Temp4Sts_event132	4	0b	Status of Temp4 event; write 1 to clear it to 0
FanIn0Sts_event133	5	0b	Status of FanIn0 event; write 1 to clear it to 0
FanIn1Sts_event134	6	0b	Status of FanIn1 event; write 1 to clear it to 0
FanIn2Sts_event135	7	0b	Status of FanIn2 event; write 1 to clear it to 0
FanIn3Sts_event136	8	0b	Status of FanIn3 event; write 1 to clear it to 0
FanIn4Sts_event137	9	0b	Status of FanIn4 event; write 1 to clear it to 0
Fake0Sts_event138	10	0b	Status of Fake0; write 1 to clear it to 0
Fake1Sts_event139	11	0b	Status of Fake1; write 1 to clear it to 0
Fake2Sts_event140	12	0b	Status of Fake2; write 1 to clear it to 0
CStateMsg_event141	13	0b	Status of C State Change message request; write 1 to clear it to 0
ShortTimer_event142	14	0b	Status of Short Timer Smi request; write 1 to clear it to 0
LongTimer_event143	15	0b	Status of Long Timer Smi request; write 1 to clear it to 0
AbSmiTrap_event144	16	0b	Status of AB Smi trapping request; write 1 to clear it to 0
PStateChange_event145	17	0b	Status of P State request; write 1 to clear it to 0
PStateChange_event146	18	0b	Status of P State request; write 1 to clear it to 0
PStateChange_event147	19	0b	Status of P State request; write 1 to clear it to 0
IoTrapping0_event148	20	0b	Status of Io Trapping0 Smi request; write 1 to clear it to 0
IoTrapping1_event149	21	0b	Status of Io Trapping1 Smi request; write 1 to clear it to 0
IoTrapping2_event150	22	0b	Status of Io Trapping2 Smi request; write 1 to clear it to 0
IoTrapping3_event151	23	0b	Status of Io Trapping3 Smi request; write 1 to clear it to 0
MemTrapping0_event152	24	0b	Status of memory Trapping0 Smi request; write 1 to clear it to 0

SmiStatus4- RW – 32 bits - [SMI_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
MemTrapping1_event153	25	0b	Status of memory Trapping1 Smi request; write 1 to clear it to 0
MemTrapping2_event154	26	0b	Status of memory Trapping2 Smi request; write 1 to clear it to 0
MemTrapping3_event155	27	0b	Status of memory Trapping3 Smi request; write 1 to clear it to 0
CfgTrapping0_event156	28	0b	Status of Pci configuration cycle Trapping0 Smi request ; write 1 to clear it to 0
CfgTrapping1_event157	29	0b	Status of Pci configuration cycle Trapping1 Smi request; write 1 to clear it to 0
CfgTrapping2_event158	30	0b	Status of Pci configuration cycle Trapping2 Smi request; write 1 to clear it to 0
CfgTrapping3_event159	31	0b	Status of Pci configuration cycle Trapping3 Smi request; write 1 to clear it to 0

SmiPointer - R – 8 bits - [SMI_Reg: 94h]			
Field Name	**Bits**	**Default**	**Description**
SmiSciSource	0	0b	Indicates whether the SMI source is from SMISCI.
SmiStatusSource0	1	0b	Indicates whether the SMI source is from SmiStatus0[31:0] if the corresponding SMI enable is selected.
SmiStatusSource1	2	0b	Indicates whether the SMI source is from SmiStatus1[31:0] if the corresponding SMI enable is selected.
SmiStatusSource2	3	0b	Indicates whether the SMI source is from SmiStatus2[31:0] if the corresponding SMI enable is selected.
SmiStatusSource3	4	0b	Indicate whether the SMI source is from SmiStatus3[31:0] if the corresponding SMI enable is selected.
SmiStatusSource4	5	0b	Indicate whether the SMI source is from SmiStatus4[31:0] if the corresponding SMI enable is selected.
Reserved	15:6	0	Reserved.

Note: This register is meant as a faster mechanism to locate the SMI source. BIOS can examine this register to find out the SMI source instead of reading SmiStatus0 through SmiStatus4 individually

There are two SMI timers, short timer runs at 1us unit time and long timer is 1ms unit time. SMI_Reg:96h is actually made up of two sets of registers depending on the setting of PMIO_98[29]. When PMIO_98[29]=0, it is selecting the control registers for the short timer. When PMIO_98[29]=1, it is selecting the control registers for the long timer

SmiShortTimer – R/W – 16 bits - [SMI_Reg: 96h]			
Field Name	**Bits**	**Default**	**Description**
SmiTimerCount	14:0	0000h	Actual timer duration = TimerTime + 1 unit (us)
TimerEn	15	0b	Enable the SMI short Timer or long timer, which is selected by SmiTimerEn (PMIO_98[29]). 0 = Disable 1 = Enable

***Note:** This register 96h can be either “SmiShortTimer” or “SmiLongTimer,” depending on the select bit “SmiTimerSel” in SMI_Reg 98[29]. The default setting (SmiTimerSel=0) selects this register as “SmiShortTimer”; software needs to set the “SmiTimerSel=1” to select this register as “SmiLongTimer”.

SmiLongTimer – R/W – 16 bits - [SMI_Reg: 96h]			
Field Name	**Bits**	**Default**	**Description**
SmiTimerCount	14:0	0000h	Actual timer duration = TimerTime + 1 unit (ms)

SmiLongTimer – R/W – 16 bits - [SMI_Reg: 96h]			
Field Name	**Bits**	**Default**	**Description**
TimerEn	15	0b	Enable the SMI short Timer or long timer, which is selected by SmiTimerEn (PMIO_98[29]). 0 = Disable 1 = Enable

***Note:** This register 96h can be either "SmiShortTimer" or "SmiLongTimer," depending on the select bit "SmiTimerSel" in SMI_Reg 98[29]. The default setting (SmiTimerSel=0) selects this register as "SmiShortTimer"; software needs to set the "SmiTimerSel=1" to select this register as "SmiLongTimer".

There are 24 trigger bits for 24 Gevent.

SmiTrig0 - RW – 8/16/32 bits - [SMI_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
SmiTrig0	0	1b	This defines the trigger mode for SmiStatus0[23:0]. Note these are different from SciTrig 0: Active low 1: Active high
SmiTrig1	1	1b	0: Active low 1: Active high
SmiTrig2	2	1b	0: Active low 1: Active high
SmiTrig3	3	1b	0: Active low 1: Active high
SmiTrig4	4	1b	0: Active low 1: Active high
SmiTrig5	5	1b	0: Active low 1: Active high
SmiTrig6	6	1b	0: Active low 1: Active high
SmiTrig7	7	1b	0: Active low 1: Active high
SmiTrig8	8	1b	0: Active low 1: Active high
SmiTrig9	9	1b	0: Active low 1: Active high
SmiTrig10	10	1b	0: Active low 1: Active high
SmiTrig11	11	1b	0: Active low 1: Active high
SmiTrig12	12	1b	0: Active low 1: Active high
SmiTrig13	13	1b	0: Active low 1: Active high
SmiTrig14	14	1b	1: Active high 0: Active low
SmiTrig15	15	1b	0: Active low 1: Active high
SmiTrig16	16	1b	0: Active low 1: Active high
SmiTrig17	17	1b	0: Active low 1: Active high
SmiTrig18	18	1b	0: Active low 1: Active high
SmiTrig19	19	1b	0: Active low 1: Active high
SmiTrig20	20	1b	0: Active low 1: Active high

SmiTrig0 - RW – 8/16/32 bits - [SMI_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
SmiTrig21	21	1b	0: Active low 1: Active high
SmiTrig22	22	1b	0: Active low 1: Active high
SmiTrig23	23	1b	0: Active low 1: Active high
TrappingIRQonPIC	24	1b	SMI will be generated when 0: Trapping Irq0 ~ 15 of IoApIC 1: Trapping Irq0 ~ 15 of PIC
FakeSts0	25	1b	Program the value to emulate an SMI input event.
FakeSts1	26	1b	Program the value to emulate an SMI input event.
FakeSts2	27	1b	Program the value to emulate an SMI input event.
Eos	28	1b	Set to1 to allow SMI to be sent out to CPU; otherwise SMI is blocked.
SmiTimerSel	29	0b	0: Selects the SMI_Reg 96h to be SmiShortTimer register. 1: Selects the SMI_Reg 96h to be SmiLongTimer register.
SmiEnB	31	1b	Enable SMI function. 0: Enable 1: Disable

There are 24 trigger bits for 24 Irq

SmiTrig1 - RW – 8/16/32 bits - [SMI_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
SmiIrq0Trig	0	0b	0: Active low 1: Active high
SmiIrq1Trig	1	0b	0: Active low 1: Active high
SmiIrq2Trig	2	0b	0: Active low 1: Active high
SmiIrq3Trig	3	0b	0: Active low 1: Active high
SmiIrq4Trig	4	0b	0: Active low 1: Active high
SmiIrq5Trig	5	0b	0: Active low 1: Active high
SmiIrq6Trig	6	0b	0: Active low 1: Active high
SmiIrq7Trig	7	0b	0: Active low 1: Active high
SmiIrq8Trig	8	0b	0: Active low 1: Active high
SmiIrq9Trig	9	0b	0: Active low 1: Active high
SmiIrq10Trig	10	0b	0: Active low 1: Active high
SmiIrq11Trig	11	0b	0: Active low 1: Active high
SmiIrq12Trig	12	0b	0: Active low 1: Active high
SmiIrq13Trig	13	0b	0: Active low 1: Active high
SmiIrq14Trig	14	0b	0: Active low 1: Active high
SmiIrq15Trig	15	0b	0: Active low 1: Active high

SmiTrig1 - RW – 8/16/32 bits - [SMI_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
SmiIrq16Trig	16	0b	0: Active low 1: Active high
SmiIrq17Trig	17	0b	0: Active low 1: Active high
SmiIrq18Trig	18	0b	0: Active low 1: Active high
SmiIrq19Trig	19	0b	0: Active low 1: Active high
SmiIrq20Trig	20	0b	0: Active low 1: Active high
SmiIrq21Trig	21	0b	0: Active low 1: Active high
SmiIrq22Trig	22	0b	0: Active low 1: Active high
SmiIrq23Trig	23	0b	0: Active low 1: Active high

SMI_Reg 0xA0 through 0xA7 specify the control mechanism for SMI source 0 through 159 (please see SMI_Reg 0x80 through 0x90). Each control takes up 2 bits to control the behavior for each source.

SmiControl0 - RW – 8/16/32 bits - [SMI_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_0	1:0	00b	Control for GEVENT0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_1	3:2	00b	Control for GEVENT1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_2	5:4	00b	Control for GEVENT2 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_3	7:6	00b	Control for GEVENT3 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_4	9:8	00b	Control for GEVENT4 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_5	11:0	00b	Control for GEVENT5 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl0 - RW – 8/16/32 bits - [SMI_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_6	13:12	00b	Control for GEVENT6 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_7	15:14	00b	Control for GEVENT7 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_8	17:16	00b	Control for GEVENT8 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_9	19:18	00b	Control for GEVENT9 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_10	21:20	00b	Control for GEVENT10 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_11	23:22	00b	Control for GEVENT11 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_12	25:24	00b	Control for GEVENT12 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_13	27:26	00b	Control for GEVENT13 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_14	29:28	00b	Control for GEVENT14 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_15	31:30	00b	Control for GEVENT15 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl1 - RW – 8/16/32 bits - [SMI_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_16	1:0	00b	Control for GEVENT16 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl1 - RW – 8/16/32 bits - [SMI_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_17	3:2	00b	Control for GEVENT17 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_18	5:4	00b	Control for GEVENT18 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_19	7:6	00b	Control for GEVENT19 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_20	9:8	00b	Control for GEVENT20 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_21	11:0	00b	Control for GEVENT21 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_22	13:12	00b	Control for GEVENT22 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_23	15:14	00b	Control for GEVENT23 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_24	17:16	00b	Control for USB_PME (device 18) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_25	19:18	00b	Control for USB_PME (device 19) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_26	21:20	00b	Control for USB_PME (device 22) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_27	23:22	00b	Control for USB_PME (device 20) 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl1 - RW – 8/16/32 bits - [SMI_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_28	25:24	00b	Control for GPP_PME (device 21, function0) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_29	27:26	00b	Control for GPP_PME (device 21, function1) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_30	29:28	00b	Control for GPP_PME (device 21, function2) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_31	31:30	00b	Control for GPP_PME (device 21, function3) 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl2 - RW – 8/16/32 bits - [SMI_Reg: A8h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_32	1:0	00b	Control for GPP_HotPlug (device 21, function 0) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_33	3:2	00b	Control for GPP_HotPlug (device 21, function 1) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_34	5:4	00b	Control for GPP_HotPlug (device 21, function 2) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_35	7:6	00b	Control for GPP_HotPlug (device 21, function 3) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_36	9:8	00b	Control for PME frpm HD Audio 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_37	11:0	00b	Control for Sata Gevent0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_38	13:12	00b	Control for Sata Gevent1 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl2 - RW – 8/16/32 bits - [SMI_Reg: A8h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_39	15:14	00b	Control for Gec Pme 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_40	17:16	00b	Control for IMC Gevent0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_41	19:18	00b	Control for IMC Gevent1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_42	21:20	00b	Control for CIR PME 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_43	23:22	00b	Control for Wak# pin 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_44	25:24	00b	Control for FanThermal Gevent 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_45	27:26	00b	Control for ASF Master interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_46	29:28	00b	Control for ASF Slave interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_47	31:30	00b	Control for SMBUS0 interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl3 - RW – 8/16/32 bits - [SMI_Reg: ACh]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_48	1:0	00b	Control for TWARN# 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl3 - RW – 8/16/32 bits - [SMI_Reg: ACh]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_49	3:2	00b	Control for internal Traffic monitor interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_50	5:4	00b	Control for iLLB# 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_51	7:6	00b	Control for Power button event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_52	9:8	00b	Control for ProcHot event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_53	11:10	00b	Control for NB hw assertion 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl4 - RW – 8/16/32 bits - [SMI_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_65	3:2	00b	Control for writting SLP_TYP to put the system in S state. 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_66	5:4	00b	Control for GEC shodows rom write 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_67	7:6	00b	Control for Sata AHCI event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_68	9:8	00b	Control for NB Gpp PME 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_69	11:10	00b	Control for NB Gpp Hotplug 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_70	13:12	00b	Control for rtc IRQ 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl4 - RW – 8/16/32 bits - [SMI_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_71	15:14	00b	Control for Pm timer rollerover 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_72	17:16	00b	Control for writing GBL_RLS 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_73	19:18	00b	Control for writing BIOS_RLS 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_74	21:20	00b	Control for power botton being pressed 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_75	23:22	00b	Control for writing Smi command port 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_76	25:24	00b	Control for Usb Smi request 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_77	27:26	00b	Control for Smi request form serial Irq 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_78	29:28	00b	Control for SMBUS0 interrupt 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_79	31:30	00b	Control for IMC Smi request0 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl5 - RW – 8/16/32 bits - [SMI_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_80	1:0	00b	Control for IMC Smi request1 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl5 - RW – 8/16/32 bits - [SMI_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_81	3:2	00b	Control for Intruder event. 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_82	5:4	00b	Control for VBAT low 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_83	7:6	00b	Control for ProcHot 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_84	9:8	00b	Control for SERR# 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_85	11:10	00b	Control for FCH GPP Serr#(device 21, function 0) 01: SMI 10: NMI 11: IRQ13
SmiControl_86	13:12	00b	Control for FCH GPP Serr#(device 21, function 1) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_87	15:14	00b	Control for FCH GPP Serr#(device 21, function 2) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_88	17:16	00b	Control for FCH GPP Serr#(device 21, function 3) 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_89	19:18	00b	Control for ThermalTrip# assertion 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_90	21:20	00b	Control for Emulation64 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_91	23:22	00b	Control for Usb FLR 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_92	25:24	00b	Control for Sata FLR 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl5 - RW – 8/16/32 bits - [SMI_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_93	27:26	00b	Control for HD audio FLR 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_94	29:28	00b	Control for Gec FLR 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_95	31:30	00b	Control for Cmos Erase 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl6 - RW – 8/16/32 bits - [SMI_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_96	1:0	00b	Control for Irq0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_97	3:2	00b	Control for Irq1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_98	5:4	00b	Control for Irq2. 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_99	7:6	00b	Control for Irq3 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_100	9:8	00b	Control for Irq4 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_101	11:10	00b	Control for Irq5 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_102	13:12	00b	Control for Irq6 01: SMI 10: NMI 11: IRQ13
SmiControl_103	15:14	00b	Control for Irq7 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl6 - RW – 8/16/32 bits - [SMI_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_104	17:16	00b	Control for Irq8 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_105	19:18	00b	Control for Irq9 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_106	21:20	00b	Control for Irq10 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_107	23:22	00b	Control for Irq11 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_108	25:24	00b	Control for Irq12 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_109	27:26	00b	Control for Irq13 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_110	29:28	00b	Control for Irq14 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_111	31:30	00b	Control for Irq15 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl7 - RW – 8/16/32 bits - [SMI_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_112	1:0	00b	Control for Irq16 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_113	3:2	00b	Control for Irq17 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_114	5:4	00b	Control for Irq18 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl7 - RW – 8/16/32 bits - [SMI_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_115	7:6	00b	Control for Irq19 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_116	9:8	00b	Control for Irq20 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_117	11:10	00b	Control for Irq21 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_118	13:12	00b	Control for Irq22 01: SMI 10: NMI 11: IRQ13
SmiControl_119	15:14	00b	Control for Irq23 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_120	17:16	00b	Control for Vin0 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_121	19:18	00b	Control for Vin1 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_122	21:20	00b	Control for Vin2 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_123	23:22	00b	Control for Vin3 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_124	25:24	00b	Control for Vin4 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_125	27:26	00b	Control for Vin5 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_126	29:28	00b	Control for Vin6 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl7 - RW – 8/16/32 bits - [SMI_Reg: BCh]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_127	31:30	00b	Control for Vin7 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl8 - RW – 8/16/32 bits - [SMI_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_128	1:0	00b	Control for Internal Temp out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_129	3:2	00b	Control for Temp0 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_130	5:4	00b	Control for Temp1 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_131	7:6	00b	Control for Temp2 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_132	9:8	00b	Control for Temp3 out of limit 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_133	11:10	00b	Control for Fan Tach 0 too slow event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_134	13:12	00b	Control for Fan1 Tach too slow event 01: SMI 10: NMI 11: IRQ13
SmiControl_135	15:14	00b	Control for Fan2 Tach too slow event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_136	17:16	00b	Control for Fan3 Tach too slow event 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_137	19:18	00b	Control for Fan4 Tach too slow event 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl8 - RW – 8/16/32 bits - [SMI_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_138	21:20	00b	Control for FakeSts0 00: Disable 01: SMI 10: NMI 11: IRQ13 Note: FakeSts0 defined in PMIO can be programmed to generate SMI/NMI/IRQ13 specified in those two bits.
SmiControl_139	23:22	00b	Control for FakeSts1 00: Disable 01: SMI 10: NMI 11: IRQ13 Note: FakeSts1 defined in PMIO can be programmed to generate SMI/NMI/IRQ13 specified in those two bits.
SmiControl_140	25:24	00b	Control for FakeSts2 00: Disable 01: SMI 10: NMI 11: IRQ13 Note: FakeSts2 defined in PMIO can be programmed to generate SMI/NMI/IRQ13 specified in those two bits.
SmiControl_141	27:26	00b	Control for C state Message 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_142	29:28	00b	Control for Short timer 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_143	31:30	00b	Control for Long timer 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl9 - RW – 8/16/32 bits - [SMI_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_144	1:0	00b	Control for AB Smi trapping request 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_145	3:2	00b	Control for P state message 0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_146	5:4	00b	Control for P state message 1 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl9 - RW – 8/16/32 bits - [SMI_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_147	7:6	00b	Control for P state message 2 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_148	9:8	00b	Control for Io trapping 0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_149	11:10	00b	Control for Io trapping 1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_150	13:12	00b	Control for Io trapping 2 01: SMI 10: NMI 11: IRQ13
SmiControl_151	15:14	00b	Control for Io trapping 3 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_152	17:16	00b	Control for memory trapping 0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_153	19:18	00b	Control for memory trapping 1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_154	21:20	00b	Control for memory trapping 2 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_155	23:22	00b	Control for memory trapping 3 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_156	25:24	00b	Control for configuration cycle trapping 0 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_157	27:26	00b	Control for configuration cycle trapping 1 00: Disable 01: SMI 10: NMI 11: IRQ13
SmiControl_158	29:28	00b	Control for configuration cycle trapping 2 00: Disable 01: SMI 10: NMI 11: IRQ13

SmiControl9 - RW – 8/16/32 bits - [SMI_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
SmiControl_159	31:30	00b	Control for configuration cycle trapping 3 00: Disable 01: SMI 10: NMI 11: IRQ13

IoTrapping0 - RW – 8/16 bits - [SMI_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
IoTrapping0	15:0	00b	Specify the I/O address which causes SMI event.

IoTrapping1 - RW – 8/16 bits - [SMI_Reg: CAh]			
Field Name	**Bits**	**Default**	**Description**
IoTrapping1	15:0	00b	Specify the I/O address which causes SMI event.

IoTrapping2 - RW – 8/16 bits - [SMI_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
IoTrapping2	15:0	00b	Specify the I/O address which causes SMI event.

IoTrapping3 - RW – 8/16 bits - [SMI_Reg: CEh]			
Field Name	**Bits**	**Default**	**Description**
IoTrapping3	15:0	00b	Specify the I/O address which causes SMI event.

MemTrapping0 - RW – 8/16/32 bits - [SMI_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
MemTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
MemRdOvrEn	1	0b	Set to 1 to force read data to be replaced by MemRdOvrData0.
MemTrapping	31:2	00000000h	Specify the 30-bit memory address which causes SMI event; lowest 2 bits are ignored.

MemRdOvrData0 - RW – 8/16/32 bits - [SMI_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
MemRdOvrData	31:0	00h	The 32 bit data is used as the return data when the memory read trapping is enabled in MemTrapping0. with MemRdOvrEn = 1

MemTrapping1 - RW – 8/16/32 bits - [SMI_Reg: D8h]			
Field Name	**Bits**	**Default**	**Description**
MemTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
MemRdOvrEn	1	0b	Set to 1 to force read data to be replaced by MemRdOvrData1.
MemTrapping	31:2	00000000h	Specify the 30-bit memory address which causes SMI event; lowest 2 bits are ignored.

MemRdOvrData1 - RW – 8/16/32 bits - [SMI_Reg: DCh]			
Field Name	**Bits**	**Default**	**Description**
MemRdOvrData	31:0	00h	The 32 bit data is used as the return data when the memory read trapping is enabled in MemTrapping1. with MemRdOvrEn = 1.

MemTrapping2 - RW – 8/16/32 bits - [SMI_Reg: E0h]			
Field Name	**Bits**	**Default**	**Description**
MemTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
MemRdOvrEn	1	0b	Set to 1 to force read data to be replaced by MemRdOvrData2.
MemTrapping	31:2	00000000h	Specify the 30-bit memory address which causes SMI event; lowest 2 bits are ignored.

MemRdOvrData2 - RW – 8/16/32 bits - [SMI_Reg: E4h]			
Field Name	**Bits**	**Default**	**Description**
MemRdOvrData	31:0	00h	The 32 bit data is used as the return data when the memory read trapping is enabled in MemTrapping2. with MemRdOvrEn = 1

MemTrapping3 - RW – 8/16/32 bits - [SMI_Reg: E8h]			
Field Name	**Bits**	**Default**	**Description**
MemTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
MemRdOvrEn	1	0b	Set to 1 to force read data to be replaced by MemRdOvrData3.
MemTrapping	31:2	00000000h	Specify the 30-bit memory address which causes SMI event; lowest 2 bits are ignored.

MemRdOvrData3 - RW – 8/16/32 bits - [SMI_Reg: ECh]			
Field Name	**Bits**	**Default**	**Description**
MemRdOvrData	31:0	00h	The 32 bit data is used as the return data when the memory read trapping is enabled in MemTrapping3. with MemRdOvrEn = 1

CfgTrapping0 - RW – 8/16/32 bits - [SMI_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
CfgTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
IoTrappingRw0	1	0b	0: Trap on I/O read access on the address specified in IoTrappingAdr0 1: Trap on I/O write access on the address specified in IoTrappingAdr0
CfgTrapping	31:2	00000000h	Specify the I/O address which causes SMI event.

CfgTrapping1 - RW – 8/16/32 bits - [SMI_Reg: F4h]			
Field Name	**Bits**	**Default**	**Description**
CfgTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
IoTrappingRw1	1	0b	0: trap on I/O read access on the address specified in IoTrappingAdr1 1: trap on I/O write access on the address specified in IoTrappingAdr1
CfgTrapping	31:2	00000000h	Specify the I/O address which causes SMI event.

CfgTrapping2 - RW – 8/16/32 bits - [SMI_Reg: F8h]			
Field Name	**Bits**	**Default**	**Description**
CfgTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
IoTrappingRw2	1	0b	0: Trap on Io read access on the address specified in IoTrappingAdr2 1: Trap on Io write access on the address specified in IoTrappingAdr2
CfgTrapping	31:2	00000000h	Specify the I/O address which causes SMI event.

CfgTrapping3 - RW – 8/16/32 bits - [SMI_Reg: FCh]			
Field Name	**Bits**	**Default**	**Description**
CfgTrappingRw	0	0b	0: Trap on read access 1: Trap on write access
IoTrappingRw3	1	0b	0: Trap on Io read access on the address specified in IoTrappingAdr3 1: Trap on Io write access on the address specified in IoTrappingAdr3
CfgTrapping	31:2	00000000h	Specify the I/O address which causes SMI event.

2.3.6 GPIO Registers

GPIO registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from "AcpiMMioAddr" + 0x100 to "AcpiMMioAddr" + 0x1FF.

The base address "AcpiMMioAddr" is defined in PM_reg x24, with the default base address at "FED8_0000."

The GPIO registers are used to control the GPIO pin statuses. Each GPIO pin has one register associated with it: the pin GPIO<N>, where the N is in the range of 0 ~ 67, 128~150, 160~228, maps to the register offset <NNh>, where "NNh" is the hexadecimal of number N.

The GPIO registers also control the GEvent pins. The GEvent<X> pins, where the X is in the range of 0 ~ 23, map to the offset range 60h ~ 77h (or 96 ~ 119 in decimal). That means the register Gpio60 is to control pin GEvent0, register Gpio61 is to control GEvent1, and so on.

Gpio<N> – R/W 8 bits - [Gpio_Reg: NNh]			
Field Name	**Bits**	**Default**	**Description**
OwnedByImc	0	0b	This bit can only be written by IMC. If this bit is set, only IMC can write to bits 6:2 and bit 1 can no longer be written by host. This bit is always sticky.
OwnedByHost	1	0b	This bit can only be written by host (BIOS). If this bit is set, only host can write to bits 6:2 and bit 0 can no longer be written by IMC. This bit is always sticky.
Sticky	2	0b	If set, bits 6:3 are sticky. If cleared, bits 6:3 are reset back to default values whenever a reset occurs. This will allow every GPIO to be sticky or non-sticky
PullUpB	3	0b	0: Pull-up enable 1: Pull-up disabled
PullDown	4	0b	0: Pull down disabled 1: Pull down enabled
GpioOutEnB	5	1b	0: Output enable 1: Output disable
GpioOut	6	0b	Output state when GpioOutEnableB is enabled
GpioIn	7	0b	Read only – current pin state
See also IOMUX registers required to control the GPIO function that are muxed with other functions			

2.3.6.1 Additional Register Programming Requirement for GPIO Control

Some GPIO may require additional register programming besides the one mentioned above and in section 2.3.7 IOMUX Registers.

GPIO	Register to Program		Comments
GPIO160	PMIO DC bit 7 = 0b	PMIO E6[1:0] = 2'b01	These registers are required to be programmed before programming the GPIO / IOMUX registers.

2.3.7 IoMux Registers

IoMux registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from "AcpiMMioAddr" + 0xD00 to "AcpiMMioAddr" + 0xDFF.

The base address "AcpiMMioAddr" is defined in PM_reg x24, with the default base address at "FED8_0000."

The IoMux register is used to select the function for multi-function IO pins. For example, the pin "AD0/GPIO0" is a multi-function pin that can perform either the "AD0" function or "GPIO0" function. The first part of the pin name indicates the default function, the second part indicates the second function, and so on.

Hudson-1 has GPIO pins ranging from GPIO0 to GPIO228, mapped to IoMux registers IoMux00 to IoMuxE4 ("00" and "E4" are hexadecimal values). The IoMux registers also control the function selection for GEvent pins, with GEvent0~ GEvent23 mapped to GPIO96 ~ GPIO119.

IoMux<N>-Gpio<X> – R/W 8 bits - [IoMux_Reg: <N>h]			
Field Name	**Bits**	**Default**	**Description**
IOMux – GPIO<X>	1:0	00b	Multi-function IO pin function select for pin GPIO<X> 00: function-0 01: function-1 10: function-2 11: function-3
Reserved	7:2	000000b	Reserved

***Note:**
<N> denotes number in hexadecimal: 00h ~ E4h.
<X> denotes number in decimal: 0 ~ 228.
Function-{0,1,2,3} corresponds to multifunction assigned to the pin.
E.g. multifunction pin "SATA_IS4#/FANOUT3/GPIO55" function-0 corresponds to SATA_IS4, function-1 corresponds to FANOUT3 and function-2 corresponds to GPIO55.

2.3.8 Miscellaneous Registers

Miscellaneous registers are accessed by memory-mapped (or IO-mapped) IOs, and they range from "AcpiMMioAddr " + 0xE00 to "AcpiMMioAddr" + 0xEFF.

The base address "AcpiMMioAddr" is defined in PM_reg x24, with the default base address at "FED8_0000."

The Miscellaneous Registers block is used for e-fuse, strap, and clock control.

Register Name	Offset Address
GPPClkCntrol	00h
ClkOutputCntrl	04h
CGPllConfig1	08h
CGPllConfig2	0Ch
CGPllConfig3	10h
CGPllConfig4	14h

Register Name	Offset Address
CGPllConfig5	18h
CGPllConfig6	1Ch
OscFreqCounter	30h
HpetClkPeriod	34h
MiscClkCntrl	40h
PostCode	44h
StrapStatus	80h
StrapOverride	84h
CPU_PState0	C0h
CPU_PState1	C4h
CPU_CState0	D0h
CPU_CState1	D4h
SataPortSts	F0h

GPPClkCntrol – R/W – 32 bits - [MISC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK0 Clock Request mapping	3:0	Fh	GPP0 PCIE clock pins (GPP_CLK0P/GPP_CLK0N) output control by CLKREQ# pin GPP_CLK0P/GPP_CLK0N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP0 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP0 PCIE clock output pins if it is asserted. GPP0_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

GPPClkCntrol – R/W – 32 bits - [MISC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK1 Clock Request mapping	7:11	Fh	GPP1 PCIE clock pins (GPP_CLK1P/GPP_CLK1N) output control by CLKREQ# pin GPP_CLK1P/GPP_CLK1N pins are powered off when FCH is strapped to use an external clock and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP1 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off GPP1 PCIE clock output pins if it is asserted. GPP1_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)
GPP_CLK2 Clock Request mapping	11:8	Fh	GPP2 PCIE clock pins (GPP_CLK2P/GPP_CLK2N) output control by CLKREQ# pin GPP_CLK2P/GPP_CLK2N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP0 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP2 PCIE clock output pins if it is asserted. GPP2_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

GPPClkCntrol – R/W – 32 bits - [MISC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK3 Clock Request mapping	15:12	Fh	GPP3 PCIE clock pins (GPP_CLK3P/GPP_CLK3N) output control by CLKREQ# pin GPP_CLK3P/GPP_CLK3N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP0 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP3 PCIE clock output pins if it is asserted. GPP3_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)
GPP_CLK4 Clock Request mapping	19:16	Fh	GPP4 PCIE clock pins (GPP_CLK4P/GPP_CLK4N) output control by CLKREQ# pin GPP_CLK4P/GPP_CLK4N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP0 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP4 PCIE clock output pins if it is asserted. GPP4_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

GPPClkCntrol – R/W – 32 bits - [MISC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK5 Clock Request mapping	23:20	Fh	GPP5 PCIE clock pins (GPP_CLK5P/GPP_CLK5N) output control by CLKREQ# pin GPP_CLK5P/GPP_CLK5N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP0 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP5 PCIE clock output pins if it is asserted. GPP5_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)
GPP_CLK6 Clock Request mapping	27:24	Fh	GPP6 PCIE clock pins (GPP_CLK6P/GPP_CLK6N) output control by CLKREQ# pin GPP_CLK6P/GPP_CLK6N pins are powered off when FCH is strapped to use an external clock, and powered on when strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP6 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off GPP6 PCIE clock output pins if it is asserted. GPP6_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

GPPClkCntrol – R/W – 32 bits - [MISC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK7 Clock Request mapping	31:28	Fh	GPP7 PCIE clock pins (GPP_CLK7P/GPP_CLK7N) output control by CLKREQ# pin GPP_CLK7P/GPP_CLK7N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP7 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off GPP7 PCIE clock output pins if it is asserted. GPP7_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

ClkOutputCntrl – R/W – 32 bits - [MISC_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
GPP_CLK8 Clock Request mapping	3:0	Fh	GPP8 PCIE clock pins (GPP_CLK8P/GPP_CLK8N) output control by CLKREQ# pin GPP_CLK8P/GPP_CLK8N PCIE clock output pins are powered off when FCH is strapped to use an external clock, and powered on when strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP8 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off GPP8 PCIE clock output pins if it is asserted. GPP8_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)

ClkOutputCntrl – R/W – 32 bits - [MISC_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
SLT_GFX_CLK Clock Request Mapping	7:4	Fh	Gfx PCIE clock pins (SLT_GFX_CLKP/SLT_GFX_CLKN) output control SLT_GFX_CLKP/SLT_GFX_CLKN pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, Gfx PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off Gfx PCIE clock output pins if it is asserted. Gfx_CLKREQ_Mapping: 0000 – Off 0001 – CLK_REQ0# 0010 – CLK_REQ1# 0011 – CLK_REQ2# 0100 – CLK_REQ3# 0101 – CLK_REQ4# 0110 – CLK_REQ5# 0111 – CLK_REQ6# 1000 – CLK_REQ7# 1001 – CLK_REQ8# 1010 – CLK_REQGfx# 1011 ~ 1110 – Off, reserved 1111 – On (default)
CPU_HT/NB/DispClk override enable	8	0b	Enable clock buffers override control for CPU_HT, NB_HT, NB_PCIE, and NB_DISP differential clock outputs. The state of the following 4 differential clock pairs, CPU_HT_CLK, NB_HT_CLK, NB_PCIE_CLK & NB_DISP_CLK are controlled by the strap (LPCCLK1). The states are, Strap (LPCCLK1) = 1 : clock output buffers enable Strap (LPCCLK1) = 0 : clock output buffers OFF This “override enable bit” allows the clock output buffers can be controlled through ClkCntrol1 register regardless of the strap value. 0: Disable override control over clock strap (LPCCLK1) 1: Enable override control clock strap (LPCCLK1)
CPU_HT_CLK Power Down Enable	9	0b	Power down CPU_HT_CLK output buffer for power saving Set to 1 to power down the CPU_HT_CLK output buffer, this bit can only take effect when “CPU_HT/NB/DispClk override enable” is set to 1.
NB_HT_CLK Power Down Enable	10	0b	Power down NB_HT_CLK output buffer for power saving Set to 1 to power down the NB_HT_CLK output buffer, this bit can only take effect when “CPU_HT/NB/DispClk override enable” is set to 1.
NB_PCIE_CLK Power Down Enable	11	0b	Power down NB_PCIE_CLK output buffer for power saving Set to 1 to power down the NB_PCIE_CLK output buffer, this bit can only take effect when “CPU_HT/NB/DispClk override enable” is set to 1.

ClkOutputCntrl – R/W – 32 bits - [MISC_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
NB_DISP_CLK Power Down Enable	12	0b	Power down NB_DISP_CLK output buffer for power saving Set to 1 to power down the NB_DISP_CLK output buffer, this bit can only take effect when "CPU_HT/NB/DispClk override enable" is set to 1.
PCIE_RCLK Power Down Enable	13	0b	Power down PCIE_RCLK input buffer for power saving Set to 1 to power down the PCIE_RCLK input buffer.
Clock Buffer Driving Strength Control	15:14	01b	Drive Strength control for all the differential Clock Buffers (NB_HT/NB_DISP/SLT_GFX_CLK/GPP_CLK*) 00: 12 mA 01: 13 mA 10: 14 mA 11: 15 mA
Clock Buffer Bias Power Down Enable	16	1b	Set to 1 to power down the clock buffers bias current circuit for power saving.
Reserved	19:17	-	
CPU_HT_CLK voltage swing control	20	0b	Voltage swing control for CPU_HT_CLK output buffer. 0: High swing, 20% more than regular swing, recommend setting for K8 CPU 1: Normal swing

CGPllConfig1 – R/W – 32 bits - [MISC_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
CG1 Spread Spectrum Enable	0	0b	CG1_PLL Spread Spectrum Enable 0: Disable Spread Spectrum (default) 1: Enable Spread Spectrum
Reserved	4:!	-	
SATA clock source select	5	0b	SATA clock source frequency select from CG2_PLL 0: PLL 100Mhz (default) 1: Buffered 25Mhz
Reserved	6	-	
Cg1Pll_SS_AMOUNT_NFRAC_SLIP_0	7	0b	CG1 PLL spread magnitude (slip portion) when "Enhanced Spread Mode Enable" (MISC_Reg x08[8])" is set. This bit is not used when "Enhanced Spread Mode Enable" (MISC_Reg x08[8])" is not set. Only available for silicon revision A12 and above.
Enhanced Spread Mode Enable	8	0b	To enable enhanced Spread Spectrum Mode 0: Disable 1: Enable Only available for silicon revision A12 and above. **Note:** When the bit is set to 1, the control of Spread magnitude and spread range can be controlled separately. The spread range is controlled by Cg1Pll_Q_SS_DSFRAC, Cg1Pll_ FBDIV_FRACTION & Cg1Pll_ FBDIV. And the spread magnitude is controlled by Cg1Pll_SS_AMOUNT_DSFRAC, Cg1Pll_SS_AMOUNT_NFRAC_SLIP.

CGPllConfig1 – R/W – 32 bits - [MISC_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
CgPll_overclocking_test	9	0b	Over-clocking test enable 0: Disable 1: Enable
CG2 Reset	10	0b	CG2 PLL Reset Set to 1 to reset the CG2 PLL, the bit will be clear to '1' by hardware after reset sequence is done.
Cg2Pll_ OCLKBYX_SEL	12:11	00b	Source of OCLKBYX: non-slip clock running at 400MHz 0x0 = non-slip clock divided by 1 0x1 = non-slip clock divided by 2 0x2 = non-slip clock divided by 3 0x3 = non-slip clock divided by 4
Cg2Pll_Q_IBIAS	14:13	01b	CG2 PLL current bias adjustment
Cg2Pll_Q_ICO_IBIAS	16:15	10b	ICO current bias adjustment
Cg2Pll_Q_SCL_IBIAS	18:17	10b	SCL Dividers' current bias adjustment
Cg2Pll_ MODE_S_FORCE	22:19	0101b	Force calibration results to known state (Strap) Must bypass calibration logic by setting Cg2Pll_CAL_BYPASS =1
Cg2Pll_ CAL_BYPASS	23	0b	CG2 PLL Calibration by-pass mode select 0: Calibrate 1: Bypass calibration and use Cg2Pll_MODE_S_FORCE[3:0] setting.
Cg1Pll_ Q_CP	27:24	1h	CG1 PLL charge pump current adjustment. A11: Controls the charge pump for CG2, with default value = 7h. A12 & above: Controls the charge pump for CG1.
Cg1Pll_SS_AMOUNT_DSFRAC_12_9	31:28	0h	CG1 PLL spread magnitude (delta-sigma portion) when "Enhanced Spread Mode Enable" (MISC_Reg x08[8]) is set. These bits are not used when "Enhanced Spread Mode Enable" (MISC_Reg x08[8])" is not set. Only available for silicon revision A12 and above.

CGPllConfig2 – R/W – 32 bits - [MISC_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cg1Pll_Q_ LF_MODE	8:0	0FDh	CG1 PLL Loop filter mode settings A11: Controls the loop filter for CG2, with default value = 0EBh. A12 & above: Controls the loop filter for CG1.
Cg2Pll_REFDIV_LOAD	9	0b	When setting this bit, different CG2 PLL reference divider values can be loaded into CG2 PLL thru Cg2Pll_REF_DIV registers. Depending on LPCCLK1 clock mode strap, either 5'b00001 (integrated clock mode) or 5'b00100 (external clock mode) is loaded.
Cg2Pll_REF_DIV	14:10	00001b	Reference divider value for CG2 PLL 5'b00001 = 25Mhz 5'b00100 = 100Mhz
Cg2Pll_FBDIV	25:15	18h	Feedback divider value for CG2 PLL
Cg2Pll_FBDIV_FRACTION	29:26	0h	CG2PLL Fractional Control of feedback divider
Cg2Pll_ VCO_GAIN	31:30	0h	CG2 PLL VCO gain setting adjustment.

CGPllConfig3 – R/W – 32 bits - [MISC_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Cg1Pll_SS_STEP_SIZE_ DSFRAC_7_0	7:0	83h	Control spread step size (delta-sigma portion) bit-7 ~ bit-0. Use this to adjust modulation rate. A11: Controls the SS_STEP_SIZE_DSFRAC for CG2, with default value =18h. A12 & above: Controls the SS_STEP_SIZE_DSFRAC for CG1, with default value = 83h. **Note:** There are 16-bits of register to control spread step size; these bits are defined in various CGPllConfig registers: "SS_STEP_SIZE_DSFRAC_15_13" , "SS_STEP_SIZE_DSFRAC_12_8" & "SS_STEP_SIZE_DSFRAC_7_0".
Cg1Pll_Q_SS_DSFRAC	23:8	6666h	Delta Sigma signal. Fraction parameter for DS modulator, expresses x/1024. A11: Controls the SS_DSFRAC for CG2 with default value = 0000h. A12 & above: Controls the SS_DSFRAC for CG1 with default value = 6666h.
Cg1Pll_Q_SS_DSMODE	25:24	10b	Delta Sigma signal. Selects the order of DS modulator: 0: DS modulator is disabled (Default) 1: 1st order 2: 2nd order 3: 3rd order A11: Controls the SS_DSMODE for CG2 with default value =00h. A12 & above: Controls the SS_DSMODE for CG1.
Cg2Pll_CAL_FB	31:26	18h	PLL control bits for internal dividers for calibration

CGPllConfig4 – R/W – 32 bits - [MISC_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Cg2Pll_Q_HALFGM_EN	0	0b	Set second loop op-amp to ½ gm 0: Do not lower gm by 0.5 (Default). 1: Lower gm by 0.5
Cg2Pll_SEL_SPARE0	1	0b	Spare bit.
Cg2Pll_CNTL	11:2	000h	Bits for input control. IPPLL_CNTL[0] => Controls 100MHz bypass mux. 0: Send divider output to OPPLL_PCIe_CLK differential output path. 1: Send 100MHz PCIe Ref clock to OPCIe_CLK differential output. IPPLL_CNTL[4] => Enables Power Saving Mode in digital block. Tied to IPPLL_PWRSVG_EN on the digital block. 0: All blocks and dividers are enabled in the digital block (Default) 1: Some blocks and dividers are disabled in the digital block to save power and more importantly reduce noise. IPPLL_CNTL[5] => Enables Debug Bus output in digital block. Tied to IPPLL_DEBUG_EN on the digital block. 0: All 150MHz output from digital block are disabled (Default). 1: 150MHz outputs from digital block are enabled.
Cg2Pll_IVR_BIAS	15:12	0h	Adjust bias current for PLL regulator

CGPllConfig4 – R/W – 32 bits - [MISC_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Cg2Pll_ IVR_FILTER	17:16	0h	Bits for Regulator reference voltage Low Pass Filter
Cg2Pll_ IVR_LPF_C	21:18	0h	Voltage regulator bandwidth Capacitor adjustment Bit 0 if "1" remove 1X from total capacitance. Bit 1 if "1" remove 2X from total capacitance. Bit 2 if "1" remove 4X from total capacitance. Bit 3 removed programmability to improve PSRR. Default is 0000: Use all capacitors.
Cg2Pll_ IVR_LPF_R	25:22	0h	Voltage regulator bandwidth series Resistor adjustment Bit 0 if "1" short 140K from total resistance. Bit 1 if "1" short 281K from total resistance. Bit 2 if "1" short 562K from total resistance. Bit 3 if "1" short 1.124M from total resistance. Default is 0000: Use all resistors 2.1075M Ohms.
Cg2Pll_ IVR_PD	26	0b	Regulator Power Down.
Cg2Pll_ IVR_PG_BIT	31:27	00h	Voltage regulator Pass Gate control. Bit 0 if "1" disconnect 1/5th of the passgates. Bit 1 if "1" disconnect 1/5th of the passgates. Bit 2 if "1" disconnect 1/5th of the passgates. Bit 3 if "1" disconnect 1/5th of the passgates. Bit 4 if "1" disconnect 1/5th of the passgates. Default is 00000: Use all passgates (Maximum VCO current 30mA).

CGPllConfig5 – R/W – 32 bits - [MISC_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Cg2Pll_ IVR_RESET	0	0b	Regulator Reset
Cg2Pll_ IVR_TRIM	4:1	0h	Bit Setting Result Output Voltage 0000 1.222V (Nominal is 1.1V + 122mV) 0001 1.283V (+61mV) 0010 1.344V (+122mV) 0011 1.406V (+184mV) 0100 1.344V (+122mV) 0110 1.467V (+367mV) 0111 1.528V (+428mV) 1000 1.1V (-122mV) 1001 1.161V (-61mV) 1010 1.1V (-122mV) 1011 1.161V (-61mV) 1100 1.1V (-122mV) 1101 1.161V (-61mV) 1110 1.1V (-122mV) 1111 1.161V (-61mV)
Cg1Pll_FBDIV	12:5	18h	Feedback divider value for CG1 PLL

CGPllConfig5 – R/W – 32 bits - [MISC_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Cg1Pll's SS_STEP_SIZE_DSFRAC_15_14, SS_AMOUNT_FBDIV_0 / SS_AMOUNT_DSFRAC_15_13	15:13	0h	Controls spread step size (delta-sigma portion) bit-15 ~ bit-14. Use this to adjust modulation rate when "Enhanced Spread Mode Enable" (MISC_Reg x08[8]) is not set. Bit-13 is used to control spread magnitude (integer portion) when "Enhanced Spread Mode Enable" (MISC_Reg x08[8]) is not set. Controls the spread magnitude (delta-sigma portion) bit-15 ~ bit-13 when "Enhanced Spread Mode Enable" is set. This is only available in silicon revision A12 and above. **Note:** There are 16-bit of register to control spread step size; these bits are defined in various CGPllConfig registers: "SS_STEP_SIZE_DSFRAC_15_13" , "SS_STEP_SIZE_DSFRAC_12_8" & "SS_STEP_SIZE_DSFRAC_7_0".
Cg1Pll_ FBDIV_FRACTION	19:16	0h	CG1PLL Fractional Control of feedback divider
Cg2_FBMUX	20	0b	PLL feedback source
Cg1Pll_REFDIV	25:21	01h	CG1_PLL reference divider value. Only available for silicon revision A12 and above.

CGPllConfig6 – R/W – 32 bits - [MISC_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
Cg1Pll_SS_STEP_SIZE_ DSFRAC_12_8	5:0	00h	Controls spread step size (delta-sigma portion) bit-12 ~ bit-8. Use this to adjust modulation rate. Bit-5 is used to control the spread magnitude (slip portion) bit-1 (SS_AMOUNT_NFRAC_SLIP_1) when "Enhanced Spread Mode Enable" (MISC_Reg x08[8])" is set. Only available for silicon revision A12 and above. **Note:** There are 16-bits of register to control spread step size; these bits are defined in various CGPllConfig registers: "SS_STEP_SIZE_DSFRAC_15_13" , "SS_STEP_SIZE_DSFRAC_12_8" & "SS_STEP_SIZE_DSFRAC_7_0".
Reserved	31:6		Reserved

OscFreqCounter – R/W – 32 bits - [MISC_Reg: 30h]			
Field Name	**Bits**	**Default**	**Description**
OscCountPerSec	27:0	0000000h	Number of OSC clocks per 1 second. Whenever bit 31 (CountEnable) is set, an internal counter will start counting the number of OSC clocks per second and record the count value here.
Reserved	29:28	00b	Reserved
CountIsValid	30	0b	When OscCountPerSec is valid, this bit is set. This bit is read only. SW should always wait for this bit to be set before it should read OscCountPerSec
CountEnable	31	0b	When set, it enables the internal counter to count the number of OSC clocks. When SW is not using this function, it should always set it back to 0 to conserve power.

HpetClkPeriod - R/W 8/16/32 bits - [Misc_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
HpetClkPeriod	31:0	0429B17Eh	The register controls the value of clkperiod register in HPET MMIO register space.

MiscClkCntrl – R/W – 32 bits - [MISC_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Device_CLK1_sel	1:0	2'b00	Defines 14M_25M_48M_OSC output clock frequency on 14M_25M_48M_OSC pin. 00: 14Mhz (default) 01: 25Mhz 10: 48Mhz 11: 14Mhz
Device_Clk1_OutputEnB	2	1'b0	Device Clock1, 14M_25M_48M_OSC clock output enable 0: enable 1: disable
Device_Clk1_Testmode	3	1'b0	When set, 14M_25M_48M_OSC becomes a test port for clkgen_outpad. Debugging purpose only. This bit should not be set under normal operating condition Test port output will depend on the selection from ClkCntl2[19:17]
Device_CLK2_sel	5:4	2'b00	Defines 14M_25M_48M output clock frequency (Device_Clk2) on USBCLK/14M_25M_48M_OSC pin 00: 14Mhz (default) 01: 25Mhz 10: 48Mhz 11: 14Mhz
UsbClkCfg	6	1'b1	Defines whether USB uses the internal or external 48Mhz clock. If USB uses internal 48Mhz as clock source, USBCLK/14M_25M_48M_OSC pin can output 14/25/48Mhz clock depend on Device_CLK2_sel setting. If USB uses external 48Mhz clock as clock source, USBCLK/14M_25M_48M_OSC pin can't be used as Device clock output. Output enable of 14M_25M_48M_OSC pin control by UsbClkCfg and Device_Clk2_OutOff. When UsbClkCfg=1 & Device_Clk2_OutOff=0, pin output enable will be on. 0: external 48Mhz (default for A11) 1: internal 48Mhz (default for A12 and above)
Device_Clk2_OutOff	7	1'b0	If USB uses internal 48Mhz as clock source, set this to "1" will turn off USBCLK/14M_25M_48M_OSC clock output. 0: 14M_25M_48M_OSC pin output enable 1: 14M_25M_48M_OSC pin output disable. (Turn off Device_Clk2 output)
FC_Clk_Src	8	1'b0	FC Clock Source from CG1_PLL or CG2_PLL 0: FC clock source from CG1_PLL (default) 1: FC clock source from CG2_PLL. This is only for testing

MiscClkCntrl – R/W – 32 bits - [MISC_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
FC_Clk_Sel	11:9	3'b010	Flash Controller clock frequency 000: 100Mhz 001: 80Mhz 010: 66.6Mhz (default) 011: 57.14Mhz 100: 50Mhz 101: 44.4Mhz 110: 40Mhz 111: reserved
Device_14Mclk_Sel	12	1'b0	14Mhz clock selection for Device clock output 0: 14.285Mhz clock from CG2_PLL 1: 14.318Mhz clock from CLK_REQG#/14M_OSC/GPIO65 pin
TermResistorEn	13	1'b0	Enables the high speed clock termination resistors 0: Enable, default 1: Disable
14MhzEnable	14	1'b1	When this bit is set, the FCH will use the internal PLL to generate the 14Mhz.
BlinkClkSlowEnable	15	1'b0	When this bit is set, internal Blink clock will run on 66Mhz. The normal internal Blink clock is running on 133Mhz. See more detail on MISC_Reg: 40h[20]
FC_ClkStop	16	1'b0	Program this bit to "1" before change FC1x and 2x clock frequency, then program this bit to "0" to re-start FC clock
25MXtal_PWDN	17	1'b0	Power off 25M Xtal. Set this bit can power off 25Mhz Xtal pad when the following conditions is not true. (1) chip in integrated clock mode, or (2) GEC present, or (3) USB 48Mhz clock from CG2_PLL, or (4) SATA use CG2_PLL clock as ref clock source, or (5) 14.318Mhz clock generated from CG2_PLL (6) 25Mhz Device clock selected 0: power on 1: power off
DrvSth_Device_Clk1	18	1'b1	Drive Strength Control for Device Clock1 (14M_25M_48M_OSC) 0: 4 mA 1: 8 mA (Default)
DrvSth_Device_Clk2	19	1'b1	Drive Strength Control for Device Clock2 (USBCLK/14M_25M_48M_OSC) 0: 4 mA 1: 8 mA (Default)

MiscClkCntrl – R/W – 32 bits - [MISC_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Enable BlinkClkSlow Mode	20	1'b0	Set to 1 to enable internal core clock (Blink clock) running at slower speed (66Mhz) for power saving. This bit can only take effect when the pin strap mode "CoreSpeedMode" (control by pin AZ_SDOUT), is set to Low Power Mode. This feature is not supported on rev A12 and above.
Cg2Pll_VCOREF_Cntrl	22:21	2'b00	CG2Pll VCOREF Control. Only available for silicon revision A12 and above.
Cg2Pll_CALREF_Cntrl	24:23	2'b00	CG2Pll CALREF Control. Only available for silicon revision A12 and above.
Reserved	25	-	

PostCode – R 8 bits - [Misc_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
ValueOnPort80	7:0	0b	The 8 bits stores the current the value written to Port 80h

StrapStatus – R 8/16/32 bits - [Misc_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
FWHDisableStrap	0	0b	EcPwm3 pad
UseLpcRomStrap	1	1b	Inverted version from EcPwm2 pad Note: Both EcPwm3 and EcPwm2 straps pins are used to select boot ROM type.
ImcEnableStrap	2	0b	Enable IMC
BootFailTmrEnStrap	3	0b	Enable Watchdog function
ClkGenStrap	4	0b	Select 25Mhz crystal clock or 100Mhz PCIe® clock
DefaultModeStrap	5	1b	Select default debug straps
Reserved	6	-	Reserved
I2CRomStrap	7	0b	Getting UMI core strap from I2C ROM or using default value
ILAAutorunEnBStrap	8	1b	Enable trace memory auto run feature
FcPllBypStrap	9	1b	Bypass FC clock
PciPllBypStrap	10	0b	Bypass PCI PLL (used in functional test at tester)
ShortResetStrap	11	1b	Genearate short reset
Reserved	12	1b	PCI_ROM_BOOT strap
FastBif2cClkStrap	13	0b	Select fast BIF EPROM clocks
Reserved	14	-	Reserved
BlinkSlowModestrap	15	0b	Blink slow mode (100Mhz blink clock) strap
BIF_GEN2_COMPLIANCE_ Strap	16	0b	BIF gen 2 compliance strap
Reserved	31:17	4'h0000	Reserved

StrapOverride – R/W 8/16/32 bits - [Misc_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
Override FWHDisableStrap	0	0b	Override FWHDiableStrap value from external pin.
Override UseLpcRomStrap	1	0b	Override UseLpcRomStrap value from external pin.
Override EcEnableStrap	2	0b	Override EcEnableStrap value from external pin.
Override BootFailTmrEnStrap	3	0b	Override BootFailTmrEnStrap value from external pin.
Reserved	4	0b	Reserved
Override DefaultModeStrap	5	0b	Override DefaultModeStrap value from external pin.

StrapOverride – R/W 8/16/32 bits - [Misc_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	6	0b	Reserved
Override I2CRomStrap	7	0b	Override I2CRomStrap value from external pin.
Override ILAAutorunEnBStrap	8	0b	Override ILAAutorunEnBStrap value from external pin.
Override FcPllBypStrap	9	0b	Override FcPllBypStrap value from external pin.
Override PciPllBypStrap	10	0b	Override PciPllBypStrap value from external pin.
Override ShortResetStrap	11	0b	Override ShortResetStrap value from external pin.
Reserved	12	0b	Reserved
Override FastBif2ClkStrap	13	0b	Override FastBif2ClkStrap value from external pin’
Reserved	14	0b	Reserved
PciRomBoot Strap	15	0b	Override PCI Rom Boot Strap value from external pin’
BlinkSlowModestrap	16	0b	Override Blink Slow mode (100Mhz) from external pin’
ClkGenStrap	17	0b	Override CLKGEN from external pin.
BIF_GEN2_COMPL_Strap	18	0b	Override BIF_ GEN2_COMPLIANCE strap from external pin.
Reserved	30:19	0000h	Reserved
StrapOverrideEn	31	0b	Enable override strapping feature.

CPU_Pstate0 – R 8/16/32 bits - [Misc_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
Core0_PState	2:0	000b	FCH will monitor the P state of each CPU core (up to 16 cores) 000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core1_PState	6:4	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core2_PState	10:8	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core3_PState	14:12	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7

CPU_Pstate0 – R 8/16/32 bits - [Misc_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
Core4_PState	18:16	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core5_PState	22:20	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core6_PState	26:24	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core7_PState	30:28	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7

CPU_Pstate1 – R 8/16/32 bits - [Misc_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Core8_PState	2:0	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core9_PState	6:4	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core10_PState	10:8	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7

CPU_Pstate1 – R 8/16/32 bits - [Misc_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Core11_PState	14:12	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core12_PState	18:16	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core13_PState	22:20	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core14_PState	26:24	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7
Core15_PState	30:28	000b	000: P0 001: P1 010: P2 011: P3 100: P4 101: P5 110: P6 111: P7

CPU_Cstate0 – R 8/16/32 bits - [Misc_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Core0_CState	2:0	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core1_CState	6:4	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7

CPU_Cstate0 – R 8/16/32 bits - [Misc_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Core2_CState	10:8	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core3_CState	14:12	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core4_CState	18:16	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core5_CState	22:20	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core6_CState	26:24	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core7_CState	30:28	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7

CPU_Cstate1 – R 8/16/32 bits - [Misc_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
Core8_CState	2:0	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core9_CState	6:4	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core10_CState	10:8	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core11_CState	14:12	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core12_CState	18:16	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core13_CState	22:20	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7
Core14_CState	26:24	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7

CPU_Cstate1 – R 8/16/32 bits - [Misc_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
Core15_CState	30:28	000b	000: C0 001: C1 010: C2 011: C3 100: C4 101: C5 110: C6 111: C7

SataPortSts – RW 8/16/32 bits - [Misc_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
Port0Sts	0	-	This status bit indicates the internal status of each of the SATA port. The selected status of Port 0.
Port1Sts	1	-	The selected status of Port 1
Port2Sts	2	-	The selected status of Port 2
Port3Sts	3	-	The selected status of Port 3
Port4Sts	4	-	The selected status of Port 4
Port5Sts	5	-	The selected status of Port 5
Reserved	23:8	0000h	
SataPortSel	25:24	00b	00 - Select “led” for Port 0 to 5 01 – Select “det” for Port 0 to 5 10 – Select “err” for Port 0 to 5 11 – Select “led” for Port 0 to 5
Reserved	31:26	00h	

2.4 HD Audio Controller Registers (Device 20, Function 2)

2.4.1 HD Audio Controller PCI Configuration Space Registers

The PCI Configuration Space Registers define the operation of the Hudson-1's HD Audio controller on the PCI bus. These registers are accessible only when the HD Audio controller detects a Configuration Read or Write operation, with its IDSEL asserted.

Register Name	Address Offset
Device ID	00h
Vendor ID	02h
PCI Command	04h
PCI Status	06h
Revision ID	08h
Prog . Interface	09h
Sub Class Code	0Ah
Base Class Code	0Bh
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
BIST	0Fh
Lower Base Address Register	10h
Upper Base Address Register	14h
Subsystem Vendor ID	2Ch
Subsystem ID	2Eh
Capabilities Ptr	34h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Min Grant	3Eh
Max Latency	3Fh
Misc Control 1	40h
Misc Control 2	42h
Misc Control 3	43h
Intr Pin Control	44h
Capability Control	45h
Reserved	46h
Power Management Capability ID	50h
Next Capability Pointer	51h
Power Management Capabilities	52h
Power Management Control/Status	54h
MSI Capability ID	60h
Next Capability Pointer	61h
MSI Message Control	62h
MSI Lower Address	64h
MSI Upper Address	68h
MSI Message Data	6Ch
Reserved	70h – 75h

Vendor ID – R – 16 bits – [PCI_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1002h	Vendor Identifier. The vendor ID is 0x1002. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor IDs.

Device ID – R/W – 16 bits – [PCI_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	4383h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. Value is hardwired.

PCI Command – R/W – 16 bits – [PCI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved.
Memory Space Enable	1	0b	Memory Space Enable. This bit enables the HD Audio controller to respond to PCI memory space access.
Bus Master Enable	2	0b	This bit enables the HD Audio controller's bus mastering capability. 0: Disable 1: Enable
Reserved	9:3	00h	Reserved
Interrupt Disable	10	0b	Interrupt Disable. This bit disables the device from asserting INTx#. Note: This bit does not affect the generation of MSI. 0: Enable 1: Disable
Reserved	15:11	00h	Reserved

PCI Status – R/W – 16 bits – [PCI_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	2:0	0h	Reserved
Interrupt Status	3	0b	Interrupt status. This bit is "1" when INTx# is asserted. Note: This bit is not set by MSI.
Capabilities List	4	1b	PCI Capabilities List. This bit is hardwired to 1 to indicate that the HD Audio controller contains a capability pointer list. The first item is at offset 34h.
Reserved	12:5	00h	Reserved
Received Master Abort	13	0b	This bit, when set, indicates that the HD Audio controller has terminated a PCI bus operation with a Master Abort.
Reserved	15:14	0h	Reserved

Revision ID – R – 8 bits – [PCI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	40h	Chip Revision ID. This field is hardwired to 40h to indicate the revision level of the chip design.

Programming Interface – R – 8 bits – [PCI_Reg: 09h]			
Field Name	**Bits**	**Default**	**Description**
Programming Interface	7:0	00h	Programming Interface.

Sub Class Code – R – 8 bits – [PCI_Reg: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
Sub Class Code	7:0	03h	Sub Class Code. Indicates a HD Audio device in the context of a multimedia device class.

Base Class Code – R – 8 bits – [PCI_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Base Class Code	7:0	04h	Base Class Code. Indicates a multimedia device.

Cache Line Size – R/W – 8bits – [PCI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	This field is implemented as a read/write field for legacy compatibility purposes only and has no functional impact on the device's operations.

Latency Timer – R – 8 bits – [PCI_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Latency Timer	7:0	00h	Hardwired to 0.

Header Type – R – 8 bits – [PCI_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	00h	Hardwired to 0.

BIST – R – 8 bits – [PCI_Reg: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
BIST	15:0	0000h	Hardwired to 0.

Lower Base Address Register – R/W – 32 bits – [PCI_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Space Type	0	0	Hardwired to 0 to indicate this BAR is located in memory space only.
Address Range	2:1	10b	Hardwired to "10" to indicate this BAR can be located anywhere in 64-bit address space.
Prefetchable	3	0b	Hardwired to 0 to indicate this BAR is not prefetchable.
Reserved	13:4	000h	Hardwired to 0.
Lower Base Address	31:14	00000h	Lower Base Address for the HD Audio controller's memory mapped configuration registers. 16K bytes are requested when bits [13:4] are hardwired to 0.

Upper Base Address Register – R/W – 32 bits – [PCI_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
Upper Base Address	31:0	00000000h	Upper Base Address for the HD Audio controller's memory mapped configuration registers.

Subsystem Vendor ID – R/W – 16 bits – [PCI_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	This register is implemented as a write-once register. Any subsequent writes have no effect.

Subsystem ID – R/W – 16 bits – [PCI_Reg: 2Dh]			
Field Name	**Bits**	**Default**	**Description**
Subsystem ID	15:0	0000h	This register is implemented as a write-once register. Any subsequent writes have no effect.

Capabilities Pointer – R – 8 bits – [PCI_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	50h	This register indicates the offset for the capabilities pointer.

Interrupt Line – R/W – 8 bits – [PCI_Reg: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	This register is used to communicate to software the interrupt line that the interrupt pin is connected to. It is not used by the HD Audio controller.

Interrupt Pin – R – 8 bits – [PCI_Reg: 3Dh]			
Interrupt Pin	3:0	1h	This register reflects the value programmed into the Interrupt Control Pin register at offset 44h, bits [3:0]
Reserved	7:4	0h	Reserved

Minimum Grant – R – 8 bits – [PCI_Reg: 3Eh]			
Field Name	**Bits**	**Default**	**Description**
Minimum Grant	7:0	00h	Hardwired to 0.

Maximum Latency – R – 8 bits – [PCI_Reg: 3Fh]			
Field Name	**Bits**	**Default**	**Description**
Maximum Latency	7:0	00h	Hardwired to 0.

Reset Value: 0

Misc Control 1 – R/W – 16 bits – [PCI_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Static Output FIFO Size Select	1:0	00b	Static Output FIFO Size is functional only when the Static Output FIFO Size Enable (bit [8]) is set to “1”. 00: One-eighth of the maximum Output FIFO Size 01: One-quarter of the maximum Output FIFO size 10: One-half of the maximum Output FIFO Size 11: Use the maximum Output FIFO Size
Reserved	7:2	00h	Reserved
Static Output FIFO Size Enable	8	0b	Enable Static Output FIFO Size otherwise Output FIFO Size is set dynamically based on the stream format.
Reserved	15:9	00h	Reserved.

Misc Control 2 Register – R/W – 8 bits – [PCI_Reg: 42h]			
Field Name	**Bits**	**Default**	**Description**
Disable No Snoop	0	0b	0: Set the No Snoop attribute on Buffer Descriptor and Data Buffer DMA when the Traffic Priority bit is set in the Stream Descriptor 1: No Snoop attribute is disabled on Buffer Descriptor and Data Buffer DMA.
Disable No Snoop Override	1	0b	0: Override the bit [0] setting, meaning always generate No Snoop attribute on Buffer Descriptor and Data Buffer DMA 1: Bit [0] of this register controls the No Snoop attribute
Enable No Snoop Request	2	0b	0: Disable No snoop request to ACPI 1: Enable No Snoop request to ACPI When enabled and the DMA cycle is No Snoop, ACPI will not generate a wake to CPU in C2 state.
Reserved	3	0b	Reserved
Disable Minimum Retry	4	0b	0: Enable 1: Disable minimum retry on A-Link Bus When enabled, after the first request of a transaction, the HD audio controller will not generate another request for the same transaction unless notified by AB the data is available.
Enable Clock Gating	5	0b	0: Disable 1: Enable clock gating
Reserved	7:6	00h	Reserved

Misc Control 3 Register – R/W – 8 bits – [PCI_Reg: 43h]			
Reserved	7:0	00h	Reserved

Interrupt Pin Control Register – R/W – 8 bits – [PCI_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin Control	3:0	1h	Controls the value reported in Interrupt Pin register at PCI_Reg:3Dh[3:0].
Reserved	7:4	00h	Reserved

Capability Control Register – R/W – 8 bits – [PCI_Reg: 45h]			
Field Name	**Bits**	**Default**	**Description**
Enable MSI Capability	0	0b	0: Disable MSI capability 1: Enable MSI capability
Reserved	7:1	00h	Reserved

Reserved – R/W – 16 bits – [PCI_Reg: 46h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	-	

Power Management Capability ID – R – 8 bits – [PCI_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	01h	Hardwired to 0x01. Indicates PCI Power Management capability.

Power Management Capability ID – R – 8 bits – [PCI_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**

Next Capability Pointer – R – 8 bits – [PCI_Reg: 51h]			
Field Name	**Bits**	**Default**	**Description**
Next Capability Pointer	7:0	00h	00h: If MSI capability is disabled, indicates that this is the last capability structure in the list. 60h: If MSI capability is enabled, points to the next capability in the list.

Power Management Capabilities – R – 16 bits – [PCI_Reg: 52h]			
Field Name	**Bits**	**Default**	**Description**
Version	2:0	010b	Hardwired to 010b. Indicates this function complies with Revision 1.1 of the PCI Power Management Interface Specification
PME Clock	3	0b	Hardwired to 0. Indicates that no PCI clock is required for the function to generate PME#.
Reserved	4	0b	Reserved
Device Specific Initialization	5	0b	Hardwired to 0. Indicates that no device specific initialization is required.
Aux Current	8:6	001b	Hardwired to 001b. Indicates 55mA maximum suspend well current is required in the D3cold state.
D1 Support	9	0b	Hardwired to 0. Indicates D1 state is not supported.
D2 Support	10	0b	Hardwired to 0. Indicates D2 state is not supported.
PME Support	15:11	11001b	Hardwired to 11001b. Indicates PME# can be generated from D0 and D3 states.

Power Management Control/Status – R/W – 32 bits – [PCI_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
Power State	1:0	00b	This field is used both to determine the current power state and to set a new power state of the HD Audio controller.
Reserved	7:2	00h	Reserved
PME Enable	8	0b	Enables the function to assert PME#. This bit is in resume well and only cleared on power-on reset.
Reserved	14:9	00h	Reserved
PME Status	15	0b	This bit is set when HD Audio controller asserts the PME# signal. It is independent of the PME Enable bit. Writing a “1” clears this bit. This bit is in resume well and only cleared on power-on reset.
Reserved	31:16	0000h	Reserved

MSI Capability ID – R – 8 bits – [PCI_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
Capability ID	7:0	05h	Hardwired to 0x05. Indicates MSI capability.

Next Capability Pointer – R – 8 bits – [PCI_Reg: 61h]			
Field Name	**Bits**	**Default**	**Description**
Next Capability Pointer	7:0	00h	00h: Indicates that this is the last capability structure in the list.

MSI Message Control – R/W - 16 bits – [PCI_Reg: 62h]			
Field Name	**Bits**	**Default**	**Description**
MSI Enable	0	0b	Enables MSI if set to 1.
Multiple Message Capable	3:1	0h	Hardwired to 0. Indicates support for one message only.
Multiple Message Enable	6:4	0h	Hardwired to 0. Indicates support for one message only.
64 Bit Address Capability	7	1b	Hardwired to 1. Indicates the ability to generate 64-bit message address.
Reserved	15:8	00h	Reserved

MSI Message Lower Address – R/W - 32 bits – [PCI_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
MSI Message Lower Address	31:2	00000000h	Lower address used for MSI Message.
Reserved	01:0	00b	Reserved

MSI Message Upper Address – R/W - 32 bits – [PCI_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
MSI Message Upper Address	31:0	00000000h	Upper address used for MSI Message.

MSI Message Data – R/W - 16 bits – [PCI_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
MSI Message Data	15:00	0000h	Data used for MSI Message.

Reserved – R/W - 8 bits – [PCI_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

Reserved – R/W - 8 bits – [PCI_Reg: 71h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

Reserved – R/W - 8 bits – [PCI_Reg: 72h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

Reserved – R/W - 8 bits – [PCI_Reg: 73h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

Reserved – R/W - 8 bits – [PCI_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

Reserved – R/W - 8 bits – [PCI_Reg: 75h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

2.4.2 HD Audio Controller Memory Mapped Registers

The base memory location for these memory mapped registers is specified in the PCI Configuration Upper and Lower Base Adress Registers. The individual registers are then accessible at Base + offset as indicated in the following table. These registers are accessed in byte, word, or dword quantities.

Register Name	Address Offset
Global Capabilities	00h
Minor Version	02h
Major Version	03h
Output Payload Capability	04h
Input Payload Capability	06h
Global Control	08h
Wake Enable	0Ch
State Change Status	0Eh
Global Status	10h
Output Stream Payload Capability	18h
Input Stream Payload Capability	1Ah
Interrupt Control	20h
Interrupt Status	24h
Wall Clock Counter	30h
Stream Synchronization	38h
CORB Lower Base Address	40h
CORB Upper Base Address	44h
CORB Write Pointer	48h
CORB Read Pointer	4Ah
CORB Control	4Ch
CORB Status	4Dh
CORB Size	4Eh
RIRB Lower Base Address	50h
RIRB Upper Base Address	54h
RIRB Write Pointer	58h
RIRB Response Interrupt Control	5Ah
RIRB Control	5Ch
RIRB Status	5Dh
RIRB Size	5Eh
Immediate Command Output Interface	60h
Immediate Command Input Interface	64h
Immediate Command Input Interface Status	68h
DMA Position Buffer Lower Base Address	70h
DMA Position Buffer Upper Base Address	74h
Input Stream Descriptor 0	
Control	80h
Status	83h
Link Position in Current Buffer	84h
Cyclic Buffer Length	88h

Register Name	Address Offset
Last Valid Index	8Ch
FIFO Size	90h
Stream Descriptor Format	92h
Buffer Descriptor Lower Base Address	98h
Buffer Descriptor Upper Base Address	9Ch
Input Stream Descriptor 1	
Control	A0h
Status	A3h
Link Position in Current Buffer	A4h
Cyclic Buffer Length	A8h
Last Valid Index	ACh
FIFO Size	B0h
Stream Descriptor Format	B2h
Buffer Descriptor Lower Base Address	B8h
Buffer Descriptor Upper Base Address	BCh
Input Stream Descriptor 2	
Control	C0h
Status	C3h
Link Position in Current Buffer	C4h
Cyclic Buffer Length	C8h
Last Valid Index	CCh
FIFO Size	D0h
Stream Descriptor Format	D2h
Buffer Descriptor Lower Base Address	D8h
Buffer Descriptor Upper Base Address	DCh
Input Stream Descriptor 3	
Control	E0h
Status	E3h
Link Position in Current Buffer	E4h
Cyclic Buffer Length	E8h
Last Valid Index	ECh
FIFO Size	F0h
Stream Descriptor Format	F2h
Buffer Descriptor Lower Base Address	F8h
Buffer Descriptor Upper Base Address	FCh
Output Stream Descriptor 0	
Control	100h
Status	103h
Link Position in Current Buffer	104h
Cyclic Buffer Length	108h
Last Valid Index	10Ch
FIFO Size	110h
Stream Descriptor Format	112h
Buffer Descriptor Lower Base Address	118h
Buffer Descriptor Upper Base Address	11Ch

Register Name	Address Offset
Output Stream Descriptor 1	
Control	120h
Status	123h
Link Position in Current Buffer	124h
Cyclic Buffer Length	128h
Last Valid Index	12Ch
FIFO Size	130h
Stream Descriptor Format	132h
Buffer Descriptor Lower Base Address	138h
Buffer Descriptor Upper Base Address	13Ch
Output Stream Descriptor 2	
Control	140h
Status	143h
Link Position in Current Buffer	144h
Cyclic Buffer Length	148h
Last Valid Index	14Ch
FIFO Size	150h
Stream Descriptor Format	152h
Buffer Descriptor Lower Base Address	158h
Buffer Descriptor Upper Base Address	15Ch
Output Stream Descriptor 3	
Control	160h
Status	163h
Link Position in Current Buffer	164h
Cyclic Buffer Length	168h
Last Valid Index	16Ch
FIFO Size	170h
Stream Descriptor Format	172h
Buffer Descriptor Lower Base Address	178h
Buffer Descriptor Upper Base Address	17Ch
Alias Registers	
Wall Clock Counter Alias	2030h
Input Stream Descriptor 0 - Link Position in Current Buffer Alias	2084h
Input Stream Descriptor 1 - Link Position in Current Buffer Alias	20A4h
Input Stream Descriptor 2 - Link Position in Current Buffer Alias	20C4h
Input Stream Descriptor 3 - Link Position in Current Buffer Alias	20E4h
Output Stream Descriptor 0 - Link Position in Current Buffer Alias	2104h
Output Stream Descriptor 1 - Link Position in Current Buffer Alias	2124h
Output Stream Descriptor 2 - Link Position in Current Buffer Alias	2144h
Output Stream Descriptor 3 - Link Position in Current Buffer Alias	2164h

Global Capabilities – R – 16 bits - [Mem_Reg: Base + 00h]			
Field Name	**Bits**	**Default**	**Description**
64 Bit Address Supported	0	1	Hardwired to 1. Indicates that 64-bit addressing capability is supported by the HD Audio controller for BDL, data buffer, command buffer, and response buffer addresses.

Global Capabilities – R – 16 bits - [Mem_Reg: Base + 00h]			
Field Name	**Bits**	**Default**	**Description**
Number of Serial Data Output Signals	2:1	0	Hardwired to 0. Indicates that one SDO line is supported.
Number of Bidirectional Streams Supported	7:3	0	Hardwired to 0. Indicates that bidirectional stream is not supported.
Number of Input Streams Supported	11:8	4h	Hardwired to 4h. 4 Input Streams are supported.
Number of Output Streams Supported	15:12	4h	Hardwired to 4h. 4 Output Streams are supported.

Minor Version – R – 8 bits - [Mem_Reg: Base + 02h]			
Field Name	**Bits**	**Default**	**Description**
Minor Version	31:2	00000000h	Hardwired to 0.

Major Version – R – 8 bits - [Mem_Reg: Base + 03h]			
Field Name	**Bits**	**Default**	**Description**
Major Version	0	1b	Hardwired to 1.

Output Payload Capability – R – 16 bits - [Mem_Reg: Base + 04h]			
Field Name	**Bits**	**Default**	**Description**
Output Payload Capability	15:0	003Ch	Hardwired to 3Ch. Indicates the total output payload on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48kHz frame. The default link clock speed of 24MHz (double data rate) provides 1000 bits per frame minus 40 bits for command and control, leaving 960 bits (60 words) for data payload.

Input Payload Capability – R – 16 bits - [Mem_Reg: Base + 06h]			
Field Name	**Bits**	**Default**	**Description**
Input Payload Capability	15:0	001Dh	Hardwired to 1Dh. Indicates the total input payload on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48kHz frame. The default link clock speed of 24MHz provides 500 bits per frame minus 36 bits for response, leaving 464 bits (29 words) for data payload.

Global Control – R/W – 32 bits - [Mem_Reg: Base + 08h]			
Field Name	**Bits**	**Default**	**Description**
Controller Reset	0	0b	Writing a 0 to this bit causes the controller to transition to the Reset state. After the hardware has completed sequencing into the Reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit the Reset state and deassert the link RESET# signals. Software is responsible for setting/clearing this bit such that the minimum link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers.
Flush Control	1	0b	Writing a 1 to this bit initiates a flush. The flush is completed when Flush Status is set.
Reserved	7:2	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.
Accepted Unsolicited Response Enable	8	0b	If “1”, Unsolicited Response from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If “0”, Unsolicited Responses are accepted and dropped.
Reserved	31:9	000000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

Wake Enable – R/W – 16 bits - [Mem_Reg: Base + 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Wake Enable	3:0	0h	This field controls which SDIN signals may generate a wake event in response to a codec state change event. Bit [0] corresponds to Codec 0 – SDIN[0] Bit [1] corresponds to Codec 1 – SDIN[1] Bit [2] corresponds to Codec 2 – SDIN[2] Bit [3] corresponds to Codec 3 – SDIN[3] These bits are only cleared by a power-on reset.
Reserved	15:4	000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

State Change Status – R/W – 16 bits - [Mem_Reg: Base + 0Eh]			
Field Name	**Bits**	**Default**	**Description**
State Change Status Flags	3:0	0h	This field indicates which SDIN signal(s) received a State Change event. Bit [0] corresponds to Codec 0 – SDIN[0] Bit [1] corresponds to Codec 1 – SDIN[1] Bit [2] corresponds to Codec 2 – SDIN[2] Bit [3] corresponds to Codec 3 – SDIN[3] These bits are cleared by writing 1’s to them. These bits are only cleared by a power-on reset.
Reserved (R/W)	15:4	000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

Global Status – R/W – 16 bits - [Mem_Reg: Base + 10h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved. Software must use 0 for write to this bit.

Global Status – R/W – 16 bits - [Mem_Reg: Base + 10h]			
Field Name	**Bits**	**Default**	**Description**
Flush Status	1	0b	This bit is set to a “1” by hardware to indicate that the flush cycle initiated by setting the Flush Control has completed. Software must write a “1” to clear this bit before the next time Flush Control is set.
Reserved	15:2	0000h	Reserved. Software must use 0’s for write to these bits.

Output Stream Payload Capability – R – 16 bits - [Mem_Reg: Base + 18h]			
Field Name	**Bits**	**Default**	**Description**
Output Stream Payload Capability	15:0	003Ch	This field indicates the maximum number of words per frame for any single output stream. This measurement is in 16-bit word quantities per 48 kHz frame. The value must not be greater than the Output Payload Capability register value. Software must ensure that a format that would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h: No Limit (Stream size is limited only by Output Payload Capability register) 01h: 1-word payload : : FFh: 255-word payload

Input Stream Payload Capability – R – 16 bits - [Mem_Reg: Base + 1Ah]			
Field Name	**Bits**	**Default**	**Description**
Input Stream Payload Capability	15:0	0000h	This field indicates the maximum number of words per frame for any single input stream. This measurement is in units of 16-bit word per 48 kHz frame. The value must not be greater than the Input Payload Capability register value. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h: No Limit (Stream size is limited only by Input Payload Capability register) 01h: 1-word payload : : FFh: 255-word payload

Interrupt Control – R/W – 32 bits - [Mem_Reg: Base + 20h]			
Field Name	**Bits**	**Default**	**Description**
Stream Interrupt Enable	7:0	00h	When set to “1”, the individual streams are enabled to generate an interrupt when the corresponding stream status bits are set. A stream interrupt is caused as a result of a buffer with IOC in the BDL entry being completed or as a result of FIFO error. Control over the generation of each of these sources is in the associated Stream Descriptor. Bit [0]: Input Stream 0 Bit [1]: Input Stream 1 Bit [2]: Input Stream 2 Bit [3]: Input Stream 3 Bit [4]: Output Stream 0 Bit [5]: Output Stream 1 Bit [6]: Output Stream 2 Bit [7]: Output Stream 3
Reserved	29:8	000000h	Reserved
Controller Interrupt Enable	30	0b	Enables the general interrupt for controller functions. When set to “1’, the controller generates an interrupt when the corresponding status bit gets set due to a response interrupt, a response buffer overrun, and wake events.
Global Interrupt Enable	31	0b	Enables device interrupt generation. When set to “1”, the HD Audio device is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space such as the Interrupt Enable bit in the PCI configuration space.

Interrupt Status – R/W – 32 bits - [Mem_Reg: Base + 24h]			
Field Name	**Bits**	**Default**	**Description**
Stream Interrupt Status	7:0	00h	A “1” indicates that an interrupt condition occurred on the corresponding stream. These bits are cleared by writing 1’s to them. Note: These bits are set regardless of the state of the corresponding Interrupt Enable bits.
Reserved	29:8	000000h	Reserved
Controller Interrupt Status	30	0b	A “1” indicates that an interrupt condition occurred. This bit is cleared by writing a “1” to it. Note that this bit is set regardless of the state of the corresponding Interrupt Enable bit.
Global Interrupt Status	31	0b	This bit is an “OR” of all the interrupt status bits in this register.

Wall Clock Counter – R – 32 bits - [Mem_Reg: Base + 30h]			
Field Name	**Bits**	**Default**	**Description**
Wall Clock Counter	31:0	00000000h	32 bit counter that Is incremented at the link bitclock rate and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to 0 in periods of approximately 179 seconds with the nominal 24 MHz bitclock rate.

Stream Synchronization – R/W – 32 bits – [Mem_Reg: Base + 38h]			
Field Name	**Bits**	**Default**	**Description**
Stream Synchronization	7:0	00h	These bits, when set, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor. To synchronously start a set of DMA engines, the bits in this register are set to a “1”. The RUN bits for the associated Stream Descriptors can be set to a “1” to start the DMA engines. When all streams are ready, the associated Stream Synchronization bits can all be set to 0 at the same time, and transmission or reception from the link will begin together at the start of the next full link frame. To synchronously stop streams, these bits are set, and the RUN bits in the Stream Descriptors are cleared by software.
Reserved	31:8	000000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

CORB Lower Base Address – R/W – 32 bits – [Mem_Reg: Base + 40h]			
Field Name	**Bits**	**Default**	**Description**
CORB Lower Base Address Unimplemented Bits	6:0	00h	Hardwired to 0. This forces 128-byte buffer alignment for cache line fetch optimizations.
CORB Lower Base Address	31:7	0000000h	Upper 25 bits of the 32-bit Lower Base address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 1 KB boundary. This register must not be written when the DMA engine is running or the DMA transfer may be corrupted.

CORB Upper Base Address – RW – 32 bits – [Mem_Reg: Base + 44h]			
Field Name	**Bits**	**Default**	**Description**
CORB Upper Base Address	31:0	00000000h	Upper 32-bit address of the CORB. This register must not be written when the DMA engine is running or the DMA transfer may be corrupted.

CORB Write Pointer – R/W – 16 bits – [Mem_Reg: Base + 48h]			
Field Name	**Bits**	**Default**	**Description**
CORB Write Pointer	7:0	00h	Software writes the last valid CORB entry offset into this field in dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. This supports up to 256 CORB entries. This field may not be written while the DMA engine is running.
Reserved	15:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

CORB Read Pointer – R/W – 16 bits – [Mem_Reg: Base + 4Ah]			
Field Name	**Bits**	**Default**	**Description**
CORB Read Pointer	7:0	00h	Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. This field may be read while the DMA engine is running.
Reserved	14:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.
CORB Read Pointer Reset	15	0b	Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual prefetched commands in the CORB hardware buffer within the controller. The hardware will physically update this bit to 1 when the CORB pointer reset is complete. Software must read a 1 to verify that the reset has been completed correctly. Software must clear this bit back to 0, by writing a 0, and then read back the 0 to verify that the clearing has been completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.

CORB Control – R/W – 8 bits – [Mem_Reg: Base + 4Ch]			
Field Name	**Bits**	**Default**	**Description**
CORB Memory Error Interrupt Enable	0	0b	If this bit is set, the controller will generate an interrupt if the Memory Error Interrupt bit is set.
Enable CORB DMA Engine	1	0b	0: DMA Stop 1: DMA Run After software writes a "0" to this bit, the hardware may not stop immediately. The hardware will physically update the bit to "0" when the DMA engine is truly stopped. Software must read a "0" from this bit to verify that the DMA engine has truly stopped.
Reserved	7:2	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

CORB Status – R/W – 8 bits – [Mem_Reg: Base + 4Dh]			
Field Name	**Bits**	**Default**	**Description**
CORB Memory error Indication	0	0	If this status bit is set, the controller has detected an error in the pathway between the controller and memory. Writing a "1" to this bit will clear the bit, but a CRST must be performed before operation continues.
Reserved	7:2	0	Reserved. Software must use 0's for write to these bits.

CORB Size – R/W – 8 bits – [Mem_Reg: Base + 4Eh]			
Field Name	**Bits**	**Default**	**Description**
CORB Size	1:0	10b	These bits have no functional impact to the hardware. This HD Audio controller only supports 256 entries.
Reserved	3:2	00b	Reserved. Software must do a read-modify-write to preserve the value of these bits.
CORB Size Capability	7:4	0100b	Hardwired to 0100b indicating this controller only supports a CORB size of 256 entries.

RIRB Lower Base Address – RW – 32 bits – [Mem_Reg: Base + 50h]			
Field Name	**Bits**	**Default**	**Description**
RIRB Lower Base Address Unimplemented Bits	6:0	00h	Hardwired to 0. This forces 128-byte buffer alignment for cache line fetch optimizations.
RIRB Lower Base Address	31:7	0000000h	Upper 25 bits of the 32-bit Lower Base Address of the Response Input Ring Buffer, allowing the RIRB Base Address to be assigned on any 2 KB boundary. This register must not be written when the DMA engine is running or the DMA transfer may be corrupted.

RIRB Upper Base Address – RW – 32 bits – [Mem_Reg: Base + 54h]			
Field Name	**Bits**	**Default**	**Description**
RIRB Upper Base Address	31:0	00000000h	Upper 32-bit address of the RIRB. This register must not be written when the DMA engine is running or the DMA transfer may be corrupted.

RIRB Write Pointer – RW – 16 bits – [Mem_Reg: Base + 58h]			
Field Name	**Bits**	**Default**	**Description**
RIRB Write Pointer	7:0	00h	This field indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in two dwords since each RIRB entry is two dwords. This field may be read while the DMA engine is running.
Reserved	14:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.
RIRB Write Pointer Reset	15	0b	Software writes a “1” to this bit to reset the RIRB Write Pointer to 0’s. The DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.

RIRB Response Interrupt Count – R/W – 16 bits – [Mem_Reg: Base + 5Ah]			
Field Name	**Bits**	**Default**	**Description**
N Response Interrupt Count	7:0	00h	0x01: 1 Response sent to RIRB : 0xFF: 255 Responses sent to RIRB 0x00: 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note: Each response occupies two dwords in the RIRB. If more than one codec responds in one frame, the count is increased by the number of responses received in the frame.
Reserved	15:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

RIRB Control – R/W – 8 bits – [Mem_Reg: Base + 5Ch]			
Field Name	**Bits**	**Default**	**Description**
Response Interrupt Control	0	0b	0: Disable Interrupt 1: Generate an interrupt after N number of Responses are sent to the RIRB buffer or when an empty Response slot is encountered on all SDIN_x inputs after a frame that returned a response (whichever occurs first). The N counter is reset when the interrupt is generated.
RIRB DMA Enable	1	0b	0: DMA Stop 1: DMA Run
Response Overrun Interrupt Control	2	0b	If this bit is set, the hardware will generate an interrupt when the Response Overrun Interrupt Status is set.
Reserved	15:3	0000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

RIRB Status – R/W – 8 bits – [Mem_Reg: Base + 5Dh]			
Field Name	**Bits**	**Default**	**Description**
Response Interrupt	0	0b	Hardware sets this bit to “1” when an interrupt has been generated after N number of Responses are sent to the RIRB buffer or when empty Response slot is encountered on all SDIN_x inputs (whichever occurs first). Software clears this bit by writing a “1” to this bit.
Reserved	2	0b	Reserved. Software must use 0’s for write to these bits.
Response Overrun Interrupt Status	2	0b	Hardware sets this bit to a “1’ when an overrun occurs in the RIRB. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Software clears this bit by writing a “1” to it.
Reserved	7:3	00h	Reserved. Software must use 0’s for write to these bits.

RIRB Size – R/W – 8 bits – [Mem_Reg: Base + 5Eh]			
Field Name	**Bits**	**Default**	**Description**
RIRB Size	1:0	10b	These bits have no functional impact to the hardware. This HD Audio controller only supports 256 entries.
Reserved	3:2	00b	Reserved. Software must do a read-modify-write to preserve the value of these bits.
RIRB Size Capability	7:4	0100b	Hardwired to 0100b, indicating this controller only supports a RIRB size of 256 entries.

Immediate Command Output Interface – R/W – 32 bits – [Mem_Reg: Base + 60h]			
Field Name	**Bits**	**Default**	**Description**
Immediate Command Write	31:0	00000000h	The value written into this register is used as the verb to be sent out over the link when the ICB (Immediate Command Busy) bit is set to “1”. Software must ensure that the ICB bit is cleared before writing a value into this register or undefined behavior will result. Reads from this register will always return 0’s.

Immediate Command Input Interface – R/W – 32 bits – [Mem_Reg: Base + 64h]			
Field Name	**Bits**	**Default**	**Description**
Immediate Response Read	31:0	00000000h	This register contains the value from the last response to come in over the link. If multiple codecs have responded in the same frame, which one of the responses will be saved is indeterminate.

Immediate Command Input Interface – R/W – 16 bits – [Mem_Reg: Base + 68h]			
Field Name	**Bits**	**Default**	**Description**
Immediate Command Status	0	0b	This bit is a 0 when the controller can accept an immediate command. Software must wait for this bit to be 0 before writing a value in the ICW register. This bit will be clear (indicating "ready") when the following conditions are met: (1) the link is running, (2) the CORB is not active (CORBRP = CORBWP, or CORBEN is not set), and (3) there is no immediate command already in the queue waiting to be sent. Writing this bit to 1 will cause the contents of the ICW register to be sent as a verb in the next frame. Once a response is received, the IRV bit will be set and this bit will be cleared, indicating readiness to transmit another verb.
Immediate Result Valid	1	0b	This bit is set to a 1 by hardware when a new response is latched into the IRR (Immediate Response Read) register. Software must clear this bit before issuing a new command by writing a one to it, so that the software may determine when a new response has arrived.
Reserved	2	0b	Reserved. Software must use 0's for write to these bits.
Immediate Response Result Unsolicited	3	0b	Indicates whether the response latched in the Immediate Response Input Register is a solicited or unsolicited response.
Immediate Response Result Address	7:4	0h	The address of the codec which sent the response currently latched into the Immediate Response Input.
Reserved	15:8	00h	Reserved. Software must use 0's for write to these bits.

DMA Position Lower Base Address – R/W – 32 bits – [Mem_Reg: Base + 70h]			
Field Name	**Bits**	**Default**	**Description**
DMA Position Buffer Enable	0	0b	When this bit is set to a "1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically. Software can use this value to learn what data in memory is valid.
DMA Position Lower Base Address Unimplemented Bits	6:1	00h	Hardwired to 0. This forces 128-byte buffer alignment for cache line fetch optimizations.
DMA Position Lower Base Address	31:7	0000000h	Contains the upper 25 bits of the lower 32 bits of the DMA Position Buffer Base Address. This same address is used by the Flush Control, and must be programmed with a valid value before the Flush Control is initiated.

DMA Position Upper Base Address – R/W – 32 bits – [Mem_Reg: Base + 74h]			
Field Name	**Bits**	**Default**	**Description**
DMA Position Upper Base Address	31:0	00000000h	Upper 32 bits of the DMA Position Buffer Base Address. This same address is used by the Flush Control, and must be programmed with a valid value before the Flush Control is initiated.

Stream Descriptor Control – R/W – 24 bits Input Stream 0 - [Mem_Reg: Base + 80h] Input Stream 1 - [Mem_Reg: Base + A0h] Input Stream 2 - [Mem_Reg: Base + C0h] Input Stream 3 - [Mem_Reg: Base + E0h] Output Stream 0 - [Mem_Reg: Base + 100h] Output Stream 1 - [Mem_Reg: Base + 120h] Output Stream 2 - [Mem_Reg: Base + 140h] Output Stream 3 - [Mem_Reg: Base + 160h]			
Field Name	**Bits**	**Default**	**Description**
Stream Reset	0	0b	Writing a “1” causes the corresponding stream to be reset. The Stream Descriptor registers (except this bit), FIFOs, and cadence generator for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a “1” in this bit. Software must read a “1’ from this bit to verify that the stream is in reset. Writing a “0” causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a “0” in this bit. Software must read a “0” from this bit before accessing any of the stream registers. The Run bit must be cleared before asserting SRST (Stream Reset).
Stream Run	1	0b	When set to “1”, the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. When cleared to “0”, the DMA engine associated with this input stream will be disabled. If the corresponding SSYNC bit is “0”, input stream data will be taken from the link and moved to the FIFO and an over-run may occur.
Interrupt On Completion Enable	2	0b	Controls whether an interrupt is generated when the Buffer Completion Interrupt Status is set
FIFO Error Interrupt Enable	3	0b	Controls whether an interrupt is generated when the FIFO Error (Bit [3]) is set.
Descriptor Error Interrupt Enable	4	0b	Controls whether an interrupt is generated when the Descriptor Error Status is set.
Reserved	15:5	000h	Reserved. Software must do a read-modify-write to preserve the value of these bits.
Stripe Control	17:16	00b	The hardware only supports one SDO; this field has no functional impact.
Traffic Priority	18	0b	If set to “1”, it will cause the controller to generate non-snooped traffic.
Bidirectional Direction Control	19	0b	The hardware does not support bidirectional streams; this field has no impact.
Stream Number	23:20	0h	The value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal. When an input stream is detected on any of the SDIN_x signals that match this value, the data are loaded into the FIFO associated with this descriptor. 0000: Reserved 0001: Stream 1 : 1111: Stream 15

Stream Descriptor Status – R/W – 8 bits Input Stream 0 - [Mem_Reg: Base + 83h] Input Stream 1 - [Mem_Reg: Base + A3h] Input Stream 2 - [Mem_Reg: Base + C3h] Input Stream 3 - [Mem_Reg: Base + E3h] Output Stream 0 - [Mem_Reg: Base + 103h] Output Stream 1 - [Mem_Reg: Base + 123h] Output Stream 2 - [Mem_Reg: Base + 143h] Output Stream 3 - [Mem_Reg: Base + 163h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved. Software must use 0's for write to these bits.
Buffer Completion Interrupt Status	2	0b	For an Output Stream engine, this bit is set to "1" by the hardware after the last byte of data has been fetched from memory and put into DMA FIFO and the current descriptor has the IOC bit set. For an Input Stream engine, this bit is set to "1" by the hardware after the last byte of data has been removed from the DMA FIFO and the current descriptor has the IOC bit set. This bit is cleared by writing a "1" to this bit.
FIFO Error	3	0b	Set when a FIFO error occurs regardless of the FIFO Error Interrupt Enable bit. This bit is cleared by writing a "1" to this bit.
Descriptor Error	4	0b	During the fetch of a descriptor, an error has occurred.
FIFO Ready	5	0b	For an Output Stream, the controller hardware will set this bit to a "1" while the output DMA FIFO contains enough data to maintain the stream on the link.
Reserved	7:6	00b	Reserved. Software must use 0's for write to these bits.

Stream Descriptor Link Position in Buffer – R – 32 bits Input Stream 0 - [Mem_Reg: Base + 84h] Input Stream 1 - [Mem_Reg: Base + A4h] Input Stream 2 - [Mem_Reg: Base + C4h] Input Stream 3 - [Mem_Reg: Base + E4h] Output Stream 0 - [Mem_Reg: Base + 104h] Output Stream 1 - [Mem_Reg: Base + 124h] Output Stream 2 - [Mem_Reg: Base + 144h] Output Stream 3 - [Mem_Reg: Base + 164h]			
Field Name	**Bits**	**Default**	**Description**
Link Position in Buffer	31:0	00000000h	This field indicates the number of bytes that have been received off the link.

Stream Descriptor Cyclic Buffer Length – R/W – 32 bits Input Stream 0 - [Mem_Reg: Base + 88h] Input Stream 1 - [Mem_Reg: Base + A8h] Input Stream 2 - [Mem_Reg: Base + C8h] Input Stream 3 - [Mem_Reg: Base + E8h] Output Stream 0 - [Mem_Reg: Base + 108h] Output Stream 1 - [Mem_Reg: Base + 128h] Output Stream 2 - [Mem_Reg: Base + 148h] Output Stream 3 - [Mem_Reg: Base + 168h]			
Field Name	**Bits**	**Default**	**Description**
Cyclic Buffer Length	31:0	00000000h	Indicates the number of bytes in the complete cyclic buffer. Link Position in Buffer will be reset when it reaches this value. Software may only write to this register after a Global Reset, Controller Reset, or Stream Reset has occurred. Once the Run bit has been set to enable the engine, software must not write to this register until after the next reset is asserted or undefined events will occur.

Stream Descriptor Last Valid Index – R/W – 16 bits Input Stream 0 - [Mem_Reg: Base + 8Ch] Input Stream 1 - [Mem_Reg: Base + ACh] Input Stream 2 - [Mem_Reg: Base + CCh] Input Stream 3 - [Mem_Reg: Base + ECh] Output Stream 0 - [Mem_Reg: Base + 10Ch] Output Stream 1 - [Mem_Reg: Base + 12Ch] Output Stream 2 - [Mem_Reg: Base + 14Ch] Output Stream 3 - [Mem_Reg: Base + 16Ch]			
Field Name	**Bits**	**Default**	**Description**
Last Valid Index	7:0	00h	The value written to this register indicates the index for the last valid Buffer Descriptor in BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI (Last Valid Index) must be “1”; that is, there must be at least two valid entries in the BDL before DMA operations can begin. This value should not be modified except when the Run bit is “0”.
Reserved	15:8	00h	Reserved. Software must do a read-modify-write to preserve the value of these bits.

Stream Descriptor FIFO Size – R – 16 bits Input Stream 0 - [Mem_Reg: Base + 90h] Input Stream 1 - [Mem_Reg: Base + B0h] Input Stream 2 - [Mem_Reg: Base + D0h] Input Stream 3 - [Mem_Reg: Base + F0h] Output Stream 0 - [Mem_Reg: Base + 110h] Output Stream 1 - [Mem_Reg: Base + 130h] Output Stream 2 - [Mem_Reg: Base + 150h] Output Stream 3 - [Mem_Reg: Base + 170h]			
Field Name	**Bits**	**Default**	**Description**
FIFO Size	15:0	00h	For Output Stream, the FIFO Size varies between 32 dwords to 256 dwords depending on the Stream Format. For Input Stream, the FIFO Size is fixed at 64 dwords.

Stream Descriptor Format – R/W – 16 bits Input Stream 0 - [Mem_Reg: Base + 92h] Input Stream 1 - [Mem_Reg: Base + B2h] Input Stream 2 - [Mem_Reg: Base + D2h] Input Stream 3 - [Mem_Reg: Base + F2h] Output Stream 0 - [Mem_Reg: Base + 112h] Output Stream 1 - [Mem_Reg: Base + 132h] Output Stream 2 - [Mem_Reg: Base + 152h] Output Stream 3 - [Mem_Reg: Base + 172h]			
Field Name	**Bits**	**Default**	**Description**
Number of Channels	3:0	0h	Number of channels in each frame of the stream. 0000: 1 0001: 2 : 1111: 16
Bits per Sample	6:4	0h	000: 8 bits 001: 16 bits 010: 20 bits 011: 24 bits 100: 32 bits 101: 111: Reserved
Reserved	7	0b	Reserved. Software must do a read-modify-write to preserve the value of these bits.
Sample Base Rate Divisor	10:8	000b	000: Divide by 1 (48 kHz, 44.1 kHz) 001: Divide by 2 (24 kHz, 22.05 kHz) 010: Divide by 3 (16 kHz, 32 kHz) 011: Divide by 4 (11.025 kHz) 100: Divide by 5 (9.6 kHz) 101: Divide by 6 (8 kHz) 110: Divide by 7 111: Divide by 8 (6 kHz)
Sample Base Rate Multiple	13:11	000b	000: x1 (48 kHz, 44.1 kHz) 001: x2 (96 kHz, 88.2 kHz, 32 kHz) 010: x3 (144 kHz) 011: x4 (192 kHz, 176.4 kHz) 101 – 111: Reserved
Sample Base Rate	14	0b	0: 48 kHz 1: 44.1 kHz
Reserved	15	0b	Reserved

Stream Descriptor BDL Pointer Lower Base Address – R/W – 32 bits Input Stream 0 - [Mem_Reg: Base + 98h] Input Stream 1 - [Mem_Reg: Base + B8h] Input Stream 2 - [Mem_Reg: Base + D8h] Input Stream 3 - [Mem_Reg: Base + F8h] Output Stream 0 - [Mem_Reg: Base + 138h] Output Stream 2 - [Mem_Reg: Base + 158h] Output Stream 3 - [Mem_Reg: Base + 178h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	6:0	00h	Hardwired to 0's to force 128 byte alignment of the BDL.
Buffer Descriptor List Lower Base Address	31:7	0000000h	Upper 25 bits of the lower 32 bit address of the Buffer Descriptor List. This value should not be modified except when the Run bit is "0".

Stream Descriptor BDL Pointer Upper Base Address – R/W – 32 bits Input Stream 0 - [Mem_Reg: Base + 9Ch] Input Stream 1 - [Mem_Reg: Base + BCh] Input Stream 2 - [Mem_Reg: Base + DCh] Input Stream 3 - [Mem_Reg: Base + FCh] Output Stream 0 - [Mem_Reg: Base + 11Ch] Output Stream 1 - [Mem_Reg: Base + 13Ch] Output Stream 2 - [Mem_Reg: Base + 15Ch] Output Stream 3 - [Mem_Reg: Base + 17Ch]			
Field Name	**Bits**	**Default**	**Description**
Buffer Descriptor List Upper Base Address	31:0	00000000h	Upper 32 bit address of the Buffer Descriptor List. This value should not be modified except when the Run bit is "0".

Wall Clock Counter Alias – R – 32 bits – [Mem_Reg: Base + 2030h]			
Field Name	**Bits**	**Default**	**Description**
Wall Clock Counter Alias	31:0	00000000h	An alias of the Wall Clock Counter register at offset 0x30. It behaves exactly as if the Wall Clock Counter register were being read directly.

Stream Descriptor Link Position in Buffer Alias – R – 32 bits Input Stream 0 - [Mem_Reg: Base + 2084h] Input Stream 1 - [Mem_Reg: Base + 20A4h] Input Stream 2 - [Mem_Reg: Base + 20C4h] Input Stream 3 - [Mem_Reg: Base + 20E4h] Output Stream 0 - [Mem_Reg: Base + 2104h] Output Stream 1 - [Mem_Reg: Base + 2124h] Output Stream 2 - [Mem_Reg: Base + 2144h] Output Stream 3 - [Mem_Reg: Base + 2164h]			
Field Name	**Bits**	**Default**	**Description**
Link Position in Buffer Alias	31:0	00000000h	An alias of the Link Position in Buffer register of each Stream Descriptor.

Chapter 3 Register Descriptions: PCI Bridges

3.1 LPC ISA Bridge (Device 20, Function 3)

3.1.1 Programming Interface

- Enable legacy IO (ISA) address decode ranges
- Program DMA controller for any bus master or DMA cycles

3.1.2 PCI Configuration Registers

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
Command	04h
Status	06h
Revision ID/Class Code	08h
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
BIST	0Fh
Base Address Reg 0	10h
Subsystem ID & Subsystem Vendor ID	2Ch
Capabilities Pointer	34h
PCI Control	40h
IO Port Decode Enable Register	44h
IO/Mem Port Decode Enable Register	48h
Memory Range Register	4Ch
Rom Protect 0	50h
Rom Protect 1	54h
Rom Protect 2	58h
Rom Protect 3	5Ch
PCI Memory Start Address for LPC Target Cycles	60h
PCI Memory End Address for LPC Target Cycles	62h
PCI IO base Address for Wide Generic Port	64h
LPC ROM Address Range 1 (Start Address)	68h
LPC ROM Address Range 1 (End Address)	6Ah
LPC ROM Address Range 2 (Start Address)	6Ch
LPC ROM Address Range 2 (End Address)	6Eh
Firmware Hub Select	70h
Alternative Wide Io Range Enable	74h
Reserved	78h
TPM	7Ch
LPCCLKCntl	7Dh
Reserved	80h
TMKBC_BaseAddrLow	84h
TMKBC_BaseAddrHigh	88h
TMKBC_Remap	8Ch
Wide_IO2	90h
IMC_LPC_Cntrl	98h
Gec_ShadowRom_Address	9Ch
Spi_Base	A0h

Register Name	Offset Address
IMC_PortAddress	A4h
ROM_DMA_src_address	B0h
ROM_DMA_dst_address	B4h
RomDmaControl	B8h
IMCControl	BAh
HostControl	BBh
IMCRomWrOf	C0
IMCRomRdOf	C4

PCI function 3 configuration registers are described below.

Vendor ID- R - 16 bits - [PCI_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1002h	Vendor Identifier. The vendor ID is 0x1002. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor IDs

Device ID- R - 16 bits - [PCI_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	439Dh	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.

Command- RW - 16 bits - [PCI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
IO Space	0	1b	I/O Access Enable. This bit controls access to the I/O space registers. When this bit is 1, it enables access to the legacy IDE ports, and PCI bus master IDE I/O registers are enabled.
Memory Space	1	1b	Memory Access Enable. This function is not implemented. This bit is always 1.
Bus Master	2	1b	Bus Master Enable. 1: Enable 0: Disable.
Special Cycles	3	1b	Special Cycle Recognition Enable. This feature is not implemented and this bit is always 1.
Memory Write and Invalidate Enable	4	0b	Memory Write and Invalidate Enable. Not implemented. This bit is always 0.
VGA Palette Snoop	5	0b	VGA Palette Snoop Enable. The FCH does not need to snoop VGA palette cycles. This bit is always 0.
Parity Error Response	6	0b	PERR# (Response) Detection Enable bit. If set to 1, The FCH asserts PERR# when it is the agent receiving data AND it detects a parity error. PERR# is not asserted if this bit is 0.
Stepping Control	7	0b	Wait Cycle Enable. The FCH does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
SERR# Enable	8	0b	SERR# Enable. If set to 1, the FCH asserts SERR# when it detects an address parity error. SERR# is not asserted if this bit is 0.
Fast Back-to-Back Enable	9	0b	Fast Back-to-back Enable. The FCH only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
Reserved	15:10	00h	

Command- RW - 16 bits - [PCI_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**

Command Register: The PCI specification defines this register to control a PCI device's ability to generate and respond to PCI cycles. Writes to this register, except bit 6, have no effect. Bits[3:0]=0fh and are read only.

STATUS- RW - 16 bits - [PCI_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	
Capabilities List	4	0b	This bit is read only. When reg0x78[1] (Msi On) is 1, this bit reads 1; when reg0x78[1] (Msi On) is 0, this bit reads 0.
Reserved	7:5	0h	
Master Data Parity Error	8	0h	Data Parity Reported. Set to 1 if the FCH detects PERR# asserted while acting as PCI master (whether PERR# was driven by the FCH or not.)
Device Select Timing	10:9	1h	DEVSEL# Timing. Read-only bits indicating DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
Signaled Target Abort	11	0b	Signaled Target Abort. Set to 1 when the FCH signals Target Abort.
Received Target Abort	12	0b	Received Target Abort. Set to 1 when a FCH generated PCI cycle (the FCH is the PCI master) is aborted by a PCI target. Cleared by writing a 1 to it.
Received Master Abort	13	0b	Received Master Abort Status. Set to 1 when the FCH acts as a PCI master and aborts a PCI bus memory cycle. Cleared by writing a 1 to this bit.
Signaled System Error	14	0b	SERR# status. This bit is set to 1, when the FCH detects a PCI address parity error.
Detected Parity Error	15	0b	Detected Parity Error. This bit is set to 1 when the FCH detects a parity error.

Status Register: The PCI specification defines this register to record status information for PCI related events. This is a read/write register. However, writes can only reset bits. A bit is reset when the register is written and the data in the corresponding bit location is a 1.

Revision ID/Class Code - R - 32 bits - [PCI_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	00h	These bits are hardwired to 00h to indicate the revision level of the chip design.
Class Code	31:8	060100h	Class Code.

Revision ID/Class Code Register: This read only register contains the device's revision information and generic function. Since FCH is an ISA bridge, its assigned class code is 060100h.

Cache Line Size - R - 8 bits - [PCI_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	Cache Line Size.

Cache Line Size Register: This register specifies the system cache line size. This register is not implemented.

Latency Timer - R - 8 bits - [PCI_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Latency Timer	7:0	00h	Latency Timer.

Latency Timer Register: This register specifies the value of the Latency Timer in units of PCICLKs.

Header Type - R - 8 bits - [PCI_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	80h	Header Type.

Header Type - R - 8 bits - [PCI_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**

Header Type Register: This register identifies the type of the predefined header in the configuration space. Since THE FCH is a multifunction device, the most significant bit is set.

BIST- R - 8 bits - [PCI_Reg: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
BIST	7:0	00h	BIST.

Built-in Self Test Register: This register is used for control and status for Built-in Self Test. LPC has no BIST modes.

Base Address Reg 0 - RW* - 32 bits - [PCI_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Base Address 0	31:0	FEC0_0000h	Base address register 0.

* This register is write-only. Reading it always returns 0000_0000h. It has an internal value used as base address for APIC memory space. Writing to the register will change its internal value, but only bits[31:5] are overwritten, and bits[4:0] are hardwired to 00000b. The default internal value is FEC0_0000h.

Subsystem ID & Subsystem Vendor ID - W/R* - 32 bits - [PCI_Reg: 2Ch]			
Field Name	**Bits**	**Default**	**Description**
Subsystem Vendor ID	15:0	0000h	Subsystem Vendor ID.
Subsystem ID	31:16	0000h	Subsystem ID.

* This 4-byte register is a write-once & read-only afterward register. The BIOS writes this register once (all 4 bytes at once) and software reads its value (when needed).

Capabilities Pointer - R - 32 bits - [PCI_Reg: 34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	00h	When reg0x78[1] (Msi On) is 0, this field reads 0; when reg0x78[1] is 1, this field reads 80h, pointing to the starting address of the MSI Capability register.
Reserved	31:8	000000h	

PCI Control - RW - 8 bits - [PCI_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0h	
Legacy DMA Enable	2	1b	Setting it to 1 enables LPC DMA cycle. Note: 32-bit DMA is not supported. Transfer size: Channels 0-3: 8 bits, channels 5-7: 16 bits.

PCI Control - RW - 8 bits - [PCI_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	4:3	0h	
BiosSemaphore	5	0b	This bit is writeable by BIOS and read by the IMC. This is used as the software semaphore mechanism between BIOS and IMC to see who can access the common resource. BIOS should read bit[6] first to see if IMC has taken ownership of the resource first. If bit[6] is 0, then BIOS should write a 1 to this bit and then follow by a read to see if this bit is set. If this bit is set, it means BIOS has successfully taken ownership of the resource. If this bit returns 0 and bit[6] returns a 1, then IMC has taken ownership first. Software should always clear this bit after it has completed its access to the resource.
IMCSemaphore	6	0b	This bit is writeable by the IMC and read by BIOS. This is used as the software semaphore mechanism between BIOS and IMC to see who can access the common resource. IMC should read bit[5] first to see if BIOS has taken ownership of the resource first. If bit[5] is 0, then IMC should write a 1 to this bit and then follow by a read to see if this bit is set. If this bit is set, it means IMC has successfully taken ownership of the resource. If this bit returns a 0 and bit[5] returns a 1, then BIOS has taken ownership first. IMC should always clear this bit after it has completed its access to the resource.
IMCPresent	7	0b	This is a SW bit, which can be programmed by the IMC only to indicate to the host that IMC is present.

IO Port Decode Enable - RW - 32 bits - [PCI_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
Parallel Port Enable 0	0	0b	Port enable for parallel port, 378-37fh
Parallel Port Enable 1	1	0b	Port enable for parallel port, 778-77fh
Parallel Port Enable 2	2	0b	Port enable for parallel port, 278-27fh
Parallel Port Enable 3	3	0b	Port enable for parallel port, 678-67fh
Parallel Port Enable 4	4	0b	Port enable for parallel port, 3bc-3bfh
Parallel Port Enable 5	5	0b	Port enable for parallel port, 7bc-7bfh
Serial Port Enable 0	6	0b	Port enable for serial port, 3f8-3ffh

IO Port Decode Enable - RW - 32 bits - [PCI_Reg: 44h]			
Field Name	**Bits**	**Default**	**Description**
Serial Port Enable 1	7	0b	Port enable for serial port, 2f8-2ffh
Serial Port Enable 2	8	0b	Port enable for serial port, 220-227h
Serial Port Enable 3	9	0b	Port enable for serial port, 228-22fh
Serial Port Enable 4	10	0b	Port enable for serial port, 238-23fh
Serial Port Enable 5	11	0b	Port enable for serial port, 2e8-2efh
Serial Port Enable 6	12	0b	Port enable for serial port, 338-33fh
Serial Port Enable 7	13	0b	Port enable for serial port, 3e8-3efh
Audio Port Enable 0	14	0b	Port enable for audio port, 230-233h (range 220-22fh needs to be enabled using bits 0 and 1)
Audio Port Enable 1	15	0b	Port enable for audio port, 240-253h
Audio Port Enable 2	16	0b	Port enable for audio port, 260-273h
Audio Port Enable 3	17	0b	Port enable for audio port, 280-293h
MIDI Port Enable 0	18	0b	Port enable for MIDI port, 300-301h
MIDI Port Enable 1	19	0b	Port enable for MIDI port, 310-311h
MIDI Port Enable 2	20	0b	Port enable for MIDI port, 320-321h
MIDI Port Enable 3	21	0b	Port enable for MIDI port, 330-331h
MSS Port Enable 0	22	0b	Port enable for MSS port, 530-537h
MSS Port Enable 1	23	0b	Port enable for MSS port, 604-60bh
MSS Port Enable 2	24	0b	Port enable for MSS port, e80-e87h
MSS Port Enable 3	25	0b	Port enable for MSS port, f40-f47h
FDC Port Enable 0	26	0b	Port enable for FDC port, 3f0-3f7h
FDC Port Enable 1	27	0b	Port enable for FDC port, 370-377h
Game Port Enable	28	0b	Port enable for Game port, 200-20fh
KBC Port Enable	29	0b	Port enable for KBC port, 60 & 64h
ACPI Micro-Controller Port Enable	30	0b	Port enable for ACPI Micro-Controller port, 62 & 66h
Ad-Lib Port Enable	31	0b	Port enable for Ad-Lib port, 388-389h

This register controls the decoding of parallel, serial, audio, MID, and MSS, FDC, game, KBC, ACPI micro-controller, & Ad-lib ports. Writing 1 to a bit enables the corresponding I/O range.

IO/Mem Port Decode Enable - RW - 32 bits - [PCI_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
Super IO Configuration Port Enable	0	0b	Port enable for Super I/O Config Port, 2e-2fh
Alternate Super IO Configuration Port Enable	1	0b	Port enable for Alternate Super I/O Config Port, 4e-4fh
Wide Generic IO Port Enable	2	0b	Port enable for Wide Generic Port, see registers 64h-65h
Rom Range 1 Port Enable	3	0b	Port enable for LPC ROM address range 1 (memory), see registers 68h-6Bh
Rom Range 2 Port Enable	4	0b	Port enable for LPC ROM address range 2 (memory), see registers 6Ch-6Fh
Memory Range Port Enable	5	0b	Port enable for LPC memory target range, see registers 60h-63h
RTC IO Range Port Enable	6	0b	Port enable for RTC I/O range 70h~73h
Sync Timeout Counter Enable	7	0b	LPC sync timeout counter enabled when set to 1; otherwise the counter is disabled. This counter is used to avoid a deadlock condition if an LPC device drives sync forever. Timeout count is programmed in register0x49h. Write 0 to this bit if an LPC device is extremely slow & takes more than 255 LPC clocks to complete a cycle.
Sync Timeout Count	15:8	FFh	Sync Timeout Count. This is the number of LPC clocks that the state machine will wait when LPC data = sync before aborting the cycle (when Sync Timeout Counter Enable is set)
IO port enable 0	16	0b	Port enable for IO port 400h-43Fh

IO/Mem Port Decode Enable - RW - 32 bits - [PCI_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
IO port enable 1	17	0b	Port enable for IO port 480h-4BFh
IO port enable 2	18	0b	Port enable for IO port 500h-53Fh
IO port enable 3	19	0b	Port enable for IO port 580h-5BFh
Mem port enable	20	0b	Port enable for 4K byte memory range defined in reg0x4C
IO port enable 4	21	0b	Port enable for IO port 80h
IO port enable 5	22	0b	Port enable for IO port 4700h-470Bh
IO port enable 6	23	0b	Port enable for IO port FD60h-FD6Fh
Wide_io1_enable	24	0b	Wide IO port 1 (defined in registers 66/67h) enable
Wide_io2_enable	25	0b	Wide IO port 2 (defined in registers 90/91h) enable
Reserved	31:26	0b	

This register controls the decoding of Super I/O configuration, alternate Super I/O configuration, wide generic ports, ROM1 & ROM2 ports, and memory port. Writing a 1 to a bit enables the corresponding IO/ROM/Memory range.

Memory Range - RW - 32 bits - [PCI_Reg: 4Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	11:0	0	
Base Address	31:12	0	This register defines a 4K byte memory range from {Base Address, 000h} to {Base Address, FFFh}. The range is enabled by reg0x4A[4] (Mem port enable).

Rom Protect 0 - RW - 32 bits - [PCI_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
Write Protect	0	0b	When this bit is set, the memory range defined by this register is write-protected. Writing to the range has no effect.
Read Protect	1	0b	When this bit is set, the memory range defined by this register is read-protected. Reading any location in the range returns FFFF_FFFFh.
Rom Offset	10:2	000h	Rom range offset
Rom Base	31:11	000000h	Rom Base and Rom Offset together define the ROM range to be protected. The range is: From {Rom Base, 000_0000_0000b} to {Rom Base, 000_0000_0000b} + {0_0000_0000_0000b, Rom Offset, 11_1111_1111b}

For Host, this register is write/read, but it can only be written once after hardware reset. Subsequent writes to it have no effect. For IMC, this register is always write/read

Rom Protect 1 - RW - 32 bits - [PCI_Reg: 54h]			
Field Name	**Bits**	**Default**	**Description**
This register has exactly the same definition as that of Rom Protect 0.			

Rom Protect 2 - RW - 32 bits - [PCI_Reg: 58h]			
Field Name	**Bits**	**Default**	**Description**
This register has exactly the same definition as that of Rom Protect 0.			

Rom Protect 3 - RW - 32 bits - [PCI_Reg: 5Ch]			
Field Name	**Bits**	**Default**	**Description**
This register has exactly the same definition as that of Rom Protect 0.			

PCI Memory Start Address for LPC Target Cycles - RW - 16 bits - [PCI_Reg: 60h]			
Field Name	**Bits**	**Default**	**Description**
Memory Start Address	15:0	0000h	16-bit starting address of the LPC target (memory) range.

This register contains the upper 16 bits of the starting address of the LPC memory target range. The lower 16 bits of the starting address are considered 0's. This range can be enabled/disabled using reg0x48[5] (Memory Range Port Enable).

PCI Memory End Address for LPC Target Cycles - RW - 16 bits - [PCI_Reg: 62h]			
Field Name	**Bits**	**Default**	**Description**
Memory End Address	15:0	0000h	16-bit END address of the LPC target (memory) range.

This register contains the upper 16 bits of the ending address of the LPC memory target range. The lower 16 bits of the end address are considered 1's. This range can be enabled/disabled using reg0x48[5] (Memory Range Port Enable).

PCI IO base Address for Wide Generic Port - RW - 32 bits - [PCI_Reg: 64h]			
Field Name	**Bits**	**Default**	**Description**
IO Base Address 0	15:0	0000h	16-bit PCI I/O base address for wide generic port range. 512byte wide range. This function is enabled by reg0x48[2] (Wide Generic IO Port Enable).
IO Base Address 1	31:16	0000h	16-bit PCI I/O base address for wide generic port range. 512byte wide range. This function is enabled by reg0x4B[0] (Super IO Configuration Port Enable).

This register contains two 16-bits of I/O base address for LPC I/O (wide generic port) target range. The limit address is found by adding 512 to the base address.

LPC ROM Address Range 1 (Start Address) - RW - 16 bits - [PCI_Reg: 68h]			
Field Name	**Bits**	**Default**	**Description**
Rom Start Address 1	15:0	08h (if iLpc_Rom strap is enabled), 00h (if the strap is disabled)	16-bit starting address of the LPC ROM (memory) address range 1. Default is set to 512K below 1M.

This register contains the upper 16 bits of the starting address of the LPC ROM address range 1. The lower 16 bits of the starting address are considered 0's. This range can be enabled/disabled using reg0x48[3] (Rom Range 1 Port Enable) or when the strap pins are set to choose LPC ROM.

LPC ROM Address Range 1 (End Address) - RW - 16 bits - [PCI_Reg: 6Ah]			
Field Name	**Bits**	**Default**	**Description**
Rom End Address 1	15:0	0fh (if iLpc_Rom strap is enabled), 00h (if the strap is disabled)	16-bit END address of the LPC ROM (memory) address range 1.

This register contains the upper 16 bits of the ending address of the LPC ROM address range 1. The lower 16 bits of the end address are considered 1's. This range can be enabled/disabled using reg0x48[3] (Rom Range 1 Port Enable) or when the strap pins are set to choose LPC ROM.

LPC ROM Address Range 2 (Start Address)- RW - 16 bits - [PCI_Reg: 6Ch]			
Field Name	**Bits**	**Default**	**Description**
Rom Start Address 2	15:0	FFF8h (if iLpc_Rom strap is enabled), 00h (if the strap is disabled)	16-bit starting address of the LPC ROM (memory) address range 2. Default is set to 512K below 4GB

This register contains the upper 16 bits of the starting address of the LPC ROM address range 2. The lower 16 bits of the starting address are considered 0's. This range can be enabled/disabled using reg0x48[4] (Rom Range 2 Port Enable) or when strap pins are set to choose LPC ROM.

LPC ROM Address Range 2 (End Address) - RW - 16 bits - [PCI_Reg: 6Eh]			
Field Name	**Bits**	**Default**	**Description**
Rom End Address 2	15:0	FFFFh (if iLpc_Rom strap is enabled), 00h (if the strap is disabled)	16-bit END address of the LPC ROM (memory) address range 2.

This register contains the upper 16 bits of the ending address of the LPC ROM address range 2. The lower 16 bits of the end address are considered 1's. This range can be enabled/disabled using reg0x48[4] (Rom Range 2 Port Enable) or when the strap pins are set to choose LPC ROM.

Firmware Hub Select – RW* - 32 bits - [PCI_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
FWH_C0_IDSEL	3:0	7h	IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC0 0000h-FFC7 FFFFh FF80 0000h-FF87 FFFFh
FWH_C8_IDSEL	7:4	6h	IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC8 0000h-FFCF FFFFh FF88 0000h-FF8F FFFFh
FWH_D0_IDSEL	11:8	5h	IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD0 0000h-FFD7 FFFFh FF90 0000h-FF97 FFFFh
FWH_D8_IDSEL	15:12	4h	IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD8 0000h-FFDF FFFFh FF98 0000h-FF9F FFFFh
FWH_E0_IDSEL	19:16	3h	IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE0 0000h-FFE7 FFFFh FFA0 0000h-FFA7 FFFFh
FWH_E8_IDSEL	23:20	2h	IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE8 0000h-FFEF FFFFh FFA8 0000h-FFAF FFFFh
FWH_F0_IDSEL	27:24	0h	IDSEL for two 512 KB FWH memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFF0 0000h-FFF7 FFFFh FFB0 0000h-FFB7 FFFFh
FWH_F8_IDSEL	31:28	0h	IDSEL for two 512 KB FWH memory ranges and one 128KB memory range. This field is fixed at 0000. The IDSEL in this field addresses the following memory ranges: FFF8 0000h-FFFF FFFFh FFB8 0000h-FFBF FFFFh 000E 0000h-000F FFFFh

This register is used to generate the 4-bit IDSEL phase when LPC does read/write to firmware hub memory on the LPC bus. If the PCI address falls within certain range, the 4-bit value in the register for that range is used as IDSEL. Every firmware hub memory on LPC bus has 4 strap pins. If the value on those pins matches IDSEL from LPC host, the memory is selected.
*bits[31:28] are read-only
*bits[27:24] are read-only when the IMC strap pin is on.
Default value: 00234567h

Alternative Wide IO Range Enable - WR - 32 bits - [PCI_Reg: 74h]			
Field Name	**Bits**	**Default**	**Description**
Alternative Wide Io Range Enable	0	0b	Wide I/O range is usually 512 bytes. With this bit set, the range changes to 16 bytes only. To use this feature, address in reg0x64~65 must be aligned to 16 bytes, i.e., bits[3:0] must be 0. If the address is not aligned to 16 bytes, the I/O range is from address[15:0] to {address[15:4], 0xF}.
Reserved	1	0b	
Alternative Wide Io 1 Range Enable	2	0b	Similar to bit[0], but it applies to I/O address defined in reg0x66~67.
Alternative Wide Io 2 Range Enable	3	0b	Similar to bit[0], but it applies to I/O address defined in reg0x90~91.
Reserved	7:4	00h	

Miscellaneous Control Bits - WR - 8 bits - [PCI_Reg: 78h]			
Field Name	**Bits**	**Default**	**Description**
No Hog	0	1b	1: Turn on the feature so that bus master/DMA cycle will not hog PCI bus. LPC slave cycle will get retry if it visits LPC during that period. 0: Keep the old way, i.e., when bus master/DMA cycle is going on on LPC, it holds PCI grant, so no LPC slave cycle can interrupt and visit LPC.
Msi On	1	0b	1: Turn on LPC MSI Capability. The following will be true: * Reg0x06[4] (Capabilities List) reads 1. * Reg0x34[7:0] (Capabilities Pointer) reads 80h 0: Turn off LPC MSI Capability. The following will be true: * Reg0x06[4] (Capabilities List) reads 0. * Reg0x34[7:0] (Capabilities Pointer) reads 0.
LDRQ0	2	1b	Enable LDRQ0# on LPC bus if set to 1
LDRQ1	3	1b	Enable LDRQ1# on LPC bus if set to 1
SMMWriteRomEn	4	1b	Enable Rom access in SMM mode
Reserved	31:4	00000_000h	

TPM (trusted platform module) - WR - 8 bits - [PCI_Reg: 7Ch]			
Field Name	**Bits**	**Default**	**Description**
Tpm12_en	0	0b	When set to 1, it enables decoding of tpm (trusted platform module) cycles defined in TPM1.2 spec (refer to the addresses defined in bit[1] below). Note that tpm12_en and tpm_legacy are independent bits; they respectively turn on decoding of different tpm addresses.

TPM (trusted platform module) - WR - 8 bits - [PCI_Reg: 7Ch]			
Field Name	**Bits**	**Default**	**Description**
Tpm_amd	1	0b	This bit is replaced with strap pin and no longer in use. It is read-only and returns 0. When the strap is 0, it ONLY supports these normal tpm cycles. Below are the cycle definitions (left-hand-side is system/software memory address, which is translated to LPC I/O address on the right hand side.) 0xFED4_0xxx --> 0x0xxx 0xFED4_1xxx --> 0x1xxx 0xFED4_2xxx --> 0x2xxx 0xFED4_3xxx --> 0x3xxx 0xFED4_4xxx --> 0x4xxx When the strap is 1, it ONLY supports these AMD tpm cycles. 0xFED4_0xxx --> 0x0xxx 0xFED4_1xxx --> 0x1xxx 0xFED4_2xxx --> 0x2xxx 0xFED4_3xxx --> 0x3xxx 0xFD_F920_0000~0xFD_F923_FFFF --> 0x4028 0xFD_F928_0000~0xFD_F928_0003 --> 0x4020 0xFD_F928_0004~0xFD_F928_0007 --> 0x4024~0x4027
Tpm_legacy	2	0b	When set to 1, it enables decoding of legacy tpm addresses, i.e., I/O addresses 7E/7F and EE/EF will be decoded.
Tmkbc_enable	3	0b	Enable bit for the TMKBC function
Tmkbc_set	4	0b	Write once bit. Once set, all tmkbc address/remap registers cannot be changed until the next reset.
Tmkbc_sel	6:5	0b	Select which one of the four sets of tmkbc registers (specified in the registers 84h, 88h, and 8Ch) to be accessed.
WiderTpmEn	7	0b	Set to 1 to force logic to decode FED4xxxx as TPM cycles instead of FED4_0xxx, FED4_1xxx, FED4_2xxx, FED4_3xxx, and FED4_4xxx.

Note: any tpm cycle above is decoded only when the cycle is started by ALinkBridge. Access from bus master devices is not allowed.

LPCCLKCntl - RW - 8 bits - [PCI_Reg: 7Dh]			
Field Name	**Bits**	**Default**	**Description**
GpioLpcClk1	0		Read only. Status of LpcClk1 port
GpioLpcClk1OeB	1	1b	R/W. 1: disable GpioLpcClk1 output 0: enable GpioLpcClk1 output
GpioLpcClk1Out	2	0b	R/W, control GpioLpcClk1 output value
LpcClk1IsGpio	3	1b	R/W. 1: Treat LpcClk1IsGpio as GPIO 0: Treat LpcClk1IsGpio as LpcClk1
LPCCLK1 can be configured to GPIO only if the IMC is enabled via strap or by software (BIOS)			
Reserved	7:4	0000b	

Reserved – R – 32 bits – [PCI_Reg: 80h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

TMKBC_BaseAddrLow - RW - 32 bits - [PCI_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	

TMKBC_BaseAddrLow - RW - 32 bits - [PCI_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
Addr64	2	0b	Defines whether the address is 32 or 64 bits. 1: The address is 64 bits; 0: The address is 32 bits.
MaskBits10thru8	3	0b	Defines whether address bits[10:8] are masked ("masked" means bits[10:8] are don't care). 1: Masked 0: No mask
MaskBits11thru8	4	0b	Defines whether address bits [11:8] are masked. 1: Masked 0: No mask
MaskBits12thru8	5	0b	Defines whether address bits [12:8] are masked. 1: Masked 0: No mask
MaskBits13thru8	6	0b	Defines whether address bits [13:8] are masked. 1: Masked 0: No mask
TMKBC_BaseAddrLow	31:7	000000h	This register defines the lower 32 bit memory address used for the TMKBC function. There are actually four sets of such mapping. The selection is controlled by reg0x7C[6:5] (Tmkbc_sel). 00: set 0 01: set 1 10: set 2 11: set 3

TMKBC_BaseAddrHigh - RW - 32 bits - [PCI_Reg: 88h]			
Field Name	**Bits**	**Default**	**Description**
TMKBC_BaseAddrHigh	31:0	00000000h	This register defines the upper 32 bit memory address used for the TMKBC function. This register has no meaning if bit 2 of 84h is set to 0. There are actually four sets of such mapping. The selection is controlled by reg0x7C[6:5] (Tmkbc_sel). 00: set 0 01: set 1 10: set 2 11: set 3

TMKBC_Remap - RW - 16 bits - [PCI_Reg: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
TMKBC_Remap	15:8	00h	This register defines the remap address [15:8] on the LPC bus. There are actually four sets of such mapping. The selection is controlled by reg0x7C[6:5] (Tmkbc_sel). 00: set 0 01: set 1 10: set 2 11: set 3
Reserved	7:0	0h	

Wide IO 2 - RW - 16 bits - [PCI_Reg: 90h]			
Field Name	**Bits**	**Default**	**Description**
IO Base Address 2	15:0	0000h	16-bit PCI I/O base address for wide generic port range. 512 byte wide range. This function is enabled by reg0x4B[1] (Wide_io2_enable).

IMC_LPC_Cntrl - RW - 16 bits - [PCI_Reg: 98h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:9	0h	
IMCHoldLpc	8	0b	When set, IMC will hold the LPC bridge (i.e., host cannot access LPC)
Reserved	7:1	0h	
HostHoldLpc	0	0b	When set, host will hold the LPC bridge (i.e., it will prevent IMC from accessing the LPC bridge)

Gec_ShadowRom_Address - RW - 16 bits - [PCI_Reg: 9Ch]			
Field Name	**Bits**	**Default**	**Description**
Gec_ShadowRomAddr	31:10	00000h	This is the base address to the GEC shadow ROM (2K alignment)
Gec_portActive	0	-	Indicates whether shadowRom is active. 1: Active 0: Not active

SPI Base_Addr - RW - 16 bits - [PCI_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved.
SpiRomEnable	1	1b	When this bit is set and chip is strapped to SPI Rom, SPI Rom is enabled, otherwise SPI Rom is disabled.
Reserved	2	0b	Reserved.
Reserved	4:3	00b	Reserved.
SPI_BaseAddr	31:5	0000000h	This register defines the base address for the SPI ROM controller.

IMC_PortAddress - RW - 16 bits - [PCI_Reg: A4h]			
Field Name	**Bits**	**Default**	**Description**
IMC_PortActive	0	1b	When set to 1, LPC can decode the address specified in IMC_PortAddress; otherwise, LPC ignores it.
IMC_Addr15_1	15:1	0017h	When Addr15_1 is non-zero, and if an I/O cycle from host has address[15:1] = Addr15_1, the cycle will be routed to IMC instead of to LPC bus. By default, address[15:0] = 002Eh or 002Fh will be routed. Read-only to host if reg0xBA[3] (IMC_PortHostAccessEn) = 0.

RomDmaSrcAddr - RW - 16 bits - [PCI_Reg: B0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	0	
DmaStartAddr	31:6	00000000h	This register defines the starting DMA address to read from the ROM. Note this is not the same as the legacy DMA function. This is meant to be used by BIOS to fetch BOOT codes quicker.

RomDmadstAddr - RW - 16 bits - [PCI_Reg: B4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	5:0	0	
DmaDstAddr	31:6	00000000h	This register defines the target DMA address to be written in the system memory. Note this is not the same as the legacy DMA function. This is meant to be used by BIOS to fetch BOOT codes quicker.

RomDmaControl - RW - 16 bits - [PCI_Reg: B8h]			
Field Name	**Bits**	**Default**	**Description**
DmaStart	0	0b	Setting this bit will cause LPC bridge to start the DMA function, with starting addresses defined by reg0xB0 and reg0xB4. This bit will return the status of the DMA transfer. A return value of 0 means DMA transfer is completed. A return value of 1 means DMA transfer is running. Software can read this bit but writing to it has no effect.
DmaErrorStatus	1	0b	Read only. 1: Previous transfer has error. 0: Previous transfer has completed successfully.
Reserved	5:2	0000h	.
DWCount	15:6	0000h	This register defines the number of cacheline (64 bytes) to be fetched from the ROM when DMA is used.

IMCControl - RW - 8 bits - [PCI_Reg: BAh]			
Field Name	**Bits**	**Default**	**Description**
IMC Page Protect	0	0b	Enable the protection of IMC page registers. 1: 0xregBC~C7 are only read/writeable by IMC. Host write to them has no effect. Host read from them returns 0. 0: 0xregBC~C7 are read/writeable by both IMC and Host. (note: registers C5h~C7h are reserved and not shown here)
PrefetchEnSPIFromIMC	2	0b	Set to 1 to enable prefetch a cacheline (64 bytes) when IMC reads code from the SPI rom.
IMC_PortHostAccessEn	3	0b	Set to 1 to allow Host to program IMC_PortAddress register
IMCReadOfSwitch	4	0b	1: Upper 16 bits of IMC read request address are specified in IMCRomRdOf. 0: Upper 16 bits of IMC read request address are specified by auto rom diction logic.
PrefetchMissEn	5	0b	Set to1 to force the on-going prefetch to stop if the address of the pending read is not within the prefetch range for IMC. Only available for silicon revision A12 and above.
PrefetchEnSel	6	0b	0: Prefetch only the address of the read request is on the 4 byte boundary. 1: Prefetch only the address of the read request is on the 8 byte boundary. Only available for silicon revision A12 and above.
Reserved	7	000b	(spare bits)

Note: This register is read/write by IMC, and read-only by Host.

HostControl- RW - 8 bits - [PCI_Reg: BBh]			
Field Name	**Bits**	**Default**	**Description**
PrefetchEnSPIFromHost	0	0b	Set to 1 to enable prefetch a cacheline (64 bytes) when Host reads code from SPI ROM
DisableLADPullUp	1	0b	0: enable LAD Pull-up when IMC or Gec is enabled, or the system is in S0 1: Disable LAD pull-up
DIsableLpcOnPwrGood	2	0b	1: LPC signals (LAD, LFRAME#) are driven to low when IMC or Gec are not enabled and PwrGood goes to low. 0: LPC signals (LAD, LFRAME#) are driven to low when IMC or Gec are not enabled and SLP_S3 goes to low.
SpiCsFixEn	3	0b	Set to 1 to fix SPI_CS# timing issue when running at 66M. Only available for silicon revision A12 and above.
Reserved	5:4	00b	
PrefetchMissEnHost	6	0b	Set to1 to force the on-going prefetch to stop if the address of the pending read is not within the prefetch range for Host.

HostControl- RW - 8 bits - [PCI_Reg: BBh]			
			Only available for silicon revision A12 and above.
Reserved	7	0b	(spare bits)

Note: This register is read/write by IMC and Host.

IMCRomWrOf - RW - 32 bits - [PCI_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
IMCRomWrOf	31:0	FFF2_0000h	Specify address of the IMC write request.

When reg0xBA[0] (IMC Page Protect) = 1, this register will return the variables as described above. When reg0xBA[0] (IMC Page Protect) = 0, this register will return all 0s.

IMCRomRdOf - RW - 32 bits - [PCI_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
IMCRomRdOf	31:0	FFF2_0000h	Specify upper address of the IMC read request.

When reg0xBA[0] (IMC Page Protect) = 1, this register will return the variables as described above. When reg0xBA[0] (IMC Page Protect) = 0, this register will return all 0s.

3.1.3 SPI ROM Controller Registers

Register Name	Offset Address
SPI_Cntrl0	00h
SPI_RestrictedCmd	04h
SPI_RestrictedCmd2	08h
SPI_Cntrl1 Register	0Ch
SPI_CmdValue0	10h
SPI_CmdValue1	14h
SPI_CmdValue2	18h
Reserved	1Ch
Alt_SPI_CS	1Dh

Software can communicate with the SPI ROM through the default memory or alternate program method.

Memory access to the BIOS ROM address space is automatically handled by the hardware. The SPI ROM controller will translate the memory address onto the SPI bus and access the SPI ROM data. Any other commands besides memory_read or memory_write to the SPI ROM will need to go through the alternate program method. In this method, software will need to program the OpCode, SpiAddress, TxByteCount, RxByteCount, put the data into the transmit FIFO, and then execute the command. The hardware will then communicate with the SPI ROM using these parameters. This alternate method basically allows software to issue any flash vendor specific commands such as ERASE and STATUS.

SPI_Cntrl0 Register- RW - 32 bits - [Spi_Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
SPI_OpCode	7:0	0	When software uses the alternate program method to communicate with the SPI ROM, this register contains the OPCODE.

SPI_Cntrl0 Register- RW - 32 bits - [Spi_Mem_Reg: 00h]			
			Only available for silicon revision A12 and above.
TxByteCount	11:8	0	Number of bytes to be sent to SPI ROM. Only available for silicon revision A12 and above.
RxByteCount	15:12	0	Number of bytes to be received from the SPI ROM. Only available for silicon revision A12 and above.
ExecuteOpCode	16	0	Write 1 to execute the transaction in the alternate program registers. Writing 0 has no effect. When the transaction is complete, this bit will return 0. If the command is an illegal command, the bit cannot be set and thereby cannot execute. Only available for silicon revision A12 and above.
Reserved	17	0	Reserved
fastReadEnable	18	00	Set to 1 to enable Fast Read protocol.
SpiArbEnable	19	0	If a MAC is sharing the ROM with the FCH, both chips will need to go through an arbitration process before either one can access the ROM. This bit enables the arbitration. If MAC is not sharing the SPI ROM, BIOS should set this bit to 0 to speed up the SPI ROM access.
FifoPtrClr	20	0 (WO)	A write of 1 to this bit will clear the internal FIFO pointer. Only available for silicon revision A12 and above.
FifoPtrInc	21	0 (WO)	A write of 1 to this bit will cause the internal FIFO pointer to be incremented by 1. Only available for silicon revision A12 and above.
SpiAccessMacRomEn	22	1	This is a clear-once protection bit; once set, software cannot access MAC's portion of the ROM space (lower 512KB). However, IMC can always read/write this bit. Only available for silicon revision A12 and above.
SpiHostAccessRomEn	23	1	This is a clear-once protection bit; once set, MAC cannot access BIOS ROM space (upper 512KB). However, IMC can always read/write this bit. Only available for silicon revision A12 and above.
ArbWaitCount	26:24	100	Under ROM sharing mode (with the MAC), this defines the amount of wait time this controller will assert HOLD# before it should access the SPI ROM. This time is to allow the MAC to sample HOLD#. Only available for silicon revision A12 and

SPI_Cntrl0 Register- RW - 32 bits - [Spi_Mem_Reg: 00h]			
			above.
SpiBridgeDisable	27	1	Setting this bit will disable the SPI bridge mode (FCH will act as a SPI-LPC bridge to the MAC).
SPIClkGate	28	0	Set to 1 to force the 7th spiclk to be removed when reading the last data.
Reserved	30:29	0	Reserved
SpiBusy	31	0	Read only. 0: SPI bus is idle 1: SPI bus is busy

SPI_RestrictedCmd Register - RW - 32 bits - [Spi_Mem_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
RestrictedCmd0	7:0	0	This defines a restricted command issued by the MAC which will be checked by the FCH. If the opcode issued by the MAC matches with this register and the address space is in the BIOS space, this controller will simply ignore the command for the case of bridge mode. For peer mode, the SPI controller will jam the entire interface as an attempt to stop that transaction. Note when either SpiAccessMacRomEn and/or SpiHostAccessRomEn bit are cleared, these registers become read-only and cannot be changed any more.
RestrictedCmd1	15:8	0	Same as RestrictedCmd0
RestrictedCmd2	23:16	0	Same as RestrictedCmd0
RestrictedCmd3	31:24	0	Same as RestrictedCmd0

SPI_RestrictedCmd2 Register - RW - 32 bits - [Spi_Mem_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
RestrictedCmd4	7:0	0	Same as RestrictedCmd0
RestrictedCmdWoAddr0	15:8	0	Same as RestrictedCmd0 except this command does not have address
RestrictedCmdWoAddr1	23:16	0	Same as RestrictedCmd0 except this command does not have address
RestrictedCmdWoAddr2	31:24	0	Same as RestrictedCmd0 except this command does not have address

SPI_Cntrl1 Register- RW - 32 bits - [Spi_Mem_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
SPIParameters	7:0	0	This is the TX/RX FIFO port which can take up to 8 bytes. To send data to SPI ROM, software writes data into this port. To retrieve data that are received from the SPI ROM, software reads from this port.
FifoPtr	10:8	000	This three bits show the internal pointer location.
TrackMacLockEn	11	0	When set, the controller will lock the SPI for the MAC when it has detected a command (from the MAC) matching the value defined in offset 10h or 11h. Conversely, it will unlock the bus when it has detected a command (from the MAC) matching the value defined in offset 12h or 13h.
NormSpeed	13:12	11	This defines the clock speed for the non-fast read command 00 – 66Mhz 01 – 33Mhz 10 – 22 Mhz 11 – 16.5Mhz
Reserved	15:14	01	

SPI_Cntrl1 Register- RW - 32 bits - [Spi_Mem_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
RestrictedCmdWoAddr1	23:16	0	Same as RestrictedCmd0 except this command does not have address.
RestrictedCmdWoAddr2	31:24	0	Same as RestrictedCmd0 except this command does not have address.

Note: When either SpiAccessMacRomEn and/or SpiHostAccessRomEn of offset 00h are cleared, the fields RestrictedCmdWoAddr1 and RestrictedCmdWoAddr2 become read only and cannot be changed any more.

SPI_CmdValue0 Register- RW - 32 bits - [Spi_Mem_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
MacLockCmd0	7:0	06h	This is used to compare against the opcode sent out by the MAC. If SPI_Cntrl1[11] is set, the controller will lock the SPI bus for the MAC. In other words, the MAC has the exclusive access to the ROM; access by the CPU will be delayed until this is unlocked. This is to allow the MAC to do certain sequence of operations without interruption.
MacLockCmd1	15:8	20h	Same as MacLockCmd0.
MacUnlockCmd0	23:16	04h	This is used to compare against the opcode sent out by the MAC. If SPI_Cntrl1[11] is set, the controller will unlock the SPI bus for the MAC. In other words, access by the CPU will be allowed again.
MacUnlockCmd1	31:24	04h	Same as MacUnlockCmd0

Note: When either SpiAccessMacRomEn and/or SpiHostAccessRomEn of offset 00h are cleared, all of the bits become read only and cannot be changed any more.

SPI_CmdValue1 Register- RW - 32 bits - [Spi_Mem_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
WREN	7:0	06h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the WREN (write enable) command from the MAC. In the bridge mode, FCH will need to decode commands from the MAC.
WRDI	15:8	04h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the WRDI (write disable) command from the MAC.
RDID	23:16	9Fh	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the RDID (read ID) command from the MAC.
RDSR	31:24	05h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the RDSR (read status register) command from the MAC.

Note: When either SpiAccessMacRomEn and/or SpiHostAccessRomEn of offset 00h are cleared, all of the bits become read only and cannot be changed any more.

SPI_CmdValue2 Register- RW - 32 bits - [Spi_Mem_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
Read	7:0	03h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the Read (Read byte) command from the MAC. In the bridge mode, FCH will need to decode commands from the MAC.
FRead	15:8	0Bh	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the FRead (fast read) command from the MAC.

SPI_CmdValue2 Register- RW - 32 bits - [Spi_Mem_Reg: 18h]			
Field Name	**Bits**	**Default**	**Description**
PAGEWR	23:16	0Ah	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the PAGEWR (page write) command from the MAC.
BYTEWR	31:24	02h	This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the BYTEWR (byte write) command from the MAC.

Note: When either SpiAccessMacRomEn and/or SpiHostAccessRomEn of offset 00h are cleared, all of the bits become read only and cannot be changed any more.

Reserved- RW - 8 bits - [Spi_Mem_Reg: 1Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	

Alt_SPI_CS Register- RW - 8 bits - [Spi_Mem_Reg: 1Dh]			
Field Name	**Bits**	**Default**	**Description**
AltSpiCsEn	1:0	00b	These two bits enable the alternate SPI_CS# 00 – select xSPI_CS# 01 – select xSPI_CS1# 10 – select xSPI_CS2# 10 – select xSPI_CS3#
Reserved	7:2	0h	

3.1.4 SMBUS Registers

Register Name	Offset Address
SMBusStatus	00h
SMBusSlaveStatus	01h
SMBusControl	02h
SMBusHostCmd	03h
SMBusAddress	04h
SMBusData0	05h
SMBusData1	06h
SMBusBlockData	07h
SMBusSlaveControl	08h
SMBusShadowCmd	09h
SMBusSlaveEvent	0A-0Bh
SlaveData	0C-0Dh
SMBusTiming	0Eh
I2CbusConfig	10h
I2CCommand	11h
I2CShadow1	12h
I2Cshadow2	13h

Note: The SMBus registers are located at the IO memory space base address defined by PMIO register 2Ch bits 15:5.

SMBusStatus - RW - 8 bits - [SMBUS:00h]			
Field Name	**Bits**	**Default**	Description
HostBusy	0	0b	This bit indicates the SMBus controller is in the process of completing a command. When this bit is set, software should not access any other SMBus registers. [Read-only]

SMBusStatus - RW - 8 bits - [SMBUS:00h]			
Field Name	**Bits**	**Default**	Description
SMBusInterrupt	1	0b	This bit is set by hardware to indicate the completion of the last host command. This bit can be cleared by writing a 1 to it.
DeviceErr	2	0b	This bit is set by hardware to indicate an error of one of the following: 1) illegal command field, 2) unclaimed cycle, 3) host device time-out. This bit can be cleared by writing a 1 to it.
BusCollision	3	0b	This bit is set by hardware to indicate an SMBus transaction collision; this bit can be cleared by writing a 1 to it.
Failed	4	0b	This bit is set by hardware to indicate a failed bus transaction, set when SMBusControl. Kill bit is set. This bit is cleared by writing a 1 to it.
Reserved	7:5	000b	Reserved

SMBusSlaveStatus - RW - 8 bits - [SMBUS:01h]			
Field Name	**Bits**	**Default**	Description
SlaveBusy	0	0b	This bit indicates the SMBus controller slave interface is in the process of receiving data. Software should not try to access any other SMBus register when this bit is set. [Read-only]
SlaveInit	1	0b	Writing a 1 to this bit will initialize the slave. It is unnecessary to write it back to 0. A read from it will always return a 0.
SlaveStatus	2	0b	This bit is set by hardware to indicate a slave cycle event match of the SMBus slave command and SMBus Slave Event match. This bit can be cleared by writing a 1 to it.
Shadow1Status	3	0b	This bit is set by hardware to indicate a slave cycle address match of the SMB_Shadow1 port. This bit can be cleared by writing a 1 to it.
Shadow2Status	4	0b	This bit is set by hardware to indicate a slave cycle address match of the SMB_Shadow2 port. This bit can be cleared by writing a 1 to it.
AlertStatus	5	0b	This bit is set by hardware to indicate an SMBALERT_ signal. This function is not supported. [Read-only]
Reserved	7:6	00b	Reserved

SMBusControl - RW - 8 bits - [SMBUS:02h]			
Field Name	**Bits**	**Default**	Description
InterruptEnable	0	0b	Enable the generation of interrupts on the completion of current host transaction.
Kill	1	0b	Stop the current host transaction in process.
SMBusProtocol	4:2	000b	000: Quick Read or Write 001: Byte Read or Write 010: Byte Data Read or Write 011: Word Data Read or Write 100: Reserved 101: Block Read or Write 110: Reserved 111: Reserved
Reserved	5	0b	Reserved
Start	6	0b	Writing a 1 in this field initiates SMBus controller host interface to execute the command programmed in the SMBusProtocol field.
Reserved	7	0b	Reserved

SMBusHostCmd - RW – 8 bits - [SMBUS:03h]			
Field Name	**Bits**	**Default**	Description
SMBusHostCmd	7:0	00h	This field contains the data transmitted in the command field of SMBus host transaction.

SMBusAddress - RW - 8 bits - [SMBUS:04h]			
Field Name	**Bits**	**Default**	Description
SMBusRdWr	0	0b	0:Execute a Write command 1: Execute a Read command
SMBusAddr	7:1	00h	This field contains the 7-bit address of the target slave device.

SMBusData0 - RW - 8 bits - [SMBUS:05h]			
Field Name	**Bits**	**Default**	Description
SMBusData0	7:0	00h	This register should be programmed with a value to be transmitted in the data 0 field of an SMBus host interface transaction. For Block Write commands, the count of the memory should be stored in this field. The value of this register is loaded into the block transfer count field. A valid value for block command count is between 1 and 32. For block reads, count received from SMBus device is stored here.

SMBusData1 - RW - 8 bits - [SMBUS:06h]			
Field Name	**Bits**	**Default**	Description
SMBusData1	7:0	00h	This register should be programmed with a value to be transmitted in the data 1 field of an SMBus host interface transaction.

SMBusBlockData - RW - 8 bits - [SMBUS:07h]			
Field Name	**Bits**	**Default**	Description
SMBusBlockData	7:0	00h	This register is used to transfer data into or out of the block data storage array.

SMBusSlaveControl - RW - 8 bits - [SMBUS:08h]			
Field Name	**Bits**	**Default**	Description
SlaveEnable	0	0b	Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the host controller slave port of 10h, a command field that matches the SMBus slave control register, and a match of corresponding enabled events.
SMBusShadow1En	1	0b	Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the SMBus Shadow 1 register.
SMBusShadow2En	2	0b	Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the SMBus Shadow 2 register.
SMBusAlertEnable	3	0b	Enable the generation of an interrupt or resume event on the assertion of AMBALERT_ signal. (This function is not supported). [Read-only]

SMBusSlaveControl - RW - 8 bits - [SMBUS:08h]			
Field Name	**Bits**	**Default**	Description
HostSemaphore	4	0b	Bits 4 and 6 are meant to be used as software semaphore between the host and embedded controller. When both host and IMC want to use the same resource, they can write to these semaphore bits first, followed by a read. If the read returns a 1 in the semaphore bit, it means it has established the semaphore first. Write 1 to set this bit. This bit can only be set when EcSemaphore is clear. Writing 0 has no effect. Reading returns the value of this bit
ClrHostSemaphore	5	0b	Write 1 to clear HostSemaphore bit. Writing 0 has no effect and reading always returns 0
EcSemaphore	6	0b	Write 1 to set this bit. This bit can only be set when HostSemaphore is clear. Writing 0 has no effect. Reading returns the value of this bit
ClrEcSemaphore	7	0b	Write 1 to clear EcSemaphore bit. Writing 0 has no effect and reading always returns 0

SMBusShadowCmd - RW - 8 bits - [SMBUS:09h]			
Field Name	**Bits**	**Default**	Description
SMBusShadowCmd	7:0	00h	This field contains the command value that was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow ports.

SMBusSlaveEvent - RW - 16 bits - [SMBUS:0A-0Bh]			
Field Name	**Bits**	**Default**	Description
SMBusSlaveEvent	15:0	0000h	This field contains data bits used to compare against incoming data to the SMBus Slave Data register. When a bit in this register is 1 and a corresponding bit in SMBus Slave register is set, then an interrupt or resume event is generated if the command value matches the value in the SMBus slave control register and the access was to SMBus host address 10h.

SlaveData - RW - 16 bits - [SMBUS:0C-0Dh]			
Field Name	**Bits**	**Default**	Description
SlaveData	15:0	0000h	This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

SMBusTiming - RW - 8 bits - [SMBUS:0Eh]			
Field Name	**Bits**	**Default**	Description
SMBusTiming	7:0	B0h	This register controls the frequency on the SMBUS. The formula to calculate the frequency is: **Frequency = 66Mhz/(SmBusTiming * 4)**

I2CbusConfig - RW - 8 bits – [SMBUS: 10h]			
Field Name	**Bits**	**Default**	Description
I2CbusInterrupt	0	0b	0 : SMI# 1 : IRQ
Reserved	3:1	000b	Reserved
I2CRevision	7:4	0000b	SMBus controller revision

I2CbusConfig register: Registers D2-D5 control the interface when this chip is the I2C slave.

I2CCommand - RW - 8 bits - [SMBUS: 11h]			
Field Name	**Bits**	**Default**	Description
I2Ccommand	7:0	00h	I2C Host Slave Command; this value specifies the command value to be matched for I2C master accesses to the I2Ccontroller host slave interface.

I2CShadow1- RW - 8 bits - [SMBUS: 12h]			
Field Name	**Bits**	**Default**	Description
Read/Write ShadowPort1	0	0b	Read/Write for Shadow Port 1 This bit must be programmed to 0 because I2C slave controller only responds to Word Write Transaction.
I2CslaveAddr1	7:1	00h	SMBus Slave Address for shadow port 1 This value specifies the address used to match against incoming I2C addresses for Shadow port 1.

I2Cshadow2- RW - 8 bits - [SMBUS: 13h]			
Field Name	**Bits**	**Default**	Description
Read/Write ShadowPort2	0	0b	Read/Write for Shadow Port 2 This bit must be programmed to 0 because I2C slave controller only responds to Word Write Transaction.
I2CslaveAddr2	7:1	00h	SMBus Slave Address for shadow port 2 This value specifies the address used to match against incoming I2C addresses for Shadow port 2.

3.1.5 ASF SMBus Host Interface Registers

The ASF SM bus host register block is resident in the IO space whose base is defined at PMIO 0x24.

Register Name	Offset Address
HostStatus	00h
HostControl	02h
HostCommand	03h
SlaveAddress	04h
Data0	05h
Data1	06h
Data	07h
PEC	08h
ListenAdr	09h
ASFStatus	0Ah
StatusMask0	0Bh
StatusMask1	0Ch
SlaveControl	0Dh
RemoteCtrlAdr	0Eh
DataReadPointer	10h
DataWritePointer	11h
SetDataReadpointer	12h

Register Name	Offset Address
DataBankSel	13h
Semaphore	14h
SlaveEn	15h
DelayMasterTimer	16h

HostStatus – R - 8 bits - [ASF_IO: 00h]			
Field Name	**Bits**	**Default**	**Description**
HostBusy	0	0b	0: SM bus Host is idle 1: SM bus Host is busy
INTR	1	0b	The bit is set by termination of a command and can be cleared by writing to 1.
DevError	2	0b	0: Slave device behave correctly 1: No ACK or Slave device responses incorrectly
BusCollision	3	0b	0: no bus collision 1: bus collision
PECError	4	0b	0: no CRC error 1: CRC error happens
Reserved	6:5	00b	Reserved
LastByte	7	0b	0: Last byte has not received 1: Last byte has received

HostControl – RW - 8 bits - [ASF_IO: 02h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
KillHost	1	0b	0: Enable SM master 1: Reset SM master
Protocol	4:2	000b	000: Quick 001: Byte 010: Byte Data 011: Word Data 100: Process call 101: Block 110: Block write-Block read-process call
PECAppend	5	0b	0: no PEC append 1: Automatic PEC append. ASF HC calculates CRC code and append to the tail of the data packets.
Start	6	0b	WO: 0: always read 0 on reads 1: Writing 1 to initiate the command
PECEnable	7	0b	0: PEC disable 1: PEC enable, enable CRC checking when ASF HC presents as SM master and SM slave.

HostCommand – RW - 8 bits - [ASF_IO: 03h]			
Field Name	**Bits**	**Default**	**Description**
HostCommand	7:0	00h	Command to be transmitted by master

SlaveAddress– RW - 8 bits - [ASF_IO: 04h]			
Field Name	**Bits**	**Default**	**Description**
RW	0	0b	0: Write 1: Read
Address	7:1	00h	Provide the SM address of Slave

Data0– RW - 8 bits - [ASF_IO: 05h]			
Field Name	**Bits**	**Default**	**Description**
Data0	7:0	00h	Contains count or DATA0 field of transaction

Data1– RW - 8 bits - [ASF_IO: 06h]			
Field Name	**Bits**	**Default**	**Description**
Data1	7:0	00h	Contains DATA1 field of transaction

DataIndex– RW - 8 bits - [ASF_IO: 07h]			
Field Name	**Bits**	**Default**	**Description**
DataIndex	7:0	00h	Index to 32 Data registers.

PEC– RW - 8 bits - [ASF_IO: 08h]			
Field Name	**Bits**	**Default**	**Description**
PEC	7:0	00h	PEC byte to be sent to slave.

ListenAdr– RW - 8 bits - [ASF_IO: 09h]			
Field Name	**Bits**	**Default**	**Description**
ListenAdrEn	0	0	1: Enable ListenMode when the slave address equals to ListenAdr[7:1] 0: Disable ListenMode when the slave address equals to ListenAdr[7:1]
ListenAdr	7:1	00h	.The slave address which ASF slave response as ListenMode.

ASFStatus– RW - 8 bits - [ASF_IO: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
SlaveBusy	7	0b	Indicate if ASF slave is receiving data
SlaveIntr	6	0b	ASF Slave interrupt Status. Can be cleared to 0 by writing 1.
Reserved	5:4	00b	Reserved
RemotePowerCycle	3	0b	1: Power cycle has been triggered by ASF. 0: No power cycle ASF event Can be cleared to 0 by writing 1.
RemotePowerUp	2	0b	1: Power up has been triggered by ASF. 0: No Power up ASF event Can be cleared to 0 by writing 1.
RemotePowerDown	1	0b	1: Power down has been triggered by ASF 0: no Power down ASF event Can be cleared to 0 by writing 1.
RemoteReset	0	0b	1: Reset has been triggered by ASF 0: no Reset cycle ASF event Can be cleared to 0 by writing 1.

StatusMask0– RW - 8 bits - [ASF_IO: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Temp0StatusEnable	0	0b	1: Report Temp0 status to ASF 0: No report
Temp1StatusEnable	1	0b	1: Report Temp1 status to ASF 0: No report
Temp2StatusEnable	2	0b	1: Report Temp2 status to ASF 0: No report
Temp3StatusEnable	3	0b	1: Report Temp3 status to ASF 0: No report
AMDSIStatusEnable	4	0b	1: Report AMDSI status to ASF 0: No report

StatusMask0– RW - 8 bits - [ASF_IO: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
FanSpeed0StatusEnable	5	0b	1: Report Fan0 Speed Status to ASF 0: No report
FanSpeed1StatusEnable	6	0b	1: Report Fan1 Speed Status to ASF 0: No report
FanSpeed2StatusEnable	7	0b	1: Report Fan2 Speed Status to ASF 0: No report

StatusMask1– RW - 8 bits - [ASF_IO: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
AnalogIo0StatusEnable	0	0b	1: Report AnalogIo0 status to ASF 0: No report
AnalogIo1StatusEnable	1	0b	1: Report AnalogIo1 status to ASF 0: No report
AnalogIo2StatusEnable	2	0b	1: Report AnalogIo2 status to ASF 0: No report
AnalogIo3StatusEnable	3	0b	1: Report AnalogIo3 status to ASF 0: No report
AnalogIo4StatusEnable	4	0b	1: Report AnalogIo4 status to ASF 0: No report
AnalogIo5StatusEnable	5	0b	1: Report AnalogIo5 status to ASF 0: No report
AnalogIo6StatusEnable	6	0b	1: Report AnalogIo6 status to ASF 0: No report
AnalogIo7StatusEnable	7	0b	1: Report AnalogIo7 status to ASF 0: No report

SlaveStatus- RW – 8 bits - [ASF_IO: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
SlavePECError	0	0b	RO 0: No PEC error 1: PEC error
SlaveBusCollision	1	0b	RO 0: No BusCollision 1: BusCollision happens
SlaveDevError	2	0b	RO 0: Expected response 1: Unexpected response
WrongSP	3	0b	RO 0: No SP error 1: No SP symbol is detected when bus turns to read
Reserved	7:4	0000b	

RemoteCtrlAdr– RW - 8 bits - [ASF_IO: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
RemoteCtrlAdr	7:1	00h	SM address of Remote Control device.

SensorAdr– RW - 8 bits - [ASF_IO: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	
SensorAdr	7:1	00h	SM address of Sensor.

DataReadPointer– R - 8 bits - [ASF_IO: 10h]			
Field Name	**Bits**	**Default**	**Description**
DataReadPointer	7:0	00h	Current read pointer to the value specified in this register

DataWritePointer– R - 8 bits - [ASF_IO: 11h]			
Field Name	**Bits**	**Default**	**Description**
DataWritePointer	7:0	00h	Show current write pointer to the value specified in this register

SetDataReadPointer– RW - 8 bits - [ASF_IO: 12h]			
Field Name	**Bits**	**Default**	**Description**
SetDataReadPointer	7:0	00h	Force the current write pointer to the value specified in this register

DataBankSel– RW - 8 bits - [ASF_IO: 13h]			
Field Name	**Bits**	**Default**	**Description**
DataBank	1:0	0	Bit 0: 0: Data Bank 0 is the latest touched data bank. 1: Data Bank 1 is the latest touched data bank. Bit 1: 0: Data Bank still has space. 1: Data Bank is now full.
DataBank0_Full	2	0	0: Data Bank 0 is free. 1: Data Bank 0 is full. Writing 1 clears status.
DataBank1_Full	3	0	0: Data Bank 1 is free. 1: Data Bank 1 is full. Writing 1 clears status.
SetReadRevDataBank	5:4	00	00: Select to read data from Data Bank 0. 01: Select to read data from Data Bank 1 10: Select to read data from Data Bank 1 11: Select to read data from Data Bank 1
Reserved	6	0	Reserved
SetReadHostDataBank	7	0	0: Select to read data from Data Bank 0 or Data Bank 1 as decided by SetReadRevDataBank bits. 1: Select to read data from Host Data Bank.

Semaphore - RW - 4 bits - [ASF_IO:14h]			
Field Name	**Bits**	**Default**	**Description**
HostSemaphore	0	0b	Bits [0] and [2] are meant to be used as software semaphore between the host and the IMC. When both host and IMC want to use the same resource, they can write to these semaphore bits first, then followed by a read. If the read returns a 1 in the semaphore bit, it means it has established the semaphore first. Write 1 to set this bit. This bit can only be set when EcSemaphore is clear. Writing 0 has no effect. Read returns the value of this bit
ClrHostSemaphore	1	0b	Write 1 to clear HostSemaphore bit. Write 0 has no effect and read always returns 0
EcSemaphore	2	0b	Write 1 to set this bit. This bit can only be set when HostSemaphore is clear. Writing 0 has no effect. Read returns the value of this bit
ClrEcSemaphore	3	0b	Write 1 to clear EcSemaphore bit. Writing 0 has no effect and read always returns 0

SlaveEn - RW - 8 bits - [ASF_IO: 15h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved
SlaveIntrListenEn	1	0b	Set to 1 to allow ASF slave to generate slave interrupt when the address of received packet is the same as the one specified in ListenAdr register [ASF_IO:09h].
IntruderAlertStsEn	2	0b	RW: 0: FanSpeed2Status is returned 1: IntruderAlertSts is returned
SuspendSlave	3	0b	RW Write 1 to Suspend (stop) ASF Slave state machine
KillSlave	4	0b	RW Write 1 to reset Slave ASF Slave state machine
LegacySensorEn	5	0b	RW 0: Disable Legacy Sensor 1: Enable Legacy Sensor
TmrOutEn	6	0b	RW 0: Disable timer out function 1: Enable timer out function
FairArbEn	7	0b	RW 0: Disable Fair arbiter logic 1: Enable Fair Arbiter logic, which forces ASF master to give up SMBus for a certain time, specified in register at offset 16h.

DelayMasterTimer – RW - 8 bits - [ASF_IO: 16h]			
Field Name	**Bits**	**Default**	**Description**
FairArbTimer	7:0	10h	Specify how long ASF master has to wait before submitting next packet. Wait time = the value * 2us.

3.1.6 WatchDogTimer Registers

WatchDogTimer base address is defined in PM_Reg 48h.

Register Name	Offset Address
WatchDogControl	00h
WatchDogCount	04h

WatchDogControl - RW - 32 bits - [WD_Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
WatchDogRunStopB	0	0b	This bit is used to control or indicate whether the watchdog is in the Running and Stopped states. 1: Watchdog is in the Running state 0: Watchdog is in the Stopped state If the watchdog is in the Stopped state and a 1 is written to bit [0], the watchdog moves to the Running state, but a count interval is not started until a 1 is written to bit [7]. If the watchdog is in the Running state, writing a 1 to bit 0 has no effect. The bit is only valid when the watchdog is enabled.

WatchDogControl - RW - 32 bits - [WD_Mem_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
WatchDogFired	1	0b	A value of "1" indicates that the watchdog timer has expired and caused the current restart. The bit is cleared by writing a "1" to bit 1 in the Watchdog Control register. Writing a "0" has no effect. The bit is cleared by a power cycle or by the operating system and it must remain cleared for any restart that is not caused by the watchdog timer firing. The bit is only valid when the watchdog is enabled.
WatchDogAction	2	0b	This bit determines the action to be taken when the watchdog timer expires. 0: System reset 1: System power off The bit is only valid when the watchdog is enabled.
WatchDogDisable	3	0b	This bit reflects the state of the watchdog timer hardware. 0: Enable 1: Disable
Reserved	6:4		
WatchDogTrigger (WO)	7	0b	Write only. Setting this bit triggers the watchdog to start a new count interval, counting down from the value that was last written to the Watchdog Count Register. This bit is always read as zero. Setting this bit has no effect if the watchdog is disabled or stopped.
Reserved	31:8		

WatchDogCount - RW - 32 bits - [WD_Mem_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
WatchDogCount	15:0	----	This defines the countdown time for the counter. The units are defined in the Units field in the Watchdog Resource Table (WDRT). The maximum value is defined in the Max Count field in the WDRT. Reading this register returns in the current counter value.
Reserved	31:16		

3.1.7 High Precision Event Timers (HPET)

High Precision Event Timer registers are accessed by memory-mapped IOs. The base address is defined in PMIO register offset 50h. The HPET MMIO base address is FED0_0000h by default. They can also be accessed partially through the AcpiMmio registers that range from "AcpiMMioAddr" + 0xC00 to "AcpiMMioAddr" + 0xCff. (The base address "AcpiMMioAddr" is defined in PM_reg x24, with the default base address at "FED8_0000.")

Register Name	Offset Address
ID	000h
Config	010h
Interrupt Status	020h
Main_Counter	0F0h
Tmr0_Conf_Cap	100h
Tmr0_Comp	108h
Tmr1_Conf_Cap	120h

Tmr1_Comp	128h
Tmr2_Conf_Cap	140h
Tmr2_Comp	148h

ID - R - 64 bits - [HPET_Reg: 000h]			
Field Name	**Bits**	**Default**	**Description**
RevID	7:0	10h	Revision ID.
Num_Tmr_Cap	12:8	02h	Three timers are supported.
Counter_Size_Cap	13	0b	Main counter is 32-bits wide (and cannot operate in 64-bit mode).
Reserved	14	0b	Reserved.
Legacy_Cap	15	1b	Legacy replacement interrupt is supported.
VendorID	31:16	4353h	AMD vendor ID.
Counter_Clk_Period	63:32	0429B17Eh	Specifies the clock period of each HPET timer tick. HPET main counter runs at 14.31818 MHz. The unit is femptoseconds (10 ^ -15 seconds).

Config - RW - 64 bits - [HPET_Reg: 010h]			
Field Name	**Bits**	**Default**	**Description**
TmrEn	0	0b	0: Pause main counter and disable all timer interrupts. 1: Allow main counter to run and allow timer interrupts if enabled.
LegacyEn	1	0b	If LegacyEn is set to 1b then Timer0 interrupt goes to IRQ0 of PIC controller, INT2 of IoAPIC. Timer1 interrupt goes to IRQ8 of PIC controller, INT8 of IoAPIC.
Reserved	63:2	0h	Reserved.

Interrupt Status - RW - 64 bits - [HPET_Reg: 020h]			
Field Name	**Bits**	**Default**	**Description**
Tmr0IntrSts	0	0b	0: Timer0 interrupt is not active. 1: Timer0 interrupt is active. Write 1 to clear if timer0 is set to level-triggered mode. When set to edge-triggered mode, software should ignore this bit and always write 0b to this bit.
Tmr1IntrSts	1	0b	0: Timer1 interrupt is not active. 1: Timer1 interrupt is active. Write 1 to clear if timer1 is set to level-triggered mode. When set to edge-triggered mode, software should ignore this bit and always write 0b to this bit.
Tmr2IntrSts	2	0b	0: Timer2 interrupt is not active. 1: Timer2 interrupt is active. Write 1 to clear if timer2 is set to level-triggered mode. When set to edge-triggered mode, software should ignore this bit and always write 0b to this bit.
Reserved	63:3	0h	Reserved.

Main_Counter – RW - 64 bits - [HPET_Reg: 0F0h]			
Field Name	**Bits**	**Default**	**Description**
MainCounter	31:0	0h	32-bit main counter, increment by 1 on every clock. Counter should be written to only when halted.

Main_Counter – RW - 64 bits - [HPET_Reg: 0F0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	63:32	0h	Reserved.

Tmr<N>_Conf_Cap - R - 64 bits - [HPET_Reg: 100h + <N>*020h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved.
TmrIntTyp	1	0b	Control timer interrupt polarity: 0: Edge triggered 1: Level triggered
TmrIntEn	2	0b	Set to 1 to enable timer interrupt.
TmrTyp	3	0b	Select the timer interrupt type: 0: Non-periodic 1: Periodic
TmrTypCap	4	1b	The timer supports periodic interrupt delivery mode. Read only.
TmrSizeCap	5	0b	The timer is 32-bits wide. Read only.
TmrSetPer	6	0b	Set to 1 to allow software to set the timer's accumulator if the timer is set to periodic mode. The bit is automatically cleared when 'Comparator' is written by software.
Reserved	7	0b	Reserved.
Tmr32ModeEn	8	0b	64-bit timer is not supported. Read only.
TmrIntRoute	13:9	00h	These 5 bits specify which INT entry of IoAPIC the timer is routed to when LegacyEn is not set.
TmrFsbEn	14	0b	Set to 1 to enable FSB (Front Side Bus) delivery of interrupt.
TmrFsbCap	15	1b	FSB delivery is supported. Read only.
Reserved	31:16	0h	Reserved.
TmrIntRouteCap	63:32	00C00000h	Indicates which INT entry of IoAPIC can be assigned to the timer interrupt. Read only.

Note: Hardware supports 3 timers, <N> is 0, 1 or 2.

Tmr<N>_Comp - RW - 64 bits - [HPET_Reg: 108h + <N>*020h]			
Field Name	**Bits**	**Default**	**Description**
Comparator	31:0	FFFFFFFFh	The timer 32-bit wide comparator. **In non-periodic mode:** 'Comparator' is writeable. **In periodic mode:** 'Comparator' can be modified after TmrSetPer is set to 1. 'Comparator' is periodically incremented by the value last written to this register. By default, value is incremented by 0xFFFFFFFF.
Reserved	63:32	0h	Reserved.

Note: Hardware supports 3 timers, <N> is 0, 1 or 2.

3.1.8 Real Time Clock (RTC)

For software compatibility, the RTC registers and RAM are accessed through IO ports 70h/71h and with the banks (Bank 0 and Bank 1) address selected, which are shown in the diagram below. Bank 0 is selected if DV0 = 0 (DV0 is the 5th bit of Register A) while Bank 1 is chosen if DV0 = 1. Although there are two banks defined, the first 64 bytes (00h – 3Fh) are identical in each bank and should return the same value. Note: when Bank 1 is selected, byte offsets 00h – 0Dh Time/Alarm/Control registers and byte offsets 0Eh – 3Fh User RAM are read-only.

There are extended RAM space, x80 ~ xFF, defined later and accessed in a different way. One way to access the extended RAM space from x80 ~ xFF is through the indirect access of Bank 1, offset 50h/53h, which is defined to be the ExtendedRAMAddressPort.

The other way to access the extended RAM is through IO port 72h/73h, which are defined as the address/data ports for the extended RAM space. These two ports do not use the Bank 0/Bank 1 scheme. Memory can be accessed directly using the 8-bit address port. Use of the two IO ports 72h/73h to access the RTC RAM is highly recommended.

Note: Some RTC RAM space can be protected from read/write if corresponding bits are set to 1 in RTCProtect register (PCI_Reg 6Ah).

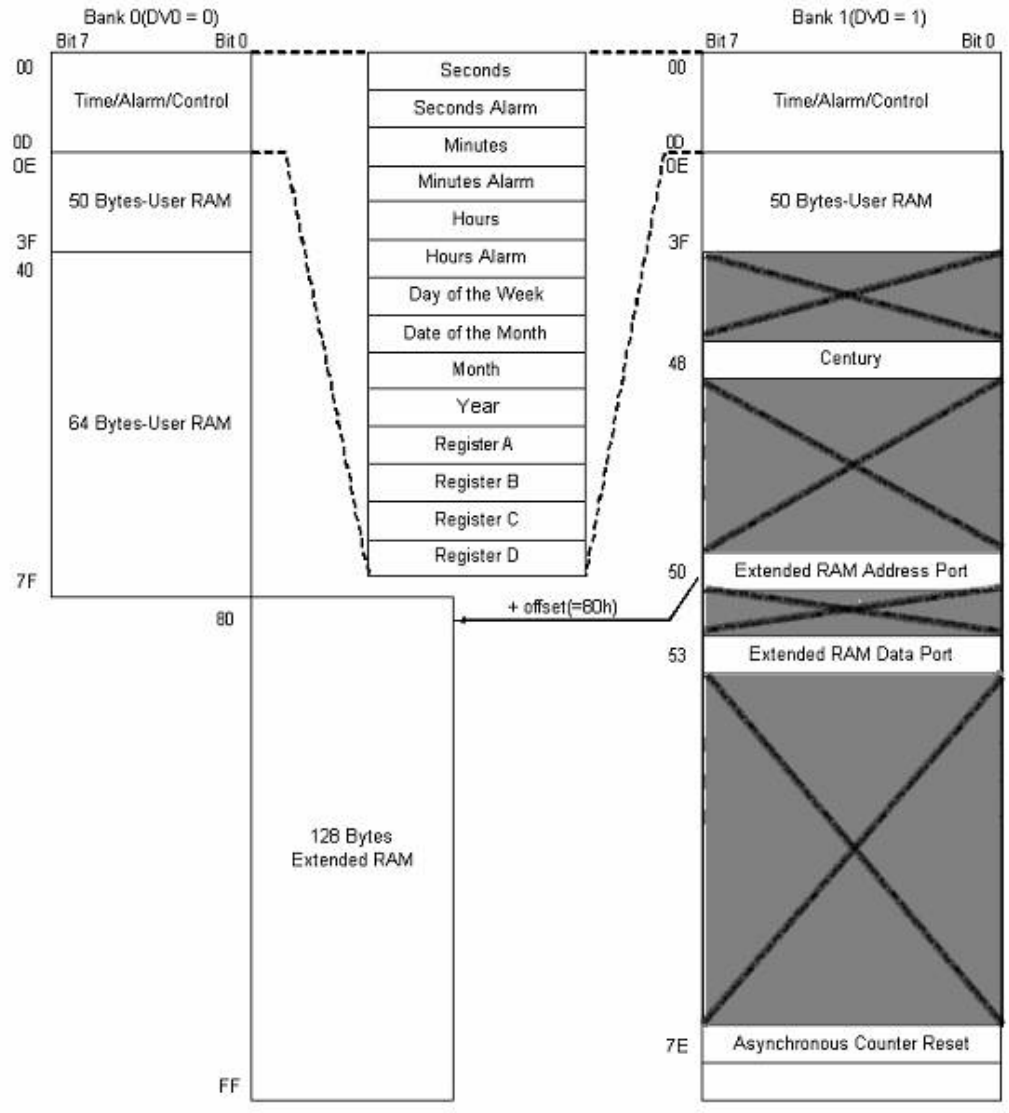

Figure 3: Register Bank Definition and Memory Address Mapping

The analog portion consists of two major parts: one is a 256-byte CMOS RAM and the other a 44-bit ripple counter.

Register Name	Offset Address
Seconds	00h
Seconds Alarm	01h
Minutes	02h
Minutes Alarm	03h
Hours	04h
Hours Alarm	05h
Day of Week	06h
Date of Month	07h
Month	08h
Year	09h
Register A	0Ah
Register B	0Bh
Register C	0Ch
Register D	0Dh
AltCentury (when DV0=0)	32h
Century (when DV0=1)	48h
Extended RAM Address Port	50h
Extended RAM Data Port	53h
RTC Time Clear	7Eh
RTC RAM Enable	7Fh

Note: Registers that are implemented in the internal RTC are described below.

Seconds - RW – 8 bits - [RTC_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Seconds	7:0	00h	Binary-Code-Decimal format. Range:00 – 59 This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every second. When set by software, hardware updating is disabled.

Seconds register

Seconds Alarm - RW – 8 bits - [RTC_Reg: 01h]			
Field Name	**Bits**	**Default**	**Description**
Seconds Alarm	7:0	00h	Binary-Code-Decimal format. If set bit = 1, the Seconds Alarm Register will never match with Seconds Register, else If bits [7:6] = [11], the Seconds Alarm Register always matches with Seconds Register.

Seconds Alarm register

Minutes - RW – 8 bits - [RTC_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Minutes	7:0	00h	Binary-Code-Decimal format. Range:00 – 59 This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every minute. When set by software, hardware updating is disabled.

Minutes register

Minutes Alarm - RW – 8 bits - [RTC_Reg: 03h]			
Field Name	**Bits**	**Default**	**Description**
Minutes Alarm	7:0	00h	Binary-Code-Decimal format. If set bit = 1, the Minutes Alarm Register will never match with Minutes Register, else If bits [7:6] = [11], the Minutes Alarm Register always matches with Minutes Register.

Minutes Alarm - RW – 8 bits - [RTC_Reg: 03h]			
Field Name	**Bits**	**Default**	**Description**

Minutes Alarm register

Hours - RW – 8 bits - [RTC_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Hours	7:0	00h	Binary-Code-Decimal format. Range:00 – 23 This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every hour. When set by software, hardware updating is disabled.

Hours register

Hours Alarm- RW – 8 bits - [RTC_Reg: 05h]			
Field Name	**Bits**	**Default**	**Description**
Hours Alarm	7:0	00h	Binary-Code-Decimal format. If set bit = 1, the Hours Alarm Register will never match with Hours Register, else If bits [7:6] = [11], the Hours Alarm Register always matches with Hours Register.

Hours Alarm register

Day of Week - RW – 8 bits - [RTC_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Day of Week	7:0	00h	Binary-Code-Decimal format. Range: 01 – 07 (Sunday = 1). No leap year correction capability. Leap year correction has to be done by software. This register can be set by a software (set bit of Register B = 1) or can be automatically updated by hardware everyday. When set by software, hardware updating is disabled.

Day of Week register

Date of Month - RW – 8 bits - [RTC_Reg: 07h]			
Field Name	**Bits**	**Default**	**Description**
Date of Month	7:0	00h	Binary-Code-Decimal format. Range: 01 – 28 for February and no leap year capability. Leap year correction has to be done by software. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware everyday. When set by software, hardware updating is disabled.

Date of Month register

Month - RW – 8 bits - [RTC_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Month	7:0	00h	Binary-Code-Decimal format. Range: 01 – 12. No leap year correction capability. Leap year correction has to be done by software. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every month. When set by software, hardware updating is disabled.

Month register

Year - RW – 8 bits - [RTC_Reg: 09h]			
Field Name	**Bits**	**Default**	**Description**
Year	7:0	00h	Binary-Code-Decimal format. Range: 00 – 99. No leap year correction capability. Leap year correction has to be done by software. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every year. When set by software, hardware updating is disabled.

Year register

Register A - RW – 8 bits - [RTC_Reg: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
Rate Selection(RS0)	0	0b	These four rate-selection bits select one of the 13 taps on the 15-stage frequency divider or disable the divider output (flat output signal). The tap selected can be used to generate a periodic interrupt. See the following table for the frequency selection.
Rate Selection(RS1)	1	0b	
Rate Selection(RS2)	2	0b	
Rate Selection(RS3)	3	0b	
Bank Selection(DV0)	4	0b	DV0 = 0 selects Bank 0; DV0 = 1 selects Bank 1. The Hudson-1 has an alternate way to access the RAM without the use of bank select bit. Port 72/73 can be used as the index to access the full 256 bytes of RAM directly.
Reserved	6:5		
Update In Progress(UIP)	7	0b	If set bit = 1, UIP is cleared. If UIP = 1, the update transfer will soon occur. If UIP = 0, the update transfer will not occur for at least 244us. [Read-only]

Register A: Control register

Rate Selection Bits				Tap Frequency(Interrupt Rate)
RS3	**RS2**	**RS1**	**RS0**	
0	0	0	0	Flat Signal(None)
0	0	0	1	256 Hz (3.90625 ms)
0	0	1	0	128 Hz (7.8125 ms)
0	0	1	1	8.192 kHz (122.070 us)
0	1	0	0	4.096 kHz (244.141 us)
0	1	0	1	2.048 kHz (488.281 us)
0	1	1	0	1.024 kHz (976.5625 us)
0	1	1	1	512 Hz (1.953125 ms)
1	0	0	0	256 Hz (3.90625 ms)
1	0	0	1	128 Hz (7.8125 ms)
1	0	1	0	64 Hz (15.625 ms)
1	0	1	1	32 Hz (31.25 ms)
1	1	0	0	16 Hz (62.5 ms)
1	1	0	1	8 Hz (125 ms)
1	1	1	0	4 Hz (250 ms)
1	1	1	1	2 Hz (500 ms)

Register B - RW – 8 bits - [RTC_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Daylight Saving Enable	0	0b	Both this bit and RtcExt_Reg: 00h bit[0] need to be set to 1 to enable RTC daylight saving feature.
HourMode	1	0b	Hour mode 0: 12 hour mode 1: 24 hour mode
Reserved	3:2	00	
Update Ended Interrupt Enable(UIE)	4	0b	UIE enables the Update End Flag (UF) bit in Register C to assert IRQ. If set bit = 1, UIE is cleared.

Register B - RW – 8 bits - [RTC_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Alarm Interrupt Enable (AIE)	5	0b	AIE enables the Alarm Flag (AF) bit in Register C to assert IRQ.
Periodic Interrupt Enable (PIE)	6	0b	PIE enables the Periodic Interrupt Flag (PF) bit in Register C to assert IRQ.
Set new time (SET)	7	0b	If set bit = 1, no internal updating for Time Registers is allowed. If set bit = 0, the Time Registers are updated every second.

Register B: Control register

Register C - R – 8 bits - [RTC_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	
Update Ended Interrupt Flag(UF)	4	0b	This bit is set to one after each update cycle. Reading Register C clears UF.
Alarm Interrupt Flag (AF)	5	0b	This bit is set to one if second, minute and hour time has matched the second, minute and hour alarm time. Reading Register C clears AF bit.
Periodic Interrupt Flag (PF)	6	0b	This bit is set to one when an edge is detected on the selected tap (through RS3 to RS0) of the frequency divider. Reading Register C clears PF bit.
Interrupt Request Flag (IRQF)	7	0b	Logically, IRQF = (PF*PIE)+(AF*AIE)+(UF*UIE)+(WF*WIE) where WF and WIE are defined in Extended Control Register 4A and 4B. Reading Register C clears IRQF bit. Any time the IRQF bit is set to one, the #IRQ pin is driven low.

Register C: Control register

DateAlarm - RW – 8 bits - [RTC_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
DateAlarm	5:0	00h	DateAlarm in BCD format and is considered when it is set to non-zero value. If this value is set to 0, then date is not compared for alarm generation.
Scratchbit	6	0b	
VRT	7	1b	Valid RAM and Time; refer to VRT_T1 and VRT_T2 registers (PMIO 3E/3F)

Date Alarm Register

AltCentury - RW – 8 bits - [RTC_Reg: 32h]			
Field Name	**Bits**	**Default**	**Description**
AltCentury	7:0	00h	(This register is accessed only when DV0=0 and PM_Reg 7Ch Bit4=1.) Binary-Code-Decimal format. Leap year correction is done through hardware. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every century. When set by software, hardware updating is disabled.

AltCentury Register

Century - RW – 8 bits - [RTC_Reg: 48h]			
Field Name	**Bits**	**Default**	**Description**
Century	7:0	00h	(This register is accessed only when DV0=1) Binary-Code-Decimal format. Leap year correction is done through hardware. This register can be set by software (set bit of Register B = 1) or can be automatically updated by hardware every century. When set by software, hardware updating is disabled.

Century Register

Extended RAM Address Port - RW – 8 bits - [RTC_Reg: 50h]			
Field Name	**Bits**	**Default**	**Description**
ExtendedRAMAddr	6:0	00h	Because only 7 address bits are used in port x70, only lower 128 bytes are accessible through port x71. The Extended RAM (upper 128 bytes) are physically located at address 80H to FFH. In order to access these address, an address offset should be programmed into this register and access them through Extended RAMDataPort. (An offset of x80H will automatically add to this 7-bit address).
Reserved	7		

Extended RAM Address Port register: The address port to access Extended RAM.

Extended RAM Data Port - RW – 8 bits - [RTC_Reg: 53h]			
Field Name	**Bits**	**Default**	**Description**
Extended RAM Data Port	7:0	xxxxxxxx	There is no physical register corresponding to this data port but the data port address is used for decoding to generate appropriate internal control signals.

Extended RAM Data Port register.

RTC Time Clear - RW – 8 bits - [RTC_Reg: 7Eh]			
Field Name	**Bits**	**Default**	**Description**
RtcTimeClear	0	0b	Setting this bit will clear the RTC second and RTC time will stop
Reserved	7:1	0000000b	

RTC Time Clear register.

RTC RAM Enable - RW – 8 bits - [RTC_Reg: 7Fh]			
Field Name	**Bits**	**Default**	**Description**
RtcRamEnable	0	1b	Setting this bit will enable access to the RTC RAM
Reserved	7:1	0000000b	
RTC RAM Enable register.			

3.1.9 RTC Extended Registers

The RTC extended register block is accessed through PM_Reg: 5E/5F Index/Data port.

Register Name	Offset Address
DltSavEnable	00h
SprFwdCtrl	01h
SprFwdMonth	02h
FallBackCtrl	03h
FallBackMonth	04h

DltSavEnable – RW – 8 bits – [RtcExt_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
DltSavEnable	0	0b	Set to 1 to enable RTC daylight saving feature.
Reserved	7:6		
DltSavEnable register			

SprFwdCtrl – RW – 8 bits – [RtcExt_Reg: 01h]			
Field Name	**Bits**	**Default**	**Description**
SprFwdHour	5:0	00h	This BCD value determines which hour (24 hour mode) to do the “spring forward”. Setting of 02h means 2am. Default is 00h which also denotes 2am. Spring forward is usually 2am in United States and 1am in Europe.
SprFwdWeek	6	0b	This value determines which Sunday morning to do the “spring forward”. Default is 0 which denotes the 1st week. Setting of 1 means the last week of the month. Spring forward is usually at the 1st Sunday of April in United States and last Sunday of March in Europe.
Reserved	7		
SprFwdCtrl register			

SprFwdMonth – RW – 8 bits – [RtcExt_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
SprFwdMonth	4:0	00h	This BCD value determines which month to “spring forward”. Setting of 04h means April. Default is 00h, which also denotes April. Spring forward is usually at April in United States and March in Europe.
Reserved	7:5		
SprFwdMonth register			

FallBackCtrl – RW – 8 bits – [RtcExt_Reg: 03h]			
Field Name	**Bits**	**Default**	**Description**
FallBackHour	5:0	00h	This BCD value determines which hour (24 hour mode) to do the “fall back”. Setting of 02h means 2am. Default is 00h which also denotes 2am. Fall back is usually 2am in United States and 1am in Europe.
FallBackWeek	6	0b	This value determines which Sunday morning to do the “fall back”. Default is 0 which denotes the last week. Setting of 1 means the first week of the month. Fall back is usually at the last Sunday of October in both United States and Europe.
Reserved	7		
FallBackCtrl register			

FallBackMonth – RW – 8 bits – [RtcExt_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
FallBackMonth	4:0	00h	This BCD value determines which month to “fall back”. Setting of 10h means October. Default is 00h which also denotes October. Fall back is usually at October in both United States and Europe.
Reserved	7:5		
FallBackMonth register			

Week Timer registers

The 16-bit Week Timer is a battery powered down counter timer that supports 1ms, 1 second and 1minute resolution and auto reloads when the timer reaches 0. The WEEK_ALRM interrupt is asserted when the timer reaches 0 and stays asserted until the timer is disabled. The Week Timer registers are located in RTC extended register block index

10h through 14h.

WeekTimerControl – RW – 8 bits – [RtcExt_Reg: 10h]			
Field Name	**Bits**	**Default**	**Description**
Enable	0	0b	This bit is used to start and stop the Week Timer. 0: Disable 1: Enable
Resolution	2:1	00b	These bits are used to control the resolution of the Week Timer counter. 00: 1 minute 01: 1 second 10: 1ms 11: Reserved
Reserved	7:3		

WeekTimerControl register
Note: The Enable should be cleared when changing the Resolution setting.

WeekTimerReloadLow – RW – 8 bits – [RtcExt_Reg: 11h]			
Field Name	**Bits**	**Default**	**Description**
WeekTimerReloadLow	7:0		This register is used to program the lower 8 bits of the 16-bit WeekTimerReload register. Writing the WeekTimerReloadLow register causes the 16-bit WeekTimerReload to be written into the Week Timer.

WeekTimerReloadLow register
Note: The Enable in the WeekTimerControl register should be cleared before performing a write access to the WeekTimerReloadLow or WeekTimerReload High register.

WeekTimerReloadHigh – RW – 8 bits – [RtcExt_Reg: 12h]			
Field Name	**Bits**	**Default**	**Description**
WeekTimerReloadHigh	7:0		This register is used to program the upper 8 bits of the 16-bit WeekTimerReload register. This register should be programmed before writing the WeekTimerReloadLow register.

WeekTimerReloadHigh register
Note: The Enable in the WeekTimerControl register should be cleared before performing a write access to the WeekTimerReloadLow or WeekTimerReload High register.

WeekTimerDataLow – R – 8 bits – [RtcExt_Reg: 13h]			
Field Name	**Bits**	**Default**	**Description**
WeekTimerDataLow	7:0		This register is used to read the current state of the 16-bit Week Timer. Reading from the WeekTimerDataLow register returns the lower 8 bits of the 16-bit Week Timer and cause the upper 8 bits to be latched into the WeekTimerDataHigh register.

WeekTimerDataLow register
Note: Two reads are required to read the current state of the 16-bit Week Timer: the first read from the WeekTimerDataLow register returns the lower 8 bits of the 16-bit Week Timer and the second read from the WeekTimerDataHigh register return the upper 8 bits of the 16-bit Week Timer.

WeekTimerDataHigh – R – 8 bits – [RtcExt_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
WeekTimerDataHigh	7:0		This register is used to read the current state of the 16-bit Week Timer. Reading from the WeekTimerDataHigh register returns the upper 8 bits of the 16-bit Week Timer latched by a previous read from the WeekTimerDataLow register.

WeekTimerDataHigh – R – 8 bits – [RtcExt_Reg: 14h]			
Field Name	**Bits**	**Default**	**Description**
WeekTimerDataLow register **Note:** Two reads are required to read the current state of the 16-bit Week Timer: the first read from the WeekTimerDataLow register returns the lower 8 bits of the 16-bit Week Timer and the second read from the WeekTimerDataHigh register return the upper 8 bits of the 16-bit Week Timer.			

3.1.10 Legacy Block Registers

The following legacy blocks are in the IO-mapped address space. These registers control the legacy functions such as DMA, timers, PIC, interrupt routing for PIC, RTC, and the Hudson-1 specific control registers.

3.1.10.1 IO-Mapped Control Registers

Register Name	IO Address
Dma_Ch 0	00h
Dma_Ch 1	02h
Dma_Ch 2	04h
Dma_Ch 3	06h
Dma_Status	08h
Dma_WriteRequest	09h
Dma_WriteMask	0Ah
Dma_WriteMode	0Bh
Dma_Clear	0Ch
Dma_MasterClr	0Dh
Dma_ClrMask	0Eh
Dma_AllMask	0Fh
IntrCntrlReg1	20h
IntrCntrlReg2	21h
TimerCh0	40h
TimerCh1	41h
TimerCh2	42h
Tmr1CntrlWord	43h
Nmi_Status	61h
Nmi_Enable	70h
RtcDataPort	71h
AlternatRtcAddrPort	72h
AlternatRtcDataPort	73h
Dma_PageCh2	81h
Dma_PageCh3	82h
Dma_PageCh1	83h
Dma_Page_Reserved1	84h
Dma_Page_Reserved2	85h
Dma_Page_Reserved3	86h
Dma_PageCh0	87h
Dma_Page_Reserved4	88h
Dma_PageCh6	89h
Dma_PageCh7	8Ah
Dma_PageCh5	8Bh
Dma_Page_Reserved5	8Ch
Dma_Page_Reserved6	8Dh
Dma_Page_Reserved7	8Eh
Dma_Refresh	8Fh

Register Name	IO Address
FastInit	92h
IntrCntrl2Reg1	A0h
IntrCntrl2Reg2	A1h
Dma2_Ch4Addr	C0h
Dma2_Ch4Cnt	C2h
Dma2_Ch5Addr	C4h
Dma2_Ch5Cnt	C6h
Dma2_Ch6Addr	C8h
Dma2_Ch6Cnt	CAh
Dma2_Ch7Addr	CCh
Dma2_Ch7Cnt	CEh
Dma_Status	D0h
Dma_WriteRequest	D2h
Dma_WriteMask	D4h
Dma_WriteMode	D6h
Dma_Clear	D8h
Dma_Clear	DAh
Dma_ClrMask	DCh
Dma_ClrMask	DEh
NCP_Error	F0h
DMA1_Extend	40Bh
IntrEdgeControl	4D0h
DMA2_Extend	4D6h
Pci_Intr_Index	C00h
Pci_Intr_Data	C01h
Pci_Error	C14h
CMIndex	C50h
CMData	C51h
GpmPort	C52h
Isa_Misc	C6Fh
PM2_Index	CD0h
PM2_Data	CD1h
BIOSRAM_Index	CD4h
BIOSRAM_Data	CD5h
PM_Index	CD6h
PM_Data	CD7h

Note: The PCI I/O registers are 32-bit registers decoded from the full 32-bit PCI address and C/BE[3:0]#. Therefore, the bytes within a 32-bit address are selected with the valid byte enables. Registers and bits within a register marked as reserved are not implemented. Writes have no effect on reserved registers. All PCI I/O registers can be accessed via 8, 16, or 32-bit cycles (i.e., each byte is individually selected by the byte enables).

Dma_Ch 0- RW – 16 bits - [IO_Reg: 00h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Ch 0	15:0	0000h	DMA1 Ch0 Base and Current Address
Dma_Ch 0 register			

Dma_Ch 1- RW – 16 bits - [IO_Reg: 02h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Ch 1	15:0	0000h	DMA1 Ch1 Base and Current Address
Dma_Ch 1 register			

Dma_Ch 2- RW – 16 bits - [IO_Reg: 04h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Ch 2	15:0	0000h	DMA2 Ch2 Base and Current Address
Dma_Ch 2 register			

Dma_Ch 3- RW – 16 bits - [IO_Reg: 06h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Ch 3	15:0	0000h	DMA1 Ch3 Base and Current Address
Dma_Ch 3 register			

Dma_Status- RW – 8 bits - [IO_Reg: 08h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Status	7:0	00h	Returns status when read; command for write
Dma_Status register			

Dma_WriteRequest- RW – 8 bits - [IO_Reg: 09h]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteRequest	7:0	00h	Request register.
Dma_WriteRequest register			

Dma_WriteMask- RW – 8 bits - [IO_Reg: 0Ah]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteMask	7:0	00h	Channel mask register.
Dma_WriteMask register			

Dma_WriteMode- RW – 8 bits - [IO_Reg: 0Bh]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteMode	7:0	00h	Mode register.
Dma_WriteMode register			

Dma_Clear- RW – 8 bits - [IO_Reg: 0Ch]			
Field Name	**Bits**	**Default**	**Description**
Dma_Clear	7:0	00h	Channel 0-3 DMA clear byte pointer
Dma_Clear register			

Dma_MasterClr- RW – 8 bits - [IO_Reg: 0Dh]			
Field Name	**Bits**	**Default**	**Description**
Dma_MasterClr	7:0	00h	Intermediate register.
Dma_MasterClr register			

Dma_ClrMask- RW – 8 bits - [IO_Reg: 0Eh]			
Field Name	**Bits**	**Default**	**Description**
Dma_ClrMask	7:0	00h	Channel 0-3 DMA Clear Mask
Dma_ClrMask register			

Dma_AllMask- RW – 8 bits - [IO_Reg: 0Fh]			
Field Name	**Bits**	**Default**	**Description**
Dma_AllMask	7:0	00h	Mask register.
Dma_AllMask register			

IntrCntrl1Reg1- RW – 8 bits - [IO_Reg: 20h]			
Field Name	**Bits**	**Default**	**Description**
IntrCntrl1Reg1	7:0	00h	IRQ0 – IRQ7: Read IRR, ISR Write ICW1, OCW2, OCW3

IntrCntrl1Reg1register

IntrCntrl1Reg2- RW – 8 bits - [IO_Reg: 21h]			
Field Name	**Bits**	**Default**	**Description**
IntrCntrl1Reg2	7:0	00h	IRQ0 – IRQ7: Read IMR Write ICW2, ICW3, ICW4, OCW1

IntrCntrl1Reg2 register

IMCR_Index- RW – 8 bits - [IO_Reg: 22h]			
Field Name	**Bits**	**Default**	**Description**
IMCR_Index	7:0	00h	The IMCR is supported by two read/writeable IO ports 22/23h; which are used as index and data port respectively. The actual IMCR register is located at index 70h.

IMCR_Index register

IMCR_Data- RW – 8 bits - [IO_Reg: 23h]			
Field Name	**Bits**	**Default**	**Description**
IMCR_Data	7:0	00h	The IMCR is supported by two read/writeable IO ports 22/23h; which are used as index and data port respectively. The actual IMCR register is located at index 70h and it is at bit 0. The actual IMCR bit can only be accessed when bit port 22 is set to 70h. Default value of IMCR is 0.

IMCR_Data register

TimerCh0- RW – 8 bits - [IO_Reg: 40h]			
Field Name	**Bits**	**Default**	**Description**
TimerCh0	7:0	00h	8254 Timer 1: Counter 0 Data Port This timer is known as the System Clock timer and it is always on. It is clocked internally by OSC/12 (1.19318MHz), and asserts IRQ0 every time the timer rolls over. This timer is used for time-of-day, diskette time-out, and other system timing functions.

TimerCh0 register

TimerCh1- RW – 8 bits - [IO_Reg: 41h]			
Field Name	**Bits**	**Default**	**Description**
TimerCh1	7:0	00h	8254 Timer 1: Counter 1 Data Port This timer is normally used for ISA refresh cycles and is also clocked by OSC/12 (1.19818MHz). Since this refresh function is no longer needed (we don't have an external ISA bus), it can be used as a general purpose timing function.

TimerCh1 register

TimerCh2- RW – 8 bits - [IO_Reg: 42h]			
Field Name	**Bits**	**Default**	**Description**
TimerCh2	7:0	00h	8254 Timer 1: Counter 2 Data Port This is the speaker tone generator and is enabled by IO port 61H. It is clocked by OSC/12 (1.19318MHz) and directly drives the output SPKR that goes to a speaker.

TimerCh2 register

Tmr1CntrlWord - RW – 8 bits - [IO_Reg: 43h]			
Field Name	**Bits**	**Default**	**Description**
CntDownSelect	0	0b	0: Binary countdown 1: BCD countdown
ModeSelect	3:1	000b	000: Asserts OUT signal at end of count 001: Hardware re-triggerable one-shot 010: Rate generator 011: Square wave output 100: Software triggered strobe 101: Hardware triggered strobe 110 – 111: Not used
CmmandSelect	5:4	00b	00: Counter latch command 01: Read/write least significant byte 10: Read/write most significant byte 11: Read/write least, and then most significant byte
CounterSelect	7:6	00b	00: Select counter 0 01: Select counter 1 10: Select counter 2 11: Read back command

Tmr1CntrlWord register: This is the control word to access the 8254 timer 1. It is used to select which counter will be accessed and how it will be accessed. This register specifies the counter, the operating mode, the order and size of the count value, and whether it counts down in a 16 bit or BCD format.
If a counter is programmed to read or write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter; otherwise, the counter will be loaded with an incorrect value. The count must always be completely loaded with both bytes.

Nmi_Status - RW – 8 bits - [IO_Reg: 61h]			
Field Name	**Bits**	**Default**	**Description**
SpkrEnable	0	0b	0: Disable counter 2 1: Enable counter 2
SpkrTmrEnable	1	0b	0: Speaker timer off 1: Speaker timer on
Parity_Nmi_En	2	1b	0: Enable Parity Error to NMI generation (from SERR# or PERR#) 1: Disable Parity Error to NMI generation and clear bit 7
Iochk_Nmi_En	3	1b	0: Enable IoChk to NMI generation 1: Disable IoChk to NMI generation
RefClk	4	-	The output of the counter 1 (8254). [Read-only]
SpkrClk	5	-	The output of the counter 2. [Read-only]
IoChk_Nmi	6	-	NMI is triggered by serial IOCHK. [Read-only]
ParErr_Nmi	7	-	NMI is caused by parity error (either PERR# or SERR#). [Read-only]

Nmi_Status register: Independent read and write registers will be accessed at this port. When writing to port 61H, bits[3:0] allow software to enable/disable parity error NMI's and control the speaker timer. When reading port 61H, status on parity errors, speaker count, speaker control and refresh cycles is returned.

Nmi_Enable - RW – 8 bits - [IO_Reg: 70h]			
Field Name	**Bits**	**Default**	**Description**
RTC Address Port	6:0	00h	This is used with either internal RTC or external RTC
NmiEnable	7	0b	0: NMI enable 1: NMI disable [Write-only]

Nmi_Enable register

RtcDataPort - RW – 8 bits - [IO_Reg: 71h]			
Field Name	**Bits**	**Default**	**Description**
RTC Data Port	7:0	00h	This is used with either internal RTC or external RTC
RtcDataPort			

AlternatRtcAddrPort - RW – 8 bits - [IO_Reg: 72h]			
Field Name	**Bits**	**Default**	**Description**
AlternatRTCAddrPort	7:0	00h	This is used with internal RTC. This port allows user to specify the full 8 bit address (instead of bank0/bank1 indexing) to access the 256 byte RTC RAM

AlternatRtcAddrPort

AlternatRtcDataPort - RW – 8 bits - [IO_Reg: 73h]			
Field Name	**Bits**	**Default**	**Description**
AlternatRTC Data Port	7:0	00h	This is used with internal RTC in conjunction with port h72

AlternatRtcDataPort

Dma_PageCh2 - RW – 8 bits - [IO_Reg: 81h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh2	7:0	00h	DMA2 ch 2 page register

Dma_PageCh2 register

Dma_PageCh3 - RW – 8 bits - [IO_Reg: 82h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh3	7:0	00h	DMA2 ch 3 page register

Dma_PageCh3 register

Dma_PageCh1 - RW – 8 bits - [IO_Reg: 83h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh1	7:0	00h	DMA2 ch 1 page register

Dma_PageCh1 register

Dma_Page_Reserved1- RW – 8 bits - [IO_Reg: 84h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved1	7:0	00h	DMA Page Reserved1 register

Dma_Page_Reserved1 register

Dma_Page_Reserved2- RW – 8 bits - [IO_Reg: 85h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved2	7:0	00h	DMA Page Reserved2 register
Dma_Page_Reserved2 register			

Dma_Page_Reserved3- RW – 8 bits - [IO_Reg: 86h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved3	7:0	00h	DMA Page Reserved3 register

Dma_Page_Reserved3 register

Dma_PageCh0 - RW – 8 bits - [IO_Reg: 87h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh0	7:0	00h	DMA2 ch 0 page register

Dma_PageCh0 register

Dma_Page_Reserved4- RW – 8 bits - [IO_Reg: 88h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved4	7:0	00h	Dma Page Reserved4 register

Dma_Page_Reserved4 register

Dma_PageCh6 - RW – 8 bits - [IO_Reg: 89h]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh6	7:0	00h	DMA2 ch 6 page register

Dma_PageCh6 register

Dma_PageCh7 - RW – 8 bits - [IO_Reg: 8Ah]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh7	7:0	00h	DMA2 ch 7 page register

Dma_PageCh7 register

Dma_PageCh5 - RW – 8 bits - [IO_Reg: 8Bh]			
Field Name	**Bits**	**Default**	**Description**
Dma_PageCh5	7:0	00h	DMA2 ch 5 page register

Dma_PageCh5 register

Dma_Page_Reserved5- RW – 8 bits - [IO_Reg: 8Ch]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved5	7:0	00h	Dma Page Reserved5 register

Dma_Page_Reserved5 register

Dma_Page_Reserved6- RW – 8 bits - [IO_Reg: 8Dh]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved6	7:0	00h	Dma Page Reserved6 register

Dma_Page_Reserved6 register

Dma_Page_Reserved7- RW – 8 bits - [IO_Reg: 8Eh]			
Field Name	**Bits**	**Default**	**Description**
Dma_Page_Reserved7	7:0	00h	Dma Page Reserved7 register

Dma_Page_Reserved7 register

Dma_Refresh- RW – 8 bits - [IO_Reg: 8Fh]			
Field Name	**Bits**	**Default**	**Description**
Dma_Refresh	7:0	00h	DMA2 ch4 page register.

Dma_Refresh register

FastInit- RW – 8 bits - [IO_Reg: 92h]			
Field Name	**Bits**	**Default**	**Description**
FastInit	0	0b	FAST_INIT. This read/write bit provides a fast software executed processor reset function. Writing a 1 to this bit will cause the INIT assertion for approximately 4ms. Before another INIT pulse can be generated via this register, this bit must be written back to a 0.
A20EnB	1	0b	A20Enable Bar bit; if set to 1 A20M# function is disabled.

IntrCntrl2Reg1- RW – 8 bits - [IO_Reg: A0h]			
Field Name	**Bits**	**Default**	**Description**
IntrCntrl2Reg1	7:0	00h	IRQ8 – IRQ15: Read IRR, ISR Write ICW1, OCW2, OCW3

IntrCntrl2Reg1 register

IntrCntrl2Reg2- RW – 8 bits - [IO_Reg: A1h]			
Field Name	**Bits**	**Default**	**Description**
IntrCntrl2Reg2	7:0	00h	IRQ8 – IRQ15: Read IMR Write ICW2, ICW3, ICW4, OCW1

IntrCntrl2Reg2 register

Dma2_Ch4Addr - RW – 8 bits - [IO_Reg: C0h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch4Addr	7:0	00h	DMA2 Ch4 Base and Current Address

Dma2_Ch4Addr register

Dma2_Ch4Cnt – RW – 8 bits - [IO_Reg: C2h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch4Cnt	7:0	00h	DMA2 Ch4 Base and Current Count

Dma2_Ch4Cnt register

Dma2_Ch5Addr - RW – 8 bits - [IO_Reg: C4h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch5Addr	7:0	00h	DMA2 Ch5 Base and Current Address

Dma2_Ch5Addr register

Dma2_Ch5Cnt - RW – 8 bits - [IO_Reg: C6h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch5Cnt	7:0	00h	DMA2 Ch4 Base and Current Count

Dma2_Ch5Cnt register

Dma2_Ch6Addr - RW – 8 bits - [IO_Reg: C8h]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch6Addr	7:0	00h	DMA2 Ch6 Base and Current Address

Dma2_Ch6Addr register

Dma2_Ch6Cnt - RW – 8 bits - [IO_Reg: CAh]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch6Cnt	7:0	00h	DMA2 Ch6 Base and Current Count

Dma2_Ch6Cnt register

Dma2_Ch7Addr - RW – 8 bits - [IO_Reg: CCh]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch7Addr	7:0	00h	DMA2 Ch5 Base and Current Address

Dma2_Ch7Addr register

Dma_Ch7Cnt - RW – 8 bits - [IO_Reg: CEh]			
Field Name	**Bits**	**Default**	**Description**
Dma2_Ch7Cnt	7:0	00h	Channel 7 DMA base and current count

Dma2_Ch7Cnt register

Dma_Status - RW – 8 bits - [IO_Reg: D0h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Status	7:0	00h	DMA2 status register

Dma_Status register

Dma_WriteRequest - RW – 8 bits - [IO_Reg: D2h]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteRequest	7:0	00h	DMA2 request register

Dma_WriteRequest register

Dma_WriteMask - RW – 8 bits - [IO_Reg: D4h]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteMask	7:0	00h	DMA2 channel mask register

Dma_WriteMask register

Dma_WriteMode - RW – 8 bits - [IO_Reg: D6h]			
Field Name	**Bits**	**Default**	**Description**
Dma_WriteMode	7:0	00h	DMA2 mode register

Dma_WriteMode register

Dma_Clear - RW – 8 bits - [IO_Reg: D8h]			
Field Name	**Bits**	**Default**	**Description**
Dma_Clear	7:0	00h	Channel 4-7 clear byte pointer

Dma_Clear register

Dma_Clear - RW – 8 bits - [IO_Reg: DAh]			
Field Name	**Bits**	**Default**	**Description**
Dma_Clear	7:0	00h	Channel 4-7 DMA master clear

Dma_Clear register

Dma_ClrMask - RW – 8 bits - [IO_Reg: DCh]			
Field Name	**Bits**	**Default**	**Description**
Dma_ClrMask	7:0	00h	Channel 4-7 DMA Clear Mask

Dma_ClrMask register

Dma_ClrMask - RW – 8 bits - [IO_Reg: DEh]			
Field Name	**Bits**	**Default**	**Description**
Dma_AllMask	7:0	00h	DMA2 mask register

Dma_AllMask register

NCP_Error - RW – 8 bits - [IO_Reg: F0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	6:0	00h	
WarmBoot	7	0b	Warm or cold boot indicator 0: Cold 1: Warm, this bit is set when any value is written to this register;

NCP_Error register: In addition to the WarmBoot function, writing to this port will assert IGNNE# if FERR# is true. If FERR# is false, then write to this port will not assert IGNNE#.

DMA1_Extend - RW – 8 bits - [IO_Reg: 40Bh]			
Field Name	**Bits**	**Default**	**Description**
DMA1_Extend	7:0	00h	DMA1 extended write mode register

DMA1_Extend register

IntrEdgeControl- RW – 16 bits - [IO_Reg: 4D0h]			
Field Name	**Bits**	**Default**	**Description**
IRQ0Control	0	0b	1: Level 0: Edge
IRQ1Control	1	0b	1: Level 0: Edge
Reserved	2	0b	
IRQ3Control	3	0b	1: Level 0: Edge
IRQ4Control	4	0b	1: Level 0: Edge
IRQ5Control	5	0b	1: Level 0: Edge
IRQ6Control	6	0b	1: Level 0: Edge
IRQ7Control	7	0b	1: Level 0: Edge
IRQ8Control	8	0b	(Read Only) Always Edge
IRQ9Control	9	0b	1: Level 0: Edge
IRQ10Control	10	0b	1: Level 0: Edge
IRQ11Control	11	0b	1: Level 0: Edge
IRQ12Control	12	0b	1: Level 0: Edge
Reserved	13	0b	
IRQ14Control	14	0b	1: Level 0: Edge
IRQ15Control	15	0b	1: Level 0: Edge

IntrEdgeControl register: This register programs each interrupt to be either edge or level sensitive.

DMA2_Extend - RW – 8 bits - [IO_Reg: 4D6h]			
Field Name	**Bits**	**Default**	**Description**
DMA2_Extend	7:0	00h	DMA2 extended write mode register

DMA2_Extend register

Pci_Intr_Index - RW – 8 bits - [IO_Reg: C00h]			
Field Name	**Bits**	**Default**	**Description**
Pci_Intr_Index	7:0	00h	PCI interrupt index –

Pci_Intr_Index register

Pci_Intr_Data - RW – 8 bits - [IO_Reg: C01h]			
Field Name	**Bits**	**Default**	**Description**
Pci_Intr_Data	7:0	00h	PCI redirection register;

Pci_Intr_Data register

Pci_Error - RW – 8 bits - [IO_Reg: C14h]			
Field Name	**Bits**	**Default**	**Description**
Serr_Nmi_Status	0	-	Set to 1 when NMI generation is enabled and SERR# has been asserted due to a PCI error. Cleared by writing a one to port 61h, bit 2. [Read-only]
Perr_Nmi_Status	1	-	Set to 1 when NMI generation is enabled and PERR# has been asserted due to a PCI data parity error. Cleared by writing a one to port 61h, bit 2. [Read-only]
Serr_Nmi	2	1b	Enable NMI generation from SERR# 0: Enable 1: Disable
Perr_Nmi	3	1b	Enable NMI generation from PERR# 0: Enable 1: Disable
Reserved	7:4	0h	

Pci_Error register

CMIndex - RW – 8 bits - [IO_Reg: C50h]			
Field Name	**Bits**	**Default**	**Description**
CMIndex	7:0	00h	Index register to client management register block 00h: IdRegister 02h: TempStatus 03h: TempInterrupt 12h: SmBus control (control to Gpoc[3:0] pins thru Bit Bang) 13h: Misccontrol Others – Super IO: Not used

CMIndex register

CMData - RW – 8 bits - [IO_Reg: C51h]			
Field Name	**Bits**	**Default**	**Description**
CMData	7:0	00h	Data register to client management register block

CMData register

GpmPort - RW – 8 bits - [IO_Reg: C52h]			
Field Name	**Bits**	**Default**	**Description**
Gpm	7:0	--	If CMIndex.13h[7:6] = 00, then this is the read port for GPM[7:0]. If CMIndex.13h[7:6]= 01, then this is the output enable for GPM[7:0], 0=enable, 1=tristate If CMIndex.13h[7:6]=10, then this is the output state control (providing enable is turned on) If CMIndex 13h[7:6]=11, then this is the GpmLock bits. When GpmLock bit is set, the corresponding Gpm pin is locked by IMC (meaning it is solely controlled by IMC; not by BIOS). Note when this bit is locked, the corresponding PU/PD (PMIO_F7:F6) are locked as well

GpmPort register

PM2_Index - RW – 8 bits - [IO_Reg: CD0h]			
Field Name	**Bits**	**Default**	**Description**
PM2_Index	7:0	00h	Power management 2 index register. This register selects one of the Power Management 2 registers.

PM2_Index register

PM2_Data - RW – 8 bits - [IO_Reg: CD1h]			
Field Name	**Bits**	**Default**	**Description**
PM2_Data	7:0	00h	Power management 2 data register. This register provides the read/write access to the indexed register.

PM2_Data register

BIOSRAM_Index - RW – 8 bits - [IO_Reg: CD4h]			
Field Name	**Bits**	**Default**	**Description**
BiosRamIndex	7:0	00h	BIOS RAM index register. This register selects one of the 256 bytes of BIOS RAM. Data in this RAM is preserved until RSMRST# is asserted, or S5 power is lost.)

BiosRamIndex register

BIOSRAM_Data - RW – 8 bits - [IO_Reg: CD5h]			
Field Name	**Bits**	**Default**	**Description**
BiosRamData	7:0	00h	Power management data register. This register provides the read/write access to the indexed register.

BiosRamData register

PM_Index - RW – 8 bits - [IO_Reg: CD6h]			
Field Name	**Bits**	**Default**	**Description**
PM_Index	7:0	00h	Power management index register. This register selects one of the Power Management registers.

PM_Index register

PM_Data - RW – 8 bits - [IO_Reg: CD7h]			
Field Name	**Bits**	**Default**	**Description**
PM_Data	7:0	00h	Power management data register. This register provides the read/write access to the indexed register. (See ***section 2.3.3, Power Management (PM) Registers*** for more information.)

PM_Data register

3.1.10.2 System Reset Register (IO CF9)

IO_Reg:CF9h is usually for generating system software resets. This register is defined to be a dual port register, and can also be accessed through PM_IO Reg xC5, which is the CF9Shadow register.

3.1.11 Interrupt Routing Registers

C00/C01 will consolidate all interrupt mapping as follow:

Pci_Intr_Index - RW – 8 bits - [IO_Reg: C00h]			
Field Name	**Bits**	**Default**	**Description**
Pci_Intr_Index	6:0	00h	PCI interrupt index. Selects which PCI interrupt to map. 0h: INTA# 1h: INTB# 2h: INTC# 3h: INTD# 4h: INTE# 5h: INTF# 6h: INTG# 7h: INTH# 8h: Misc 9h: Misc0 Ah: Misc1 Bh: Misc2 Ch: INTA from serial irq Dh: INTB from serial irq Eh: INTC from serial irq Fh: INTD from serial irq 10h: SCI 11h: SMBUS0 12h: ASF 13h: HD audio 14h: FC 15h: GEC 16h: PerMon 20h: IMC INT0 21h: IMC INT1 22h: IMC INT2 23h: IMC INT3 24h: IMC INT4 25h: IMC INT5 30h: Dev18 (USB) IntA# 31h: Dev18 (USB) IntB# 32h: Dev19 (USB) IntA# 33h: Dev19 (USB) IntB# 34h: Dev22 (USB) IntA# 35h: Dev22 (USB) IntB# 36h: Dev20 (USB) IntC# 40h: IDE pci interrupt 41h: SATA PCI interrupt 50h: GPPInt0 51h: GPPInt1 52h: GPPInt2 53h: GPPInt3
Pci_Intr_Index	7	0b	0: select IRQ routing to PIC 1: select IRQ routing to IoApic

Pci_Intr_Data - RW – 8 bits - [IO_Reg: C01h]			
Field Name	**Bits**	**Default**	**Description**
Pci_Intr_Data	7:0	00h	For index other than Misc, Misc0, Misc1, Misc2, the register specifies the IRQ number in PIC mode if Pci_Intr_Index bit7 is set or INT number in IOAPIC if Pci_Intr_Index bit7 is set. In the case, only bit[4:0] is valid. Definition for Misc (default 00h): Bit 0: 0: 8254 timer as IRQ0 input source 1: Serial IRQ or PCI devices as IRQ0 input source Bit1: 0: IMC as IRQ1 input source 1: Serial Irq or PCI devices as IRQ1 input source Bit2: 0: Rtc is IRQ8 input source 1: Serial Irq or PCI devices as IRQ8 input source Bit3: 0: IMC as IRQ12 input source 1: Serial Irq or PCI devices as IRQ12 input source Bit[5:4]: 00: IRQ14 come from legacy IDE 01: IRQ14 come from SATA IDE 10: IRQ14 come from SATA2 11: IRQ14 come from SerIrq/Pci interrupt Bit[7:6]: 00: IRQ15 come from legacy IDE 01: IRQ15 come from SATA IDE 10: IRQ15 come from SATA2 11: IRQ15 come from SerIrq/Pci interrupt Definition for Misc0 (default E7h): Bit0: 0: INT0 in IOAPIC comes from IRQ0 in PIC , INT2 in IOAPIC comes from INTR in PIC. 1: INT2 in IOAPIC comes from IRQ0 in PIC , INT0 in IOAPIC comes from INTR in PIC. Bit 1 (Merge_Ec_irq1): 0: Route serial IRQ1 to USB IRQ1 input 1: Route EC IRQ1 to USB IRQ1 input Bit 2 (Merge_Ec_irq12): 0: Route serial IRQ12 to USB IRQ12 input 1: Route EC IRQ12 to USB IRQ12 input Bit 3: MaskIrq1Irq12 0: turn on IRQ1 and IRQ12 1: Mask off IRQ1 and IRQ12 Bit 4: IrqInputEn 0: Mask off Irq input 1: Enable Irq input Bit 5: IRQ1 filter enable Bit 6: IRQ12 filter enable Bit7: INTR 600ns delay Misc2 and Misc1 define the capability bit in HPET capability register[15:0].

3.1.12 IO(x)APIC Registers

IO(x)APIC registers are defined as Memory/IO-mapped register space, the base address of which is defined through PM_Reg x34h.

3.1.12.1 Direct Access Registers

Note: The XAPIC_BASE_REGISTER has a power-on default value of FEC0_0000H.

IO Register Select Register RW [XAPIC_BASE_REGISTER + 00H]			
Field Name	**Bits**	**Default**	**Description**
Indirect Address Offset	7:0	00h	Indirect Address Offset to IO Window Register
Reserved	31:8		

Used to determine which register is manipulated during an IO Window Register read/write operation.

IO Window Register RW [XAPIC_BASE_REGISTER + 10H]			
Field Name	**Bits**	**Default**	**Description**
Mapped by the value in the IO Register Select Register, to the designated indirect access register. Technically a R/W register; however, the read/write capability is determined by the indirect access register referenced by the IO Register Select Register.			

IRQ Pin Assertion Register RW [XAPIC_BASE_REGISTER + 20H]			
Field Name	**Bits**	**Default**	**Description**
Input IRQ	7:0	00h	IRQ number for the requested interrupt
<reserved>	31:8	0000000h	

Write to this register will trigger an interrupt associated with the redirection table entry referenced by the IRQ number. Currently the redirection table has 24 entries. Write with IRQ number greater than 17H has no effect.

EOI Register W [XAPIC_BASE_REGISTER + 40H]			
Field Name	**Bits**	**Default**	**Description**
Vector	7:0	00h	Interrupt vector
<reserved>	31:8	0000000h	

Write to this register will clear the remote IRR bit in the redirection table entry found matching the interrupt vector. This provides an alternate mechanism other than PCI special cycle for EOI to reach IOXAPIC.

3.1.12.2 Indirect Access Registers

Software needs to first select the register to access using the IO Register Select Register, and then read or write using the IO Window Register.

IOAPIC ID Register [Indirect Address Offset = 00H] RW			
Field Name	**Bits**	**Default**	**Description**
Reserved	23:0	000000h	
ID	27:24	0h	IOAPIC device ID for APIC serial bus delivery mode
Reserved	31:28	0h	

Not used in XAPIC PCI bus delivery mode.

IOXAPIC Version Register [Indirect Address Offset = 01H] R			
Field Name	**Bits**	**Default**	**Description**
Version	7:0	21h	PCI 2.2 compliant
Reserved	14:8	00h	
PRQ	15	1b	IRQ pin assertion supported
Max Redirection Entries	23:16	17h	24 entries [23:0]
Reserved	31:24	00h	

IOAPIC Arbitration Register [Indirect Address Offset = 02H] R			
Field Name	**Bits**	**Default**	**Description**
Reserved	23:0	000000h	
Arbitration ID	27:24	0h	Arbitration ID for APIC serial bus delivery mode
Reserved	31:28	0h	

Not used in XAPIC PCI bus delivery mode.

Redirection Table Entry [0–23] [Indirect Address Offset = 11/10H–3F/3EH] RW			
Field Name	**Bits**	**Default**	**Description**
Vector	7:0	00h	Interrupt vector associated with this interrupt input
Delivery Mode	10:8	0h	000: Fixed 001: Lowest Priority 010: SMI/PMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
Destination Mode	11	0b	0: Physical 1: Logical
Delivery Status	12	0b	Read Only 0: Idle 1: Send Pending
Interrupt Pin Polarity	13	0b	0: High 1: Low
Remote IRR	14	0b	Read Only. Used for level triggered interrupts only. Set when interrupt message delivered. Cleared by EOI special cycle transaction or write to EOI register
Trigger Mode	15	0b	0: Edge 1: Level
Mask	16	1b	Masks the interrupt injection at the input of this device. Write 0 to unmask
Reserved	31:17	0000h	
Reserved	55:32	000000h	
Destination ID	63:56	0	Bits [19:12] of the address field of the interrupt message

Redirection Table Entry [0–23] [Indirect Address Offset = 11/10H–3F/3EH] RW			
Field Name	**Bits**	**Default**	**Description**

3.2 Host PCI Bridges Registers (Device 20, Function 4)

Note: Some PCI functions are controlled by, and associated with, certain PCI configuration registers in the SMBus/ACPI device. For more information refer to ***section 2.3, SMBus Module and ACPI Block*** (Device 20, Function 0).

PCI Bridge (PCIB) has one set of configuration registers in PCI configuration space identified by PCI function 4 on the South Bridge.

Register Name	Offset Address
Vendor ID	00h
Device ID	02h
PCI Command	04h
PCI Device Status	06h
Revision ID/Class Code	08h
Cache Line Size	0Ch
Latency Timer	0Dh
Header Type	0Eh
Reserved	0Fh
Primary Bus Number	18h
Secondary Bus Number	19h
Subordinate Bus Number	1Ah
Secondary Latency Timer	1Bh
IO Base	1Ch
IO Limit	1Dh
Secondary Status	1Eh
Memory Base	20h
Memory Limit	22h
Prefetchable Memory Base	24h
Prefetchable Memory Limit	26h
IO Base Upper 16 Bits	30h
IO Limit Upper 16 Bits	32h
Capability pointer	34h
Reserved	36h
Interrupt Line	3Ch
Interrupt Pin	3Dh
Bridge Control	3Eh
Chip Control	40h
Reserved	41h
CLK Control	42h
Arbiter Control and Priority Bits	43h
SMLT Performance	44h
PMLT Performance	46h
Reserved	48h
Reserved	49h
PCICLK Enable Bits	4Ah
Misc Control	4Bh
AutoClockRun Control	4Ch
Dual Address Cycle Enable and PCIB_SCLK_Stop Override	50h
MSI Mapping Capability	54h
Signature Register for Microsoft Rework for Subtractive Decode	58h
Reserved	5Ch
SPCI IDSEL MaskB	5Eh
Reserved	60h
Misc Control	64h

Vender ID - R - 16 bits - [PCI_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1002h	Vendor Identifier. The vendor ID is 0x1002. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor IDs

Vendor ID register

Device ID - R - 16 bits - [PCI_Reg:02h]			
Field Name	**Bits**	**Default**	**Description**
Device ID	15:0	4384h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.

Device ID register

Command - RW - 16 bits - [PCI_Reg:04h]			
Field Name	**Bits**	**Default**	**Description**
IO Enable	0	0b	I/O Response Enable. PCIB responds to I/O space accesses on the primary bus. 0: Disable 1: Enable
Memory Enable	1	0b	Memory Response Enable. PCIB responds to memory space accesses on the primary bus. 0: Disable 1: Enable
Master Enable	2	0b	Provides the ability of PCIB to act as a PCI bus master on the primary bus. 0: Disable 1: Enable
Special Enable	3	0b	Hardwired to 0 to indicate that PCIB ignores special cycles.
Mem Invalidate	4	0b	Hardwired to 0 to indicate that PCIB doesn't issue memory write and invalidate command by itself.
VGA Snoop Enable	5	0b	0: VGA palette write transactions on the primary interface are ignored unless it falls into PCIB's I/O address range. 1: VGA palette write transactions are positively decoded and forwarded downstream.
Parity Error Enable	6	0b	Parity Error Response. 0: Disables PCIB from asserting P_SERR# and P_PERR# and from reporting Detected Parity Error to the Status register. 1: Enables PCIB to assert P_SERR# and P_PERR# and to report Detected Parity Error bit to the Status register.
Addr Stepping Enable	7	0b	Controls whether or not to do address/data stepping, PCIB doesn't support address stepping. Read Only
System Error Enable	8	0b	SERR# Enable. 0: Disable PCIB from asserting P_SERR# and from reporting Signaled System Error bit. 1: Enable PCIB to assert P_SERR# and to report Signaled System Error bit.
Fast Back-to-Back Enable	9	0b	Hardwired to 0 to indicate that PCIB is not capable of issuing fast back-to-back transactions on the primary bus.
Reserved	15:10	00h	Reserved
PCI Command register			

Status - RW - 16 bits - [PCI_Reg:06h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Reserved
Capabilities List	4	0b	Read only. This bit is 1 when reg0x40[3] (MSI Cap Enable) = 1. At other times this bit is 0. 0: The bridge does not support Capabilities List 1: The bridge supports Capabilities List (reg0x34 is the pointer to the data structure).
66MHz Capable	5	1b	Hardwired to 1 to indicate PCIB support of 66MHz primary interface.
Reserved	6	0b	Reserved
Fast Back-to-Back Capable	7	1b	Hardwired to 1 to indicate PCIB is capable of accepting fast back-to-back transactions on the primary bus.
Master Parity Error	8	0b	Master Data Parity Error. An assertion of P_PERR# (when PCIB acts as a master) is received. Writing a 1 clears it.
DevSel Timing	9:10	01b	Hardwired to 01b to indicate PCIB will assert DEVSEL# with medium timing.
Target Abort	11	0b	Signaled Target Abort. Writing a 1 clears it.
Received Target Abort	12	0b	Received Target Abort. Writing a 1 clears it.
Received Master Abort	13	0b	Received Master Abort. Writing a 1 clears it.
Signaled System Error	14	0b	Signaled System Error bit. Writing a 1 clears it.
Parity Error	15	0b	Detected Parity Error. PCIB detected a parity error and will assert P_PERR#. Writing a 1 clears it.

PCI device status register.

Revision ID/Class Code - R - 32 bits - [PCI_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	40h	These bits are hardwired to reg0x40 (CPCTRL) to indicate the revision level of the chip design.
Class Code	31:8	060401h/ 060400h	A class code of 06h indicates a bridge device. A subclass code of 04h indicates PCI bridge. A programming interface of 01h indicates subtractive decoding on the primary bus is supported; whereas 00h indicates it is not supported. The programming interface is read-only in this register, but when reg0x4B[7] (SubDecodeEnable) and reg0x40[5] (Sub Decode Enable) are both 1, it reads 01h; otherwise it reads 00h.

Cache Line Size - RW - 8 bits - [PCI_Reg:0Ch]			
Field Name	**Bits**	**Default**	**Description**
Cache Line Size	7:0	00h	Read Only

Primary Master Latency Timer - RW - 8 bits - [PCI_Reg:0Dh]			
Field Name	**Bits**	**Default**	**Description**
Prim Latency Timer	7:0	00h	Primary master latency timer. Sets the minimum time that the primary bus master can retain the ownership of the bus.

Header Type - R - 8 bits - [PCI_Reg:0Eh]			
Field Name	**Bits**	**Default**	**Description**
Header Type	7:0	81h	Indicates the bridge is a multi-function device.

Primary Bus Number - RW - 8 bits - [PCI_Reg:18h]			
Field Name	**Bits**	**Default**	**Description**
Primary Bus Number	7:0	00h	Bus number of the PCI bus to which the primary interface is connected.

Secondary Bus Number - RW - 8 bits - [PCI_Reg:19h]			
Field Name	**Bits**	**Default**	**Description**
Secondary Bus Number	7:0	00h	Bus number of the PCI bus to which the secondary interface is connected.

SUBBN - RW - 8 bits - [PCI_Reg:1Ah]			
Field Name	**Bits**	**Default**	**Description**
SubordinateBusNum	7:0	00h	Bus number of the highest numbered PCI bus behind PCIB.

Subordinate Bus Number register

Secondary Latency Timer - RW - 8 bits - [PCI_Reg:1Bh]			
Field Name	**Bits**	**Default**	**Description**
Secondary Latency Timer	7:0	00h	Secondary master latency control timer. Sets the minimum time that the secondary bus master can retain the ownership of the bus.

Secondary Master Latency Timer register

IO Base - RW - 8 bits - [PCI_Reg:1Ch]			
Field Name	**Bits**	**Default**	**Description**
IO16	1:0	00b	Indicates a 16-bit I/O address space. Read Only. Can be changed to 32-bit when reg0x4B[5] (IO Mode) is set.
Reserved	3:2	00b	Reserved
IOBase	7:4	0h	Defines the bits[15:12] of the base address of 16-bit or 32-bit I/O space.

IO Limit - RW - 16 bits - [PCI_Reg:1Dh]			
Field Name	**Bits**	**Default**	**Description**
IO16	1:0	00b	Indicates a 16-bit I/O address space. Read Only. Can be changed to 32-bit when reg0x4B[5] (IO Mode) is set.
Reserved	3:2	00b	Reserved
IO Limit	7:4	0h	Defines bits [15:12] of the limit of 16-bit or 32-bit I/O space.

Secondary Status - RW - 16 bits - [PCI_Reg:1Eh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	4:0	00h	Reserved
Sec 66MHz Capable	5	0b	Indicates PCIB doesn't support 66MHz secondary interface. Read Only.
Reserved	6	0b	Reserved
Secondary Fast Back-to-Back Capable	7	1b	Indicates PCIB is capable of accepting fast back-to-back transactions on the secondary bus. Read Only.
Secondary Master Data Parity Error	8	0b	Master Data Parity Error on the secondary bus, assertion of S_PERR# (when PCIB acts as a master) is received, writing a 1 clears it.
Secondary DevSel Timing	10:9	01b	DEVSEL# timing, indicates PCIB will assert DEVSEL# with medium timing on the secondary bus. Read Only.
Secondary Target Abort	11	0b	Signaled Target Abort on the secondary bus, writing a 1 clears it.
Received Secondary Target Abort	12	0b	Received Target Abort on the secondary bus. Writing a 1 clears it.
Received Secondary Master Abort	13	0b	Received Master Abort on the secondary bus. Writing a 1 clears it.
Received Serr	14	0b	Received System Error on the secondary bus, PCIB asserts P_SERR# to propagate the error back to the primary bus. Writing a 1 clears it.

Secondary Status - RW - 16 bits - [PCI_Reg:1Eh]			
Field Name	**Bits**	**Default**	**Description**
Data Parity Error	15	0b	Detected Parity Error on the secondary bus, PCIB detected a parity error and will assert S_PERR#. Writing a 1 clears it.

Memory Base - RW - 16 bits - [PCI_Reg:20h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Indicates a non-prefetchable 32-bit memory space. Read Only.
Non Pref Mem Base	15:4	000h	Defines the highest 12 bits ([31:20]) of the base address of this 32-bit memory space.

Memory Limit - RW - 16 bits - [PCI_Reg:22h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Indicates a non-prefetchable 32-bit memory space. Read Only.
Non Pref Mem Limit	15:4	000h	Defines the highest 12 bits ([31:20]) of the upper limit of this 32-bit memory space.

Prefetchable Memory Base - RW - 16 bits - [PCI_Reg:24h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Indicates a 32-bit only memory space. Read Only
Pref Mem Base	15:4	000h	Defines the highest 12 bits ([31:20]) of the base address of this 32-bit memory space.

Prefetchable Memory Limit - RW - 16 bits - [PCI_Reg:26h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	3:0	0h	Indicates a 32-bit only memory space. Read Only.
Perf Mem Limit	15:4	000h	Defines the highest 12 bits ([31:20]) of the upper limit of this 32-bit memory space.

IO Base Upper 16 Bits - RW - 16 bits - [PCI_Reg:30h]			
Field Name	**Bits**	**Default**	**Description**
IOBase Upper	15:0	0000h	Top 16 bits of the base address of 32-bit I/O transactions. If the I/O address decode mode bit, i.e., reg0x4B[5] (IO Mode), is cleared, then these bits will be 0s.

IO Limit Upper 16 bits - RW - 16 bits - [PCI_Reg:32h]			
Field Name	**Bits**	**Default**	**Description**
IOLimit Upper	15:0	0000h	Top 16 bits of the upper limit of 32-bit IO transactions. If the I/O address decode mode bit, i.e., reg0x4B[5] (IO Mode), is cleared, then these bits will be 0s.

Capabilities Pointer - R - 8 bits - [PCI_Reg:34h]			
Field Name	**Bits**	**Default**	**Description**
Capabilities Pointer	7:0	00h	Enhanced Capability Pointer. Read Only. Value = 54h when reg0x40[3] (MSI Cap Enable) is set to 1.

Interrupt Line - R - 8 bits - [PCI_Reg:3Ch]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Line	7:0	00h	Interrupt pin routing information, used as communication window between BIOS and the device driver.

Interrupt Pin - R - 8 bits - [PCI_Reg:3Dh]			
Field Name	**Bits**	**Default**	**Description**
Interrupt Pin	7:0	00h	Interrupt pin usage information. 0 indicates PCIB does not support interrupt routing.

Bridge Control - RW - 16 bits - [PCI_Reg:3Eh]			
Field Name	**Bits**	**Default**	**Description**
Parity Error Enable	0	0b	Parity Error Response. 0: Disable PCIB from asserting P_SERR# and S_PERR# and from reporting Detected Parity Error to the Secondary Status register. 1: Enable PCIB to assert P_SERR# and S_PERR# and to report Detected Parity Error to the Secondary Status register.
SERRr# Enable	1	0b	SERR# Forward Enable. 0: PCIB doesn't drive P_SERR# when it detects S_SERR#. 1: PCIB drives P_SERR# when it detects S_SERR#, if reg0x04[8] (System Error Enable) is set.
ISA_Enable	2	0b	ISA Enable. 0: No ISA address mode 1: ISA address mode is supported.
VGA_Enable	3	0b	VGA Enable. 0: Disable 1: Enable
VGA 16-bit Decode	4	0b	This bit only has meaning if either bit[3] (VGA Enable) of this register, or bit[5] (VGA Palette Snoop Enable) of the Command register, is also set to 1, thereby enabling VGA I/O decoding and forwarding by the bridge. The status after reset is 0. This read/write bit enables system configuration software to select between 10-bit and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from the primary to the secondary bus. 0: Execute 10-bit address decodes on VGA I/O accesses. 1: Execute 16-bit address decodes on VGA I/O Accesses.
Master Abort Report	5	0b	0: Do not report master aborts (return FFFF,FFFFh on reads and discard data on write) 1: Report master aborts by signaling target abort or by asserting SERR# if enabled.
Secondary Reset	6	0b	Secondary bus reset. This bit can be masked using ACPI PCI Config register (pmio reg0x04[25]). 0: Disable 1: Trigger reset
Secondary Fast Back-to-Back Enable	7	0b	PCIB is not capable of issuing fast back-to-back transactions on the secondary bus. Read Only
Primary Discard Timer	8	0b	Primary Discard Timer configuration 0: Configure the timer to 15-bit 1: Configure the timer to 10-bit
Secondary Discard Timer	9	0b	Secondary Discard Timer configuration 0: Configure the timer to 15-bit 1: Configure the timer to 10-bit
Discard Timer Status	10	0b	0: No discard timer error 1: Discard timer error
Discard Timer Serr# Enable	11	0b	0: Disable 1: Enable
Reserved	15:12	0h	Reserved

CPCTRL - RW - 8 bits - [PCI_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	0b	Reserved
Mem Write Size Ctrl	1	0b	Controls the memory write size. When set, the memory write size will be cacheline aligned; else it will be 32-byte aligned.
Lock Enable	2	1b	Downstream locked transaction enable.
MSI Cap Enable	3	0b	MSI Capability Enable Guide bit. Setting this bit to 1 will change the status of reg0x06[4] (Capabilities List) from 0 to 1 and will change reg0x34[7:0] (Capabilities Pointer) from the default value of 00h to 54h. 1: Enable 0: Disable
Reserved	4	0b	Reserved
Sub Decode Enable	5	0b	This bit is used only when reg0x4B[7] (SubDecodeEnable) = 1. 1: Subtractive decoding is enabled. 0: Subtractive decoding is disabled.
Bridge Lock State	7:6	00b	Bridge secondary master lock states. Read Only 00: Free 01: Busy 10: Req 11: Locked

Chip control register

Reserved - RW - 8 bits - [PCI_Reg:41h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	-	Reserved

CLKCTRL - RW - 8 bits - [PCI_Reg:42h]			
Field Name	**Bits**	**Default**	**Description**
PCICLKStopEnable	0	0b	33MHz PCICLKs request bit. 1: 33 MHz PCI clocks are requested to stop.
PCICLKStopStatus	1	0b	Read only. 33MHz PCICLKs stop status: 1: Stopped 0: Running.
PCICLK0Enable	2	1b	33MHz PCICLK0 Enable.
PCICLK1Enable	3	1b	33MHz PCICLK1 Enable.
PCICLK2Enable	4	1b	33MHz PCICLK2 Enable.
PCICLK3Enable	5	1b	33MHz PCICLK3 Enable.
P2SControl	6	0b	P_CLK domain to S_CLK domain synch-up disable.
S2PControl	7	0b	S_CLK domain to P_CLK domain synch-up disable.

Clock control register

ARCTRL - RW - 8 bits - [PCI_Reg:43h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	6:0	ffh	Reserved
ArbiterEnable	7	1b	Arbiter Enable. 0: Disabled to give PCIB the exclusive ownership of the secondary bus.

Arbiter control register

SMLT_PERF - R - 16 bits - [PCI_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
SMLT_Perf	15:0	0000h	Count the total number of a burst being broken into multiple transactions due to MLT timeout.

Secondary MLT performance register

PMLT_PERF - R - 16 bits - [PCI_Reg:46h]			
Field Name	**Bits**	**Default**	**Description**
PMLT_Perf	15:0	0000h	Count the total number of a burst being broken into multiple transactions due to MLT timeout.

Primary MLT performance register

Reserved - RW - 8 bits - [PCI_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	1b	Reserved

Reserved - RW - 8 bits - [PCI_Reg:49h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	1b	Reserved

PCICLK Enable Bits - RW - 8 bits - [PCI_Reg:4Ah]			
Field Name	**Bits**	**Default**	**Description**
PCICLK4Enable	0	1b	33MHz PCICLK4 Enable.
Reserved	1	1b	Reserved
Reserved	2	1b	Reserved
PCICLK7Enable	3	1b	33MHz internal feedback clock. Should be programmed to 1 always.
Reserved	7:4	3h	Reserved

Misc Control - RW - 8 bits - [PCI_Reg:4Bh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	0	-	
Memory Read Burst Size	4:1	0h	Specifies up to how many double words burst to support during an upstream or downstream memory read. 1xxx: Burst up to 16 double words 01xx: Burst up to 8 double words 001x: Burst up to 4 double words 0001: Burst up to 2 double words Others: Burst up to 8 double words **Note:** It has no effect on a downstream normal memory read (other than read line and read multiple), which has no burst in this design.
IOMode	5	0b	Control bit to change the I/O addressing mode to 32/16 bit. 0: 16-bit; 1: 32-bit.
MemReadCmdMatch	6	0b	Control bit to enable the match of memory read/memory read line commands when there is a read command in the Delay queue.
SubDecodeEnable	7	0b	Control bit for the subtractive decode status (reg0x08[8] (Class Code)). 0: No subtractive decode; 1: Whether subtractive decode is enabled depends on reg0x40[5] (Sub Decode Enable).

AutoClockRun Control - RW - 32 bits - [PCI_Reg:4Ch]			
Field Name	**Bits**	**Default**	**Description**
Autoclkrun Enable	0	0b	Enable the auto clkrun functionality.
Autoclkrun Count	31:1	0000_0000h	Number of cycles after which the secondary clock stops when clkrun is enabled.

Dual Address Cycle Enable and PCIB_CLK_Stop Override - RW - 16 bits - [PCI_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
PCIB_Dual_EN_up	0	0b	Enable decoding of Dual Address Cycle on secondary side for upstream memory transactions.
PCIB_Dual_EN_dn	1	0b	Enable decoding of Dual Address Cycle on secondary side for downstream memory transactions.
Reserved	5:2	0h	
ClkrunOvrridePCICLK	6	0b	When set, overrides the CLKRUN# and 33MHz PCICLK continues to run.
ClkrunOvrridePCICLK1	7	0b	When set, overrides the CLKRUN# and 33MHz PCICLK1 continues to run.
ClkrunOvrridePCICLK2	8	0b	When set, overrides the CLKRUN# and 33MHz PCICLK2 continues to run.
ClkrunOvrridePCICLK3	9	0b	When set, overrides the CLKRUN# and 33MHz PCICLK3 continues to run.
ClkrunOvrridePCICLK4	10	0b	When set, overrides the CLKRUN# and 33MHz PCICLK4 continues to run.
ClkrunOvrrideLPCCLK	11	0b	When set, overrides the CLKRUN# and LPCCLK continues to run.
ClkrunOvrrideLPCCLK1	12	0b	When set, overrides the CLKRUN# and LPCCLK1 continues to run.
ClkrunOvrridePCICLKFB	13	0b	When set, overrides the CLKRUN# and 33MHz PCICLKFB continues to run. PCICLKFB is the feedback clock that is used internally by PCIB.
Reserved	14	0b	
Reserved	15	0b	

MSI Mapping Capability - R - 32 bits - [PCI_Reg:54h]			
Field Name	**Bits**	**Default**	**Description**
MSI Cap ID	7:0	08h	MSI Capability ID
MSI Cap Pointer	15:8	00h	MSI Capabilities Pointer
MSI Cap Enable	16	1b	MSI Capabilities Enable
MSI Fixed	17	1b	MSI Fixed
MSI Reserved	26:18	000h	Reserved
MSI CapType	31:27	15h	MSI Capability Type

Signature Register for Microsoft Rework for Subtractive Decode - R - 32 bits - [PCI_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
Signature Register for Microsoft Rework for Subtractive Decode	31:0	00000000h	When Microsoft® Rework for Subtractive Decode is done, this register will contain the signature value.

Reserved – RW - 16 bits - [PCI_Reg:5Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	-	

SPCI IDSEL MaskB – RW - 16 bits - [PCI_Reg:5Eh]			
Field Name	**Bits**	**Default**	**Description**
PCI IDSEL MaskB	15:0	FFFFh	Each bit represents masking of the specific device on the PCI bus. The purpose of this register is to hide the device from the OS. 0: The corresponding IDSEL bit is masked. 1: The corresponding IDSEL bit is not masked.

Reserved – RW - 32 bits - [PCI_Reg:60h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Misc Control Register - RW - 32 bits - [PCI_Reg:64h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	11:0	-	
Fast Grant Deassert En	12	1b	Normally PCIGNT# is deasserted two clocks after PCIREQ# deasserts. With this bit set, PCIGNT# will deassert 1 clock after PCIREQ# deasserts. It is recommended to have this bit set.
Reserved	19:13	-	
One Channel Enable	20	0h	When this bit is set to 1, the four upstream read channels are cut to one channel.
Reserved	24:21	-	
Spci Grant 3 Output Enable	25	0h	0: Disable spci gnt 3 output. 1: Enable spci gnt 3 output.
Reserved	31:26	0h	

Chapter 4 UMI/PCIe® Bridge Registers

The Unified Media Interface (UMI) and the FCH/GPP link interface are configured through the following seven register spaces: ABCFG, AXCFG, AXINDC, AXINDP, RCCFG, RCINDC, and RCINDP. These register spaces, and the method for accessing them, are described in the following sections.

4.1 Accessing UMI and PCIe® Bridge Registers

4.1.1 AB_INDX/AB_DATA

An indirect mechanism has to be used to access any of the seven register spaces. The method makes use of an address-register/data-register pair: AB_INDX/AB_DATA.

Note: AB_INDX is write-only. Reads to this register may result in data corruption.

AB_INDX – W – 32 bits – [ABRegBar: 00h]					
Field Name	**Bits**	**Default**	**Description**		
RegAddr	16:0		Register Address		
Reserved	23:17		Reserved		
PortNum	25:24		Port number for RC_INDP Registers 00: Port A 01 : Port B This field only applies to RC_INDP registers and has no effect on other register spaces.		
Reserved	28:26		Reserved		
RegSpace	31:29		000	AXINDC	AXINDC Index/Data Registers
			010	AXINDP	AXINDP Index/Data Registers
			100	AXCFG	UMI Configuration
			110	ABCFG	A-Link Bridge Configuration
			001	RCINDC	RCINDC Registers
			011	RCINDP	RCINDP Registers
			101	Reserved	
			111	Reserved	

AB_DATA – RW – 32 bits – [ABRegBar: 04h]			
Field Name	**Bits**	**Default**	**Description**
Data	31:0		

The AB_INDX/AB_DATA register pair is located in the IO address space as defined by ABRegBar in the PM_Reg E0h. The “RegSpace” is used to define different register blocks access and the “RegAddr” is used to defined the register index.

4.2 UMI/PCIe® Register Descriptions

4.2.1 ABCFG Register

ABCFG, registers are accessed indirectly through AB_INDX/AB_DATA. To read or write a particular register through AB_INDX/AB_DATA, the register address and the register space identifier are first written to AB_INDX with RegSpace (AB_INDX[31:29]) = “110” and register index mapped to RegAddr (AB_INDX[16:0]). The specified register is then accessed by doing a read or write to AB_DATA. Two programming examples are provided below to illustrate the use of AB_INDX/AB_DATA to access ABCFG registers.

Example: Write FFFFFFFFh to ABCFG:58h

```
OUT AB_INDX, C0000058h     // Set AB_INDX RegSpace=110, RegAddr=58h
OUT AB_DATA, FFFFFFFFh
```

Register Name	Offset Address
Vendor ID	00
Revision ID	08
MiscCtl_50	50
MiscCtl_54	54
BL RAB Control	58
Reserved	60 -78
BL DMA Prefetch Enable Control	80
BIF Control 0	90
MSI Control	94
BIF Control 1	98
MiscCtl_9C	9C
PCIEPHY Control Enable	A0
PCIEPHY Control-1	A4
PCIEPHY Control-2	A8
Reserved	B0
PCIE_GPP_Enable	C0
PCIE_P2P_Int_Map	C4
Reserved	D0 - EC
GPP_Upstream_Control	F0
FCH_Trap_Control	FC
FCH_Trap0_AddrL	100
FCH_Trap0_AddrH	104
FCH_Trap0_Cmd	108
FCH_Trap0_Data	10C
FCH_Trap1_AddrL	110
FCH_Trap1_AddrH	114
FCH_Trap1_Cmd	118
FCH_Trap1_Data	11C
FCH_Trap2_AddrL	120
FCH_Trap2_AddrH	124
FCH_Trap2_Cmd	128
FCH_Trap2_Data	12C
FCH_Trap3_AddrL	130
FCH_Trap3_AddrH	134
FCH_Trap3_Cmd	138

Register Name	Offset Address
FCH_Trap3_Data	13C
Reserved	300 - 354
GPP0_Shadow_Command	404
GPP0_Shadow_Bus_Number	418
GPP0_Shadow_IO_Limit_Base	41C
GPP0_Shadow_Mem_Limit_Base	420
GPP0_Shadow_Pref_Mem_Limit_Base	424
GPP0_Shadow_Pref_Base_Upper	428
GPP0_Shadow_Pref_Limit_Upper	42C
GPP0_Shadow_IO_Limit_Base_Upper	430
GPP0_Shadow_Bridge_Control	43C
GPP1_Shadow_Command	444
GPP1_Shadow_Bus_Number	458
GPP1_Shadow_IO_Limit_Base	45C
GPP1_Shadow_Mem_Limit_Base	460
GPP1_Shadow_Pref_Mem_Limit_Base	464
GPP1_Shadow_Pref_Base_Upper	468
GPP1_Shadow_Pref_Limit_Upper	46C
GPP1_Shadow_IO_Limit_Base_Upper	470
GPP1_Shadow_Bridge_Control	47C
Reserved	484 to 4FC
MiscCtl_10050	10050
AL_Arb_Ctl	10054
AL_Clk_Ctl	10056
AL RAB Control	10058
AL DMA Prefetch Enable Control	10060
AL DMA Prefetch Flush Control	10064
AL DMA Prefetch Control	1006C
ClkMuxStatus	10080
MiscCtl_10090	10090

Vendor ID – R – 32 bits – [ABCFG_Reg:00h]			
Field Name	**Bits**	**Default**	**Description**
Vendor ID	15:0	1002h	Vendor Identifier. The vendor ID is 0x1002. This is the former ATI vendor ID which is now owned by AMD. AMD officially has two vendor Ids.
Reserved	31:16	0000h	Reserved

Revision ID – R – 32 bits – [ABCFG_Reg:08h]			
Field Name	**Bits**	**Default**	**Description**
Revision ID	7:0	00h	Device Identifier. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.
Reserved	31:8	000000h	Reserved

BL_EventCnt0Lo – R – 32 bits – [ABCFG_Reg:40h]			
Field Name	**Bits**	**Default**	**Description**
BL_EventCnt0Lo	31:0	00000000h	B-Link Event Counter 0[31:0]
BL_EventCnt1Lo – R – 32 bits – [ABCFG_Reg:44h]			
Field Name	**Bits**	**Default**	**Description**
BL_EventCnt1Lo	31:0	00000000h	B-Link Event Counter 1[31:0]

BL_EventCntSel – RW – 16 bits – [ABCFG_Reg:48h]			
Field Name	**Bits**	**Default**	**Description**
BL_EventSel0	7:0	00h	Select event to be counted by BL_EventCnt0.
BL_EventSel1	15:8	00h	Select event to be counted by BL_EventCnt1.

BL_EventCnt0Hi – R – 8 bits – [ABCFG_Reg:4Ah]			
Field Name	**Bits**	**Default**	**Description**
BL_EventCnt0Hi	7:0	00h	B-Link Event Counter 0[39:32]

BL_EventCnt1Hi – R – 8 bits – [ABCFG_Reg:4Bh]			
Field Name	**Bits**	**Default**	**Description**
BL_EventCnt1Hi	7:0	00h	B-Link Event Counter 1[39:32]

BL_EventCntCtl – RW – 32 bits – [ABCFG_Reg:4Ch]			
Field Name	**Bits**	**Default**	**Description**
BL_EventCntEn	0	0b	Enable B-Link event counters.
BL_EventCntResetB	1	1b	Active low reset for B-Link event counters.
BL_EventCntShadow	2	0b	Transfer B-Link event counter to shadow register.
Reserved	31:3	00000000h	Reserved

MiscCtl_50 – RW – 32 bits – [ABCFG_Reg:50h]			
Field Name	**Bits**	**Default**	**Description**
MemRdLineEn	0	0b	Downstream read transactions issued on A-Link as memory-read-line.
Reserved	25:1	-	
BL_MST_NpqFull_En	26	1h	Enable GEC to use second ReqIdHi to send write when the Read tag buff is full (BL_MST_NpqFull is asserted) to improve GEC performance
Reserved	31:27	0h	

MiscCtl_54 – RW – 32 bits – [ABCFG_Reg:54h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	23:0	000000h	Reserved
BL_Clk_Gate_En	24	0b	Set to 0 for AB internal clock gating.
Reserved	25	0b	Reserved.
MstUMI_grnt_split_tran_en	26	0b	Control MST to UMI arbitration scheme based on split write transaction 0: Disable the arbitration scheme 1: Enable the arbitration scheme Only available for silicon revision A12 and above
Reserved	31:26	00h	Reserved.

BL RAB Control – RW – 32 bits – [ABCFG_Reg:58h]			
Field Name	**Bits**	**Default**	**Description**
Rab_timer_ctl	3:0	Eh	The timeout value sets the bits in the RAB timeout counter. If the RAB has been used but the data has not been requested for a certain amount of time, AB will purge the fetched data and release that occupied RAB.
Rab_timer_ctl_pref	7:4	Eh	The same kind of timer like Rab_timer but this is for prefetch purpose. If a RAB is used for prefetch purpose and not been requested for a certain amount of time, AB will purge the prefetched data and release this RAB.
Reserved	8	-	
Reserved	15:9	00h	Reserved
BL_RAB_Depth	21:16	05h	Set depth of B-Link RAB. Maximum legal value is 5.
Reserved	31:21	000h	Reserved

Reserved – RW – 32 bits – [ABCFG_Reg:60h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW – 32 bits – [ABCFG_Reg:64h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW – 32 bits – [ABCFG_Reg:68h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – R – 32 bits – [ABCFG_Reg:6Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – R – 32 bits – [ABCFG_Reg:70h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW – 32 bits – [ABCFG_Reg:74h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW – 32 bits – [ABCFG_Reg:78h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

BL DMA Prefetch Control – RW – 32 bits – [ABCFG_Reg:80h]			
Field Name	**Bits**	**Default**	**Description**
BL_Pref_En	7:0	00h	Enable B-Link prefetch on a per-device basis. Bit [0]: USB OHCI Bit [7:1]: Reserved
Reserved	15:8	00h	Reserved
BL_Pref_Mode	21:16	00h	Bit [16] - Reserved Bit [17] - Reserved Bit [18] - Reserved Bit [19] - Reserved Bit [20] - Reserved Bit [21] - Reserved
Reserved	31:22	000h	Reserved

BIF Control 0 – RW – 32 bits – [ABCFG_Reg:90h]			
Field Name	**Bits**	**Default**	**Description**
Bif_Ctl_0	5:0	00h	BIF Control Register 0 Bit 0 - Enable BIF TXCLK gating. Bits [3:2] - B-Link TLA Debug Bus Select Bit 5 - Enable override of EEPROM Debug Select.
GPP Reset PHY Power Down Enable	6	0b	Set to 1 to enable the function of PHY power down while "GPP_RESET" (ABCFG_Reg xC0[8]) is set. 0: Disable PHY Power down when GPP_RESET=1 1: Enable PHY power down when GPP_RESET=1 Only available for silicon revision A12 and above.
Reserved	16:7	-	Reserved
USB_Delay_BIF_enter_L1	17	0b	0: Disable the feature of delaying L1 entering. 1: Enable the feature that when USB is not idle, it can delay BIF entering L1.
Reserved	18	-	Reserved
GPP L1 PLL Power Down Enable	19	0b	GPP PHY power saving 0: Disable this feature 1: Enable this feature. When all GPP connected ports are in L1 state, it will assert PLL_PDNB_GPP. Only available for silicon revision A12 and above.
Reserved	23:20	-	Reserved
BL_RAM_PwrDn_Disable	24	0b	Disables B-Link RAM power saving mode.
Reserved	25	0b	Reserved
Up_Req_Stall_En	26	0b	Stalls upstream requests when set.
Reserved	31:27	00h	Reserved

MSI Control – RW – 32 bits – [ABCFG_Reg:94h]			
Field Name	**Bits**	**Default**	**Description**
MSI_Addr[39:20]	19:0	00FEEh	MSI Address
MSI_Addr_En	20	0b	Enable AB to detect MSI sent upstream from FCH and inform power-management controller.
Reserved	31:21	000h	Reserved

BIF Control 1 – RW – 32 bits – [ABCFG_Reg:98h]			
Field Name	**Bits**	**Default**	**Description**
Bif_Ctl_1	7:0	0000h	Bif Control Register 1 [4:0] : Spci Debug Select if EEPROM is over-ridden.
Bif_Mst_Clk_Gate_En	8	0b	Enable gating of Bif Master Clocks.
Bif_Slv_Clk_Gate_En	9	0b	Enable gating of Bif Slave Clocks.
Bif_Reg_Clk_Gate_En	10	0b	Enable gating of Bif Reg Clocks
Bif_Clk_Gate_Mode	11	0b	When set to 1, Bif clocks will only be gated if TXCLK can also be gated.
Bif_Clk_Gate_Delay	15:12	0h	Number of cycles to delay before gating BIF/GPP clocks after idle condition is detected. 0h: 0 cycles 1h: 1 cycles 2h: 3 cycles 3h: 5 cycles 4h: 7 cycles 5h: 9 cycles 6h: 11 cycles 7h: 13 cycles 8h: 15 cycles 9h: 20 cycles Ah: 30 cycles Bh: 40 cycles Ch: 50 cycles Dh: 60 cycles Eh: 70 cycles Fh: 80 cycles
AB_BIF_reqid_en	16	1b	1: Enable IOMMU features 0: Disable IOMMU features
AB_BIF_reqid_en_gpp	17	0b	1: Enable IOMMU features related to GPP port 0: Disable IOMMU features related to GPP port
Reserved	31:18	-	Reserved

MiscCtl_9C – RW – 32 bits – [ABCFG_Reg:9Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	Reserved

PCIEPHY Control Enable – RW – 16 bits – [ABCFG_Reg:A0h]			
Field Name	**Bits**	**Default**	**Description**
B_P90PLL_BACKUP_ENABLE	0	0b	Enable bit for bits 2:0 of ABCFG_Reg:A8h (PCIEPHY Control-2)
B_PPLL_PDNB_ENABLE	1	0b	Enable bit for bit 3 of ABCFG_Reg:A8h (PCIEPHY Control-2)
B_P90PLL_IBIAS_RD_ENABLE	2	0b	Enable bit for bits 5:4 of ABCFG_Reg:A8h (PCIEPHY Control-2)
B_P90PLL_CLKF_ENABLE	3	0b	Enable bit for bits 12:6 of ABCFG_Reg:A8h (PCIEPHY Control-2)
B_P90PLL_CLKR_ENABLE	4	0b	Enable bit for bits 14:13 of ABCFG_Reg:A8h (PCIEPHY Control-2)
B_P90RX_EN_ENABLE	5	0b	Enable bit for bit 15 of PCIEPHY Control-2. Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.
B_PRX_PDNB_ENABLE	6	0b	Enable bit for bit 16 of PCIEPHY Control-2. Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.

PCIEPHY Control Enable – RW – 16 bits – [ABCFG_Reg:A0h]			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PWRS_ENB_ENABLE	7	0b	Enable bit for bit 17 of ABCFG_Reg:A8h (PCIEPHY Control-2). Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.
B_P90TX_DRV_STR_ENABLE	8	0b	Enable bit for bits 19:18 of ABCFG_Reg:A8h (PCIEPHY Control-2). Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.
B_P90TX_DEEMPH_STR_ENABLE	9	0b	Enable bit for bits 21:20 of ABCFG_Reg:A8h (PCIEPHY Control-2). Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.
B_PTX_EN_ENABLE	10	0b	Enable bit for bit 22 of ABCFG_Reg:A8h (PCIEPHY Control-2). Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.
B_PTX_PDNB_ENABLE	11	0b	Enable bit for bit 23 of ABCFG_Reg:A8h (PCIEPHY Control-2). Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.
B_PRX_IMPVAL_ENABLE	12	0b	Enable bit for bits 15:0 of ABCFG_Reg:A4h (PCIEPHY Control-1). Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.
B_PTX_IMPVAL_ENABLE	13	0b	Enable bit for bits 31:16 of ABCFG_Reg:A4h (PCIEPHY Control-1). Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.
Reserved	15:4	00b	Reserved

PCIEPHY Control-1 – RW – 32 bits – [ABCFG_Reg:A4h]			
Field Name	**Bits**	**Default**	**Description**
B_PRX_IMPVAL	12:0	0000h	Override the receiver impedance control value of PCIe® PHY using register. Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.
Reserved	18:13	00h	Reserved
B_PTX_IMPVAL	31:19	0000h	Override the receiver impedance control value of PCIe PHY using register. Note that all 4 lanes are controlled by one register. There is no independent control for each of the lanes.

PCIEPHY Control-2 – RW – 32 bits – [ABCFG_Reg:A8h]			
Field Name	**Bits**	**Default**	**Description**
B_P90PLL_BACKUP	2:0	000b	PHY control register
B_PPLL_PDNB	3	0b	PHY control register
B_P90PLL_IBIAS_RD	5:4	00b	PHY control register
B_P90PLL_CLKF	12:6	000_0000b	PHY control register
B_P90PLL_CLKR	14:13	00b	PHY control register
B_P90RX_EN	15	0b	PHY control register. Note that all 8 lanes are controlled by one register. There is no independent control for each of the lanes.
B_PRX_PDNB	16	0b	PHY control register. Note that all 8 lanes are controlled by one register. There is no independent control for each of the lanes.

PCIEPHY Control-2 – RW – 32 bits – [ABCFG_Reg:A8h]			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PWRS_ENB	17	0b	PHY control register. Note that all 8 lanes are controlled by one register. There is no independent control for each of the lanes.
B_P90TX_DRV_STR	19:18	00b	PHY control register. Note that all 8 lanes are controlled by one register. There is no independent control for each of the lanes.
Reserved	21:20	00b	Reserved
B_PTX_EN	22	0b	PHY control register. Note that all 8 lanes are controlled by one register. There is no independent control for each of the lanes.
B_PTX_PDNB	23	0b	PHY control register. Note that all 8 lanes are controlled by one register. There is no independent control for each of the lanes.
B_P90TX_DEEMPH_STR	31:24	0000_0000b	PHY control register. Note that all 8 lanes are controlled by one register. There is no independent control for each of the lanes

Reserved – RW – 32 bits – [ABCFG_Reg:B0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	Reserved

PCIE_GPP_Enable – RW – 32 bits – [ABCFG_Reg:C0h]			
Field Name	**Bits**	**Default**	**Description**
GPP_LINK_CONFIG	3:0	0h	This connects to the STRAP_BIF_LINK_CONFIG signals to support one of 4 legal configurations (from Picard Straps document) 0000: PortA lanes[3:0] 0001: N/A 0010: PortA lanes[1:0], PortB lanes[3:2] 0011: PortA lanes[1:0], PortB lane2, PortC lane3 0100: PortA lane0, PortB lane1, PortC lane2, PortD lane3.
GPP_PortA_Enable	4	0b	GPP PortA Enable. Although a port might be configured, it might not be enabled. 0: Disable Port A 1: Enable Port A
GPP_PortB_Enable	5	0b	GPP Port B Enable. Although a port might be configured, it might not be enabled. 0: Disable Port B 1: Enable Port B
GPP_PortC_Enable*	6	0b	GPP Port C Enable. Although a port might be configured, it might not be enabled. 0: Disable Port C 1: Enable Port C
GPP_PortD_Enable*	7	0b	GPP Port D Enable. Although a port might be configured, it might not be enabled. 0: Disable Port D 1: Enable Port D
GPP_RESET	8	1b	Reset the GPP Ports Reset on S0 power up. BIOS will need to remove reset before allowing system enumeration.
Reserved	31:9	-	Reserved
* Applicable to Hudson-M1 only, not applicable to Hudson-1D.			

PCIE_P2P_Int_Map – RW – 8 bits – [ABCFG_Reg:C4h]			
Field Name	**Bits**	**Default**	**Description**
PortA_map	1:0	00b	This determines the mapping of INTx received from FCHGPP PortA P2P bridge. 00: A to A, B to B, C to C, D to D 01: A to B, B to C, C to D, D to A 10: A to C, B to D, C to A, D to B 11: A to D, B to A, C to B, D to C
PortB_map	3:2	01b	This determines the mapping of INTx received from FCHGPP PortB P2P bridge. 00: A to A, B to B, C to C, D to D 01: A to B, B to C, C to D, D to A 10: A to C, B to D, C to A, D to B 11: A to D, B to A, C to B, D to C
PortC_map	5:4	10b	This determines the mapping of INTx received from FCHGPP PortC P2P bridge. 00: A to A, B to B, C to C, D to D 01: A to B, B to C, C to D, D to A 10: A to C, B to D, C to A, D to B 11: A to D, B to A, C to B, D to C
PortD_map	7:6	11b	This determines the mapping of INTx received from FCHGPP PortD P2P bridge. 00: A to A, B to B, C to C, D to D 01: A to B, B to C, C to D, D to A 10: A to C, B to D, C to A, D to B 11: A to D, B to A, C to B, D to C

PCIE_P2P_Int_Map register

Reserved – W – 32 bits – [ABCFG_Reg:D0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW – 32 bits – [ABCFG_Reg:D4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – R – 32 bits – [ABCFG_Reg:E0h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – R – 32 bits – [ABCFG_Reg:E4h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

Reserved – RW – 32 bits – [ABCFG_Reg:ECh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	

GPP_Upstream_Control – RW – 32 bits – [ABCFG_Reg:F0h]			
Field Name	**Bits**	**Default**	**Description**
Gpp_err_discard	0	1b	Set how to handle GPP upstream ERROR message. 0: Pass upstream to NB. 1: Discard the error message.
Gpp_at_chk_en	1	1b	Address Translation support enable in GPP port 0: Disable Address Translation support. 1: Enable Address Translation support.
Reserved	31:2	-	Reserved

FCH_Trap_Control – RW – 32 bits – [ABCFG_Reg:FCh]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap_Enable	3:0	0000b	Enable(1) or disable(0) corresponding FCH traps[3:0].
Reserved	7:4	0h	Reserved
FCH_Trap_Status	11:8	0000b	SMI status of corresponding FCH traps[3:0]. Write 1 to any of the bits to clear It.
Reserved	31:12	00000h	Reserved

FCH_Trap0_AddrL – RW – 32 bits – [ABCFG_Reg:100h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved
FCH_Trap0_Addr[31:2]	31:2	0000h	Addr[31:2] of FCH trap0

FCH_Trap0_AddrH – RW – 32 bits – [ABCFG_Reg:104h]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap0_Addr[63:32]	31:0	0000h	Addr[63:32] of FCH trap0

FCH_Trap0_Cmd – RW – 8 bits – [ABCFG_Reg:108h]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap0_Type	4:0	0_0000b	Type[4:0] of FCH trap0*
FCH_Trap0_Fmt	6:5	00b	Fmt[1:0] of FCH trap0*
FCH_Trap0_Action	7	0b	Action to FCH trap0. If set to 1, a write will be discarded and a read will have its return data taken from FCH_Trap0_Data. Otherwise the command will proceed as normal after SMI assertion.

***Note:** See *Table 5* for the transaction types defined by Type[4:0] and Fmt[1:0].

Table 5: Transaction Types Defined by Type [4:0] and Fmt[1:0] of FCH_TrapX

TLP Type	Fmt[1:0]	Type [4:0]	TLP Type Description
MRd	00 01	00000	Memory Read Request
MRdLk	00 01	00001	Memory Read Request-Locked
MWr	10 11	00000	Memory Write Request
IORd	00	00010	I/O Read Request
IOWr	10	00010	I/O Write Request

TLP Type	Fmt[1:0]	Type [4:0]	TLP Type Description
CfgRd0	00	00100	Configuration Read Type 0
CfgWr0	10	00100	Configuration Write Type 0
CfgRd1	00	00101	Configuration Read Type1
CfgWr1	10	00101	Configuration Write Type 1
TCfgRd	00	11011	Deprecated TLP Type
TCfgWr	10	11011	Deprecated TLP Type
Msg	01	1 0r2r1r0	Message Request – The sub-field r[2:0] specifies the Message routing mechanism
MsgD	11	1 0r2r1r0	Message Request with data payload – The sub-field r[2:0] specifies the Message routing mechanism
Cpl	00	01010	Completion without Data – Used for I/O and Configuration Write Completions and Read Completions (I/O, Configuration, or Memory) with Completion Status other than Successful Completion
CplD	10	01010	Completion with Data – Used for Memory, I/O, and Configuration Read Completions.
CplLk	00	01011	Completion for Locked Memory Read without Data – Used only in error case
CplDLk	10	01011	Completion for Locked Memory Read – otherwise like Cp

FCH_Trap0_Data – RW – 32 bits – [ABCFG_Reg:10Ch]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap0_Data	31:0	0000h	Read return data of FCH trap0. This is valid only if the trap is a read and FCH_Trap0_Action (bit 7 of RegAdddr:108h) is set to 1.

FCH_Trap1_AddrL – RW – 32 bits – [ABCFG_Reg:110h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved
FCH_Trap1_Addr[31:2]	31:2	0000h	Addr[31:2] of FCH trap1

FCH_Trap1_AddrH – RW – 32 bits – [ABCFG_Reg:114h]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap1_Addr[63:32]	31:0	0000h	Addr[63:32] of FCH trap1

FCH_Trap1_Cmd – RW – 8 bits – [ABCFG_Reg:118h]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap1_Type	4:0	0_0000b	Type[4:0] of FCH trap1
FCH_Trap1_Fmt	6:5	00b	Fmt[1:0] of FCH trap1

FCH_Trap1_Cmd – RW – 8 bits – [ABCFG_Reg:118h]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap1_Action	7	0b	Action to FCH trap1. If set to 1, a write will be discarded and a read will have its return data taken from FCH_Trap1_Data. Otherwise the command will proceed as normal after SMI assertion.

***Note:** See *Table 5* for the transaction types defined by Type[4:0] and Fmt[1:0].

FCH_Trap1_Data – RW – 32 bits – [ABCFG_Reg:11Ch]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap1_Data	31:0	0000h	Read return data of FCH trap1. This is valid only if the trap is a read and FCH_Trap1_Action (ABCFG_Reg:11Ch[7]) is set to 1.

FCH_Trap2_AddrL – RW – 32 bits – [ABCFG_Reg:120h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved
FCH_Trap2_Addr[31:2]	31:2	0000h	Addr[31:2] of FCH trap2

FCH_Trap2_AddrH – RW – 32 bits – [ABCFG_Reg:124h]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap2_Addr[63:32]	31:0	0000h	Addr[63:32] of FCH trap2

FCH_Trap2_Cmd – RW – 8 bits – [ABCFG_Reg:128h]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap2_Type	4:0	0_0000b	Type[4:0] of FCH trap2
FCH_Trap2_Fmt	6:5	00b	Fmt[1:0] of FCH trap2
FCH_Trap2_Action	7	0b	Action to FCH trap2. If set to 1, a write will be discarded and a read will have its return data taken from FCH_Trap2_Data. Otherwise the command will proceed as normal after SMI assertion.

***Note:** See *Table 5* for the transaction types defined by Type[4:0] and Fmt[1:0].

FCH_Trap2_Data – RW – 32 bits – [ABCFG_Reg:12Ch]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap2_Data	31:0	0000h	Read return data of FCH trap2. This is valid only if the trap is a read and FCH_Trap2_Action (ABCFG_Reg:128h[7]) is set to 1.

FCH_Trap3_AddrL – RW – 32 bits – [ABCFG_Reg:130h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	1:0	00b	Reserved
FCH_Trap3_Addr[31:2]	31:2	0000h	Addr[31:2] of FCH trap3

FCH_Trap3_AddrH – RW – 32 bits – [ABCFG_Reg:134h]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap3_Addr[63:32]	31:0	0000h	Addr[63:32] of FCH trap3

FCH_Trap3_Cmd – RW – 8 bits – [ABCFG_Reg:138h]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap3_Type	4:0	0_0000b	Type[4:0] of FCH trap3
FCH_Trap3_Fmt	6:5	00b	Fmt[1:0] of FCH trap3
FCH_Trap3_Action	7	0b	Action to FCH trap3. If set to 1, a write will be discarded and a read will have its return data taken from FCH_Trap3_Data. Otherwise the command will proceed as normal after SMI assertion.

FCH_Trap3_Data – RW – 32 bits – [ABCFG_Reg:13Ch]			
Field Name	**Bits**	**Default**	**Description**
FCH_Trap3_Data	31:0	0000h	Read return data of FCH trap3. This is valid only if the trap is a read and FCH_Trap3_Action (bit 7 of ABCFG_Reg:13 Ch) is set to 1.

***Note:** See *Table 5* for the transaction types defined by Type[4:0] and Fmt[1:0].

Reserved – RW – 32 bits – [ABCFG_Reg:300h – 354h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	-	Reserved

Note: This register table represents registers from offset 300h to 354h

GPP0_Shadow_Command – R – 32 bits – [ABCFG_Reg:404h]			
Field Name	**Bits**	**Default**	**Description**
Command Shadow	15:0	0000h	GPP Port0 bridge configuration Command shadow
Reserved	31:16	0000h	Reserved

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP0_Shadow_Bus_Number – R – 32 bits – [ABCFG_Reg:418h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	00h	Reserved
SecBusNumber Shadow	15:8	00h	GPP Port0 bridge configuration Secondary Bus Number shadow
SubBusNumber Shadow	23:16	00h	GPP Port0 bridge configuration Subordinate Bus Number shadow
Reserved	31:24	00h	Reserved

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP0_Shadow_IO_Limit_Base – R – 32 bits – [ABCFG_Reg:41Ch]			
Field Name	**Bits**	**Default**	**Description**
IO_Base Shadow	7:0	00h	GPP Port0 bridge configuration IO Base shadow
IO_Limit Shadow	15:8	00h	GPP Port0 bridge configuration IO Limit shadow
Reserved	31:16	0000h	Reserved
Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.			

GPP0_Shadow_Mem_Limit_Base – R – 32 bits – [ABCFG_Reg:420h]			
Field Name	**Bits**	**Default**	**Description**
Mem_Base Shadow	15:0	0000h	GPP Port0 bridge configuration Memory Base shadow
Mem_Limit Shadow	31:16	0000h	GPP Port0 bridge configuration Memory Limit shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP0_Shadow_Pref_Mem_Limit_Base – R – 32 bits – [ABCFG_Reg:424h]			
Field Name	**Bits**	**Default**	**Description**
Pref_Mem_Base Shadow	15:0	0000h	GPP Port0 bridge configuration Prefetchable Memory Base shadow
Pref_Mem_Limit Shadow	31:16	0000h	GPP Port0 bridge configuration Prefetchable Memory Limit shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP0_Shadow_Pref_Mem_Base_Upper – R – 32 bits – [ABCFG_Reg:428h]			
Field Name	**Bits**	**Default**	**Description**
Pref_Mem_Base_Upper Shadow	31:0	0000_0000h	GPP Port0 bridge configuration Prefetchable Memory Base Upper shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP0_Shadow_Pref_Mem_Limit_Upper – R – 32 bits – [ABCFG_Reg:42Ch]			
Field Name	**Bits**	**Default**	**Description**
Pref_Mem_Limit_Upper Shadow	31:0	0000_0000h	GPP Port0 bridge configuration Prefetchable Memory Limit Upper shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP0_Shadow_IO_Limit_Base_Upper – R – 32 bits – [ABCFG_Reg:430h]			
Field Name	**Bits**	**Default**	**Description**
IO_Base_Upper Shadow	15:0	0000h	GPP Port0 bridge configuration IO Base Upper shadow
IO_Limit_Upper Shadow	31:16	0000h	GPP Port0 bridge configuration IO Limit Upper shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP0_Shadow_Bridge_Control – R – 32 bits – [ABCFG_Reg:43Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	0000h	Reserved
Bridge_Control Shadow	31:16	0000h	GPP Port0 bridge configuration Bridge Control shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP1_Shadow_Command – R – 32 bits – [ABCFG_Reg:444h]			
Field Name	**Bits**	**Default**	**Description**
Command Shadow	15:0	0000h	GPP Port1 bridge configuration Command shadow
Reserved	31:16	0000h	Reserved

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP1_Shadow_Bus_Number – R – 32 bits – [ABCFG_Reg:458h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	00h	Reserved
SecBusNumber Shadow	15:8	00h	GPP Port1 bridge configuration Secondary Bus Number shadow
SubBusNumber Shadow	23:16	00h	GPP Port1 bridge configuration Subordinate Bus Number shadow
Reserved	31:24	00h	Reserved

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP1_Shadow_IO_Limit_Base – R – 32 bits – [ABCFG_Reg:45Ch]			
Field Name	**Bits**	**Default**	**Description**
IO_Base Shadow	7:0	00h	GPP Port1 bridge configuration IO Base shadow
IO_Limit Shadow	15:8	00h	GPP Port1 bridge configuration IO Limit shadow
Reserved	31:16	0000h	Reserved

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP1_Shadow_Mem_Limit_Base – R – 32 bits – [ABCFG_Reg:460h]			
Field Name	**Bits**	**Default**	**Description**
Mem_Base Shadow	15:0	0000h	GPP Port1 bridge configuration Memory Base shadow
Mem_Limit Shadow	31:16	0000h	GPP Port1 bridge configuration Memory Limit shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP1_Shadow_Pref_Mem_Limit_Base – R – 32 bits – [ABCFG_Reg:464h]			
Field Name	**Bits**	**Default**	**Description**
Pref_Mem_Base Shadow	15:0	0000h	GPP Port1 bridge configuration Prefetchable Memory Base shadow
Pref_Mem_Limit Shadow	31:16	0000h	GPP Port1 bridge configuration Prefetchable Memory Limit shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP1_Shadow_Pref_Mem_Base_Upper – R – 32 bits – [ABCFG_Reg:468h]			
Field Name	**Bits**	**Default**	**Description**
Pref_Mem_Base_Upper Shadow	31:0	0000_0000h	GPP Port1 bridge configuration Prefetchable Memory Base Upper shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP1_Shadow_Pref_Mem_Limit_Upper – R – 32 bits – [ABCFG_Reg:46Ch]			
Field Name	**Bits**	**Default**	**Description**
Pref_Mem_Limit_Upper Shadow	31:0	0000_0000h	GPP Port1 bridge configuration Prefetchable Memory Limit Upper shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP1_Shadow_IO_Limit_Base_Upper – R – 32 bits – [ABCFG_Reg:470h]			
Field Name	**Bits**	**Default**	**Description**
IO_Base_Upper Shadow	15:0	0000h	GPP Port1 bridge configuration IO Base Upper shadow
IO_Limit_Upper Shadow	31:16	0000h	GPP Port1 bridge configuration IO Limit Upper shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

GPP1_Shadow_Bridge_Control – R – 32 bits – [ABCFG_Reg:47Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	0000h	Reserved
Bridge_Control Shadow	31:16	0000h	GPP Port1 bridge configuration Bridge Control shadow

Shadow registers are read-only. The defined data fields reflect the last write attempt to the same fields in GPP bridge configuration registers.

Reserved – R – 32 bits – [ABCFG_Reg:484h – 4FCh]			
Field Name	**Bits**	**Default**	**Description**
Reserved	31:0	0000h	Reserved

Note: This register table represents registers with offsets from 484h to 4FCh.

AL_EventCnt0Lo – R – 32 bits – [ABCFG_Reg:10040h]			
Field Name	**Bits**	**Default**	**Description**
AL_EventCnt0Lo	31:0	00000000h	A-Link Event Counter 0[31:0]

AL_EventCnt1Lo – R – 32 bits – [ABCFG_Reg:10044h]			
Field Name	**Bits**	**Default**	**Description**
AL_EventCnt1Lo	31:0	00000000h	A-Link Event Counter 1[31:0]

AL_EventCntSel – RW – 16 bits – [ABCFG_Reg:10048h]			
Field Name	**Bits**	**Default**	**Description**
AL_EventSel0	7:0	00h	Select event to be counted by AL_EventCnt0.
AL_EventSel1	15:8	00h	Select event to be counted by AL_EventCnt1.

AL_EventCnt0Hi – R – 8 bits – [ABCFG_Reg:1004Ah]			
Field Name	**Bits**	**Default**	**Description**
AL_EventCnt0Hi	7:0	00h	A-Link Event Counter 0[39:32]

AL_EventCnt1Hi – R – 8 bits – [ABCFG_Reg:1004Bh]			
Field Name	**Bits**	**Default**	**Description**
AL_EventCnt1Hi	7:0	00h	A-Link Event Counter 1[39:32]

AL_EventCntCtl – RW – 32 bits – [ABCFG_Reg:1004Ch]			
Field Name	**Bits**	**Default**	**Description**
AL_EventCntEn	0	0b	Enable A-Link event counters.
AL_EventCntResetB	1	1b	Active low reset for A-Link event counters.
AL_EventCntShadow	2	0b	Transfer A-Link event counter to shadow register.
Reserved	31:3	00000000h	Reserved

MiscCtl_10050 – RW – 32 bits – [ABCFG_Reg:10050h]			
Field Name	**Bits**	**Default**	**Description**
Req_Mask_Pref_Dis	0	0b	Disable setting of A-Link request mask for a currently pending read.
Pcib_Lock_Stall_En	1	1b	Enables stalling of a downstream memory-read-lock command if pci bus is currently locked.
Syncflood_En	2	0b	Enable AB to forward downstream syncflood message to system controller.
Reserved	31:3	-	Reserved

AL_Arb_Ctl – RW – 16 bits – [ABCFG_Reg:10054h]			
Field Name	**Bits**	**Default**	**Description**
Arb_Ctl	11:0	0000h	A-Link Arbiter Control
Reserved	15:12	0h	Reserved

AL_Clk_Ctl – RW – 16 bits – [ABCFG_Reg:10056h]			
Field Name	**Bits**	**Default**	**Description**
AL_Clk_Gate_Delay	7:0	00h	Number of cycles to delay before gating A-Link clocks after idle condition is detected.
AL_Clk_Gate_En	8	0b	Enable gating of A-Link clocks when idle is detected.
Reserved	15:9	00h	Reserved

AL RAB Control – RW – 32 bits – [ABCFG_Reg:10058h]			
Field Name	**Bits**	**Default**	**Description**
Rab_timer_ctl	3:0	Eh	The timeout value sets the bits in the RAB timeout counter. If the RAB has been used but the data has not being requested for certain amount of time, AB will purge the fetched data and release that occupied RAB
Rab_timer_ctl_pref	7:4	Eh	The same kind of timer like rab_timer but this is for prefetch purpose. If a RAB is used for prefetch purpose and not being requested for certain amount of time, AB will purge the prefetched data and release this RAB.
Reserved	8	0b	Reserved
Lpc_dma_mst_mode	9	0b	Set to select if LPC will release PCI bus during DMA retry 0: New design; LPC will release PCI bus during retry 1: Old design; LPC will NOT release PCI bus during retry
Reserved	15:10	-	Reserved
AL_RAB_Depth	21:16	20h	Set depth of A-Link RAB. Maximum legal value is 32.
Reserved	31:22	000h	Reserved

AL MLT Control – RW – 8 bits – [ABCFG_Reg:1005Ch]			
Field Name	**Bits**	**Default**	**Description**
AL_MLT	7:0	FFh	Number of cycles an upstream requestor may occupy A-Link before bus ownership is withdrawn.

AL DMA Prefetch Enable – RW – 32 bits – [ABCFG_Reg:10060h]			
Field Name	**Bits**	**Default**	**Description**
Dma_imp_pref_en_0	15:0	0000h	Implicit Prefetch enable 0: Disable implicit prefetch device in this bit location 1: Enable implicit prefetch device in this bit location Bit [0]: Reserved Bit [1]: Reserved Bit [2]: Reserved Bit [3]: Reserved Bit [4]: PCIB Bit [5]: Reserved Bit [6]: Reserved Bit [7]: Reserved Bit [15:8]: Reserved
Dma_exp_pref_en_0	31:16	0000h	Explicit Prefetch enable 0: Disable implicit prefetch device in this bit location 1: Enable implicit prefetch device in this bit location Bit [16]: Reserved Bit [17]: Reserved Bit [18]: Reserved Bit [19]: Reserved Bit [20]: PCIB Bit [21]: Reserved Bit [22]: Reserved Bit [23]: Reserved Bit [31:24]: Reserved

AL DMA Prefetch Flush Control – RW – 32 bits – [ABCFG_Reg:10064h]			
Field Name	**Bits**	**Default**	**Description**
Dma_imp_pflush_en_0	15:0	0000h	Implicit Prefetch Flush enable 0: Disable implicit prefetch flush device in this bit location 1: Enable implicit prefetch flush device in this bit location Bit [0]: Reserved Bit [1]: Reserved Bit [2]: Reserved Bit [3]: Reserved Bit [4]: PCIB Bit [5]: Reserved Bit [6]: Reserved Bit [7]: Reserved Bit [15:8]: Reserved

AL DMA Prefetch Flush Control – RW – 32 bits – [ABCFG_Reg:10064h]			
Field Name	**Bits**	**Default**	**Description**
Dma_exp_pflush_en_0	31:16	0000h	Explicit Prefetch Flush enable 0: Disable implicit prefetch flush device in this bit location 1: Enable implicit prefetch flush device in this bit location Bit [16]: Reserved Bit [17]: Reserved Bit [18]: Reserved Bit [19]: Reserved Bit [20]: PCIB Bit [21]: Reserved Bit [22]: Reserved Bit [23]: Reserved Bit [31:24]: Reserved

AL Prefetch Limit – RW – 32 bits – [ABCFG_Reg:10068h]			
Field Name	**Bits**	**Default**	**Description**
AL_Pref_Dev_0	3:0	0h	Device for which number of prefetches is controlled by AL_Pref_Lim_0. 1: IDE 4: PCI Bridge
AL_Pref_Lim_0	7:4	0h	Number of prefetches for AL_Pref_Dev_0 will be AL_Pref_Lim_0. 0h: 0 cacheline prefetched 1h: 1 cacheline prefetched. .. 7h: 7 cachelines prefetched.
AL_Pref_Dev_1	11:8	0h	Device for which number of prefetches is controlled by AL_Pref_Lim_1.
AL_Pref_Lim_1	15:12	0h	Number of prefetches for AL_Pref_Dev_0 will be AL_Pref_Lim_1. 0h: 0 cacheline prefetched 1h: 1 cacheline prefetched. .. 7h: 7 cacheline prefetched.
AL_Pref_Dev_2	19:16	0h	Device for which number of prefetches is controlled by AL_Pref_Lim_2.
AL_Pref_Lim_2	23:20	0h	Number of prefetches for AL_Pref_Dev_0 will be AL_Pref_Lim_2. 0h: 0 cacheline prefetched 1h: 1 cacheline prefetched. .. 7h: 7 cacheline prefetched.
AL_Pref_Dev_3	27:24	0h	Device for which number of prefetches is controlled by AL_Pref_Lim_3.
AL_Pref_Lim_3	31:28	0h	Number of prefetches for AL_Pref_Dev_0 will be AL_Pref_Lim_3. 0h: 0 cacheline prefetched 1h: 1 cacheline prefetched. .. 7h: 7 cacheline prefetched.

AL DMA Prefetch Control – RW – 16 bits – [ABCFG_Reg:1006Ch]			
Field Name	**Bits**	**Default**	**Description**
Dma_pref_mode_1	5:0	000000b	[0]: 0: Flush PIO targeted device's DMA read prefetch when there is PIO request 1: Flush all devices' DMA read prefetch when there is PIO request [1]: 0: Flush 1 RAB entry if RAB is full 1: Do not flush any RAB even when RAB is full [2]: 0: Purge RAB entry when DMA write happens at the same prefetched cacheline 1: Do not purge RAB entry when DMA write to the same cacheline with prefetched data [3]: 0: Do not prefetch one more cacheline automatically when there is a hit on a valid RAB entry 1: Aggressively prefetch one more cacheline automatically when there is a hit on a valid RAB entry [4]: 0: Purge last RAB entry when RAB is full and new demand req is coming 1: Purge the first RAB entry when RAB is full and new demand req is coming [5]: During explicit prefetch enable, 0: Do not force to flush pending purge, explicit input flush signal will take main role for flush or not 1: Force to flush pending purge
Reserved	7:6	0h	Reserved
Dma_pref_range_1	13:8	3Fh	000000b: Break prefetch at 64 byte boundary (prefetch disabled). 000001b: Break prefetch at 128 byte boundary 000011b: Break prefetch at 256 byte boundary 000111b: Break prefetch at 512 byte boundary 001111b: Break prefetch at 1K byte boundary 011111b: Break prefetch at 2K byte boundary 111111b: Break prefetch at 4K byte boundary
Reserved	15:14	00b	Reserved

MiscCtl_10070 – RW – 16 bits – [ABCFG_Reg:10070h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	0000h	Reserved

ClkMuxStatus – R – 16 bits – [ABCFG_Reg:10080h]			
Field Name	**Bits**	**Default**	**Description**
ClkMuxStatus	15:0		Status from clk module

BIF Control 0 – RW – 32 bits – [ABCFG_Reg:10090h]			
Field Name	**Bits**	**Default**	**Description**
Reserved	7:0	00h	Reserved
P_Pass_NP_Ctl	12:8	00h	Bit [0]: Allow posted transaction to pass non-posted transaction based on address-decode. Bit [1]: Allow posted transaction to pass non-posted transaction based on inability of non-posted transaction to make forward progress. Bit [4:2]: Number of attempts to complete non-posted transaction before allowing a following posted transaction to pass it.
IO Trap Delay Enable	16	0b	Enables the IO trap delay logic for the SMI message to ensure that the SMI messages are sent to the CPU in the right order. This bit must be programmed as 1.
Reserved	23:17	00h	Reserved
BL_RAM_PwrDn_Disable	24	0b	Disables B-Link RAM power saving mode.
Reserved	31:25	00h	Reserved

MiscCtl_1009C – RW – 16 bits – [ABCFG_Reg:1009Ch]			
Field Name	**Bits**	**Default**	**Description**
Reserved	15:0	0000h	Reserved

4.2.2 AXCFG Registers

AXCFG, registers are accessed indirectly through AB_INDX/AB_DATA. To read or write a particular register through AB_INDX/AB_DATA, the register address and the register space identifier are first written to AB_INDX with RegSpace (AB_INDX[31:29]) = “100” and register index mapped to RegAddr (AB_INDX[16:0]). The specified register is then accessed by doing a read or write to AB_DATA. Two programming examples are provided below to illustrate the use of AB_INDX/AB_DATA to access ABCFG registers.

Example: Read AXCFG:04h to TMP

```
OUT AB_INDX, 80000004h     // Set AB_INDX RegSpace=100, RegAddr=04h.
IN  AB_DATA, TMP           // Read AXCFG:04h into TMP.
```

VENDOR_ID - RW - 16 bits - AXCFG_Reg:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID (R)	15:0	0x0	This field identifies the manufacturer of the device. 0FFFFh is an invalid value for Vendor ID.

Vendor Identification

DEVICE_ID - R - 16 bits - AXCFG_Reg:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	0x0	This field identifies the particular device. This identifier is allocated by the vendor.

Device Identification

COMMAND - RW - 16 bits - AXCFG_Reg:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0. 0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0. 0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	Controls the ability of a PCI Express® endpoint to issue Memory and I/O Read/Write Requests, and the ability of a Root or Switch Port to forward Memory and I/O Read/Write requests in the upstream direction. 0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
PARITY_ERROR_RESPONSE	6	0x0	Parity Error Response. Default value of this field is 0. 0=Disable 1=Enable
AD_STEPPING (R)	7	0x0	Address and Data Stepping. Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
SERR_EN	8	0x0	When set, enables reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. 0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
INT_DIS	10	0x0	Controls the ability of a PCI Express device to generate INTx interrupt Messages. When set, devices are prevented from generating INTx interrupt Messages. Default value 0 0=Enable 1=Disable

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

STATUS - RW - 16 bits - AXCFG_Reg:0x6			
Field Name	**Bits**	**Default**	**Description**
INT_STATUS (R)	3	0x0	Indicates that an INTx interrupt Message is pending internally to the device.
CAP_LIST (R)	4	0x1	Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.

STATUS - RW - 16 bits - AXCFG_Reg:0x6			
Field Name	**Bits**	**Default**	**Description**
PCI_66_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
UDF_EN (R)	6	0x0	User Defined Status Enable 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Does not apply to PCI Express. Hardwired to 0.
MASTER_DATA_PARITY_ERROR	8	0x0	This bit is set by Requestor if its Parity Error Enable bit is set and either of the following two conditions occurs: 1) Requestor receives a Completion marked poisoned 2) Requestor poisons a write Request 0=Inactive 1=Active
DEVSEL_TIMING (R)	10:9	0x0	Does not apply to PCI Express. Hardwired to 0.
SIGNAL_TARGET_ABORT	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status. 0=No Abort 1=Target Abort
RECEIVED_TARGET_ABORT	12	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
RECEIVED_MASTER_ABORT	13	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	This bit must be set whenever the device asserts SERR#. 0=No Error 1=SERR assert
PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1.

The Status register is used to record status information for PCI bus related events.

REVISION_ID - R - 8 bits – AXCFG_Reg:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Major revision ID. Set by the vendor.
MAJOR_REV_ID	7:4	0x0	Minor revision ID. Set by the vendor.

Specifies a device specific revision identifier. The value is chosen by the vendor.

PROG_INTERFACE - R - 8 bits - AXCFG_Reg:0x9			
Field Name	**Bits**	**Default**	**Description**
PROG_INTERFACE	7:0	0x0	Unused

Register-Level Programming Interface Register

SUB_CLASS - R - 8 bits - AXCFG_Reg:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS	7:0	0x0	The Class Code register is read-only and is used with the Base Class Code to identify the specific type of device.

Sub Class Code Register

BASE_CLASS - R - 8 bits - AXCFG_Reg:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS	7:0	0x0	The Class Code register is read-only and is used to identify the generic function of the device.

Base Class Code Register

CACHE_LINE - RW - 8 bits - AXCFG_Reg:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	This read/write register specifies the system cacheline size in units of DWORDs.

Cache Line Size Register

LATENCY - RW - 8 bits - AXCFG_Reg:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER (R)	7:0	0x0	Primary/Master latency timer does not apply to PCI Express. Register is hardwired to 0.

Master Latency Timer Register

HEADER - RW - 8 bits - AXCFG_Reg:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE (R)	6:0	0x0	Type 0 or Type 1 Configuration Space
DEVICE_TYPE (R)	7	0x0	Single function or multi function device 0=Single-Function Device 1=Multi-Function Device

Configuration Space Header

BIST - RW - 8 bits - AXCFG_Reg:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP (R)	3:0	0x0	A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device-specific failure codes can be encoded in the non-zero value.
BIST_STRT (R)	6	0x0	Write a 1 to invoke BIST. Device resets the bit when BIST is complete. Software should fail the device if BIST is not complete after 2 seconds.
BIST_CAP (R)	7	0x0	This bit is read-only and returns 1 the bridge supports BIST, otherwise 0 is returned.

Built In Self Test Register used for control and status of built-in self tests

CAP_PTR - RW - 32 bits - AXCFG_Reg:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR (R)	7:0	0x50	Pointer to a linked list of additional capabilities implemented by this device. 50=Point to PM Capability

Capability Pointer

INTERRUPT_LINE - RW - 8 bits - AXCFG_Reg:0x3C			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0xff	Interrupt Line register communicates interrupt line routing information.

Interrupt Line Register

INTERRUPT_PIN - RW - 8 bits - AXCFG_Reg:0x3D			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN (R)	7:0	0x0	The Interrupt Pin is a read-only register that identifies the legacy interrupt Message(s) the device (or device function) uses NOTE: Bits 3:7 of this field are hardwired to ZERO.

Interrupt Pin Register

ADAPTER_ID - R - 32 bits - AXCFG_Reg:0x2C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID *(mirror of ADAPTER_ID_W:SUBSYSTEM_VENDOR_ID)*	15:0	0x0	Subsystem Vendor ID. Specified by the vendor.
SUBSYSTEM_ID *(mirror of ADAPTER_ID_W:SUBSYSTEM_ID)*	31:16	0x0	Subsystem ID. Specified by the vendor.

Subsystem Vendor and Subsystem ID Register

MIN_GRANT - RW - 8 bits - AXCFG_Reg:0x3E			
Field Name	**Bits**	**Default**	**Description**
MIN_GNT (R)	7:0	0x0	Registers do not apply to PCI Express. Hardwired to 0.

Specifies how long a burst period the device needs, assuming a clock rate of 33 MHz.

MAX_LATENCY - RW - 8 bits - AXCFG_Reg:0x3F			
Field Name	**Bits**	**Default**	**Description**
MAX_LAT (R)	7:0	0x0	Registers do not apply to PCI Express. Hardwired to 0.

Specifies how often the device need to gain access to the PCI bus.

ADAPTER_ID_W - RW - 32 bits - AXCFG_Reg:0x4C			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x0	Subsystem Vendor ID. Specified by the vendor.
SUBSYSTEM_ID	31:16	0x0	Subsystem Vendor ID. Specified by the vendor.

Adapter ID

EXT_BRIDGE_CNTL - RW - 8 bits - AXCFG_Reg:0x40			
Field Name	**Bits**	**Default**	**Description**
IO_PORT_80_EN	0	0x0	Register to enable IO port 80 decoding.

External Bridge Control Register

PMI_CAP_LIST - R - 16 bits - AXCFG_Reg:0x50			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x1	Capability ID Must be set to 01h 1=PCIe® Power Management Registers
NEXT_PTR	15:8	0x58	Next Capability Pointer

Power Management Capability List

PMI_CAP - RW - 16 bits - AXCFG_Reg:0x52			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	2:0	0x3	Version 3=PMI Spec 1.2
PME_CLOCK (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0.
DEV_SPECIFIC_INIT (R)	5	0x0	Device Specific Initialization
AUX_CURRENT (R)	8:6	0x0	AUX Current
D1_SUPPORT (R)	9	0x0	D1 Support 1=Support D1 PM State.
D2_SUPPORT (R)	10	0x0	D2 Support 1=Support D2 PM State.
PME_SUPPORT (R)	15:11	0x0	For a device, this indicates the power states in which the device may generate a PME.

Power Management Capabilities Register

PMI_STATUS_CNTL - RW - 32 bits - AXCFG_Reg:0x54			
Field Name	**Bits**	**Default**	**Description**
POWER_STATE	1:0	0x0	Power State
NO_SOFT_RESET (R)	3	0x0	No Soft Reset
PME_EN (R)	8	0x0	PME Enable
DATA_SELECT (R)	12:9	0x0	Data Select
DATA_SCALE (R)	14:13	0x0	Data Scale
PME_STATUS (R)	15	0x0	PME Status
B2_B3_SUPPORT (R)	22	0x0	B2/B3 Support Does not apply to PCI Express. Hardwired to 0.
BUS_PWR_EN (R)	23	0x0	Bus Power/Clock Control Enable Does not apply to PCI Express. Hardwired to 0.
PMI_DATA (R)	31:24	0x0	Data

Power Management Status/Control Register

PCIE_CAP_LIST - R - 16 bits - AXCFG_Reg:0x58			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x10	Indicates the PCI Express® Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure. 10 = PCI Express capable
NEXT_PTR	15:8	0xa0	Next Capability Pointer -- The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.

The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 2.3 configuration space capability list.

PCIE_CAP - RW - 16 bits - AXCFG_Reg:0x5A			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	3:0	0x2	Indicates PCI-SIG defined PCI Express capability structure version number. 0=PCI Express Cap Version
DEVICE_TYPE (R)	7:4	0x0	Indicates the type of PCI Express logical device. 0=PCI Express Endpoint 1=Legacy PCI Express Endpoint 4=PCI Express Root Complex

PCIE_CAP - RW - 16 bits - AXCFG_Reg:0x5A			
Field Name	**Bits**	**Default**	**Description**
SLOT_IMPLEMENTED (R)	8	0x0	This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot.
INT_MESSAGE_NUM (R)	13:9	0x0	Interrupt Message Number.

The PCI Express Capabilities register identifies PCI Express device type and associated capabilities.

DEVICE_CAP - RW - 32 bits - AXCFG_Reg:0x5C			
Field Name	**Bits**	**Default**	**Description**
MAX_PAYLOAD_SUPPORT (R)	2:0	0x0	This field indicates the maximum payload size that the device can support for TLPs. 0=128B size
PHANTOM_FUNC (R)	4:3	0x0	This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers with the Tag identifier. 0=No Phantom Functions
EXTENDED_TAG (R)	5	0x1	This field indicates the maximum supported size of the Tag field as a Requester. 0=5 Bit Tag Supported 1=8 Bit Tag Supported
L0S_ACCEPTABLE_LATENCY (R)	8:6	0x0	This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state.
L1_ACCEPTABLE_LATENCY (R)	11:9	0x0	This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state.
ROLE_BASED_ERR_REPORTING (R)	15	0x0	This field indicates the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification 1.0a. 0=Role-Based Error Reporting Disabled 1=Role-Based Error Reporting Enabled
CAPTURED_SLOT_POWER_LIMIT (R)	25:18	0x0	(Upstream Ports only) In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.
CAPTURED_SLOT_POWER_SCALE (R)	27:26	0x0	Specifies the scale used for the Slot Power Limit Value.
FLR_CAPABLE (R)	28	0x0	This field indicates that a device is capable of initiating Function Level Resets.

The Device Capabilities register identifies PCI Express device specific capabilities.

DEVICE_CNTL - RW - 16 bits - AXCFG_Reg:0x60			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_EN	0	0x0	This bit controls reporting of correctable errors. Default value of this field is 0. 0=Disable 1=Enable
NON_FATAL_ERR_EN	1	0x0	This bit controls reporting of Non-fatal errors. Default value of this field is 0. 0=Disable 1=Enable
FATAL_ERR_EN	2	0x0	This bit controls reporting of Fatal errors. Default value of this field is 0. 0=Disable 1=Enable

DEVICE_CNTL - RW - 16 bits - AXCFG_Reg:0x60			
Field Name	**Bits**	**Default**	**Description**
USR_REPORT_EN	3	0x0	This bit enables reporting of Unsupported Requests when set. Default value of this field is 0. 0=Disable 1=Enable
RELAXED_ORD_EN	4	0x1	If this bit is set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. Default value of this bit is 1. 0=Disable 1=Enable
MAX_PAYLOAD_SIZE (R)	7:5	0x0	This field sets maximum TLP payload size for the device. Default value of this field is 000b. 0=128B size
EXTENDED_TAG_EN	8	0x0	When set, this bit enables a device to use an 8-bit Tag field as a requester. If the bit is cleared, the device is restricted to a 5-bit Tag field. Default value of this field is 0. 0=Disable 1=Enable
PHANTOM_FUNC_EN (R)	9	0x0	When set, this bit enables a device to use unclaimed functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is cleared, the device is not allowed to use Phantom Functions. 0=Disable 1=Enable
AUX_POWER_PM_EN (R)	10	0x0	This bit when set enables a device to draw AUX power independent of PME AUX power. 0=Disable 1=Enable
NO_SNOOP_EN	11	0x1	If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Default value of this bit is 1. 0=Disable 1=Enable
MAX_REQUEST_SIZE (R)	14:12	0x0	This field sets the maximum Read Request size for the Device as a Requester. Default value of this field is 010b. 0=128B size
BRIDGE_CFG_RETRY_EN (R)	15	0x0	This field enables PCI Express to PCI/PCI-X bridges to return Configuration Request Retry Status (CRS) in response to configuration requests that target devices below the bridge. 0=Disable 1=Enable

The Device Control register controls PCI Express device specific parameters.

DEVICE_STATUS - RW - 16 bits - AXCFG_Reg:0x62			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR	0	0x0	This bit indicates status of correctable errors detected.
NON_FATAL_ERR	1	0x0	This bit indicates status of Nonfatal errors detected.
FATAL_ERR	2	0x0	This bit indicates status of Fatal errors detected.
USR_DETECTED	3	0x0	This bit indicates that the device received an Unsupported Request.
AUX_PWR (R)	4	0x0	Devices that require AUX power report this bit as set if AUX power is detected by the device.

DEVICE_STATUS - RW - 16 bits - AXCFG_Reg:0x62			
Field Name	**Bits**	**Default**	**Description**
TRANSACTIONS_PEND (R)	5	0x0	Endpoints: This bit when set indicates that the device has issued Non-Posted Requests which have not been completed. Root and Switch Ports: This bit when set indicates that a Port has issued Non-Posted Requests on its own behalf (using the Port's own Requester ID) which have not been completed.

The Device Status register provides information about PCI Express device specific parameters.

LINK_CAP - RW - 32 bits - AXCFG_Reg:0x64			
Field Name	**Bits**	**Default**	**Description**
LINK_SPEED (R)	3:0	0x1	This field indicates the maximum Link speed of the given PCI Express Link. 1=2.5 Gb/s 2=5.0 Gb/s
LINK_WIDTH (R)	9:4	0x0	This field indicates the maximum width of the given PCI Express Link. 1=x1 2=x2 4=x4 8=x8 12=x12 16=x16 32=x32
PM_SUPPORT (R)	11:10	0x3	This field indicates the level of ASPM supported on the given PCI Express Link.
L0S_EXIT_LATENCY (R)	14:12	0x1	This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
L1_EXIT_LATENCY (R)	17:15	0x2	This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
CLOCK_POWER_MANAGEMENT (R)	18	0x0	This field indicates in the component tolerates removal of REFCLK via the CLKREQ# mechanism when the Link is in L1 and L23Ready.
SURPRISE_DOWN_ERR_REPORTING (R)	19	0x0	This field indicates if the component supports the detecting and reporting of a Surprise Down error condition.
DL_ACTIVE_REPORTING_CAPABLE (R)	20	0x0	This field indicates if the component supports the reporting of DL_Active state of the DLLSM.
LINK_BW_NOTIFICATION_CAP (R)	21	0x0	This field indicates if the component supports the Link Bandwidth Notification status and interrupt mechanisms.
PORT_NUMBER (R)	31:24	0x0	This field indicates the PCI Express Port number for the given PCI Express Link.

The Link Capabilities register identifies PCI Express Link specific capabilities.

LINK_CNTL - RW - 16 bits - AXCFG_Reg:0x68			
Field Name	**Bits**	**Default**	**Description**
PM_CONTROL	1:0	0x0	This field controls the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b Disabled 01b L0s Entry Enabled 10b L1 Entry Enabled 11b L0s and L1 Entry Enabled
READ_CPL_BOUNDARY (R)	3	0x0	Read Completion Boundary. Indicates the RCB value for the Root Port 0=64 Byte 1=128 Byte

LINK_CNTL - RW - 16 bits - AXCFG_Reg:0x68			
Field Name	**Bits**	**Default**	**Description**
LINK_DIS (R)	4	0x0	This bit disables the Link when set to 1b. Default value of this field is 0b.
RETRAIN_LINK (R)	5	0x0	A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. Reads of this bit always return 0b.
COMMON_CLOCK_CFG	6	0x0	This bit when set indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. Default value of this field is 0b.
EXTENDED_SYNC	7	0x0	This bit when set forces the transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set.
CLOCK_POWER_MANAGEMENT_EN	8	0x0	This bit determines if device is permitted to use CLKREQ# signal to power manage link clock.
HW_AUTONOMOUS_WIDTH_DISABLE	9	0x0	When set to 1, this bit disables hardware from changing the link width for reasons other than attempting to correct unreliable link operation by reducing link width.
LINK_BW_MANAGEMENT_INT_EN (R)	10	0x0	This bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set.
LINK_AUTONOMOUS_BW_INT_EN (R)	11	0x0	This bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set.

The Link Control register controls PCI Express Link specific parameters.

LINK_STATUS - RW - 16 bits - AXCFG_Reg:0x6A			
Field Name	**Bits**	**Default**	**Description**
CURRENT_LINK_SPEED (R)	3:0	0x1	Indicates the negotiated Link speed of the given PCI Express Link 1=2.5 Gb/s 2=5.0 Gb/s
NEGOTIATED_LINK_WIDTH (R)	9:4	0x0	This field indicates the negotiated width of the given PCI Express Link. Defined encodings are: 000001b X1 000010b X2 000100b X4 001000b X8 001100b X12 010000b X16 100000b X32 All other encodings are reserved. 1=x1 2=x2 4=x4 8=x8 12=x12 16=x16 32=x32
LINK_TRAINING (R)	11	0x0	This read-only bit indicates that Link training is in progress (Physical Layer LTSSM in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.

LINK_STATUS - RW - 16 bits - AXCFG_Reg:0x6A			
Field Name	**Bits**	**Default**	**Description**
SLOT_CLOCK_CFG (R)	12	0x1	This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be clear. 0=Diff Clock 1=Same Clock
DL_ACTIVE (R)	13	0x0	This bit indicates the status of the Data Link Control and Management State Machine. It returns 1b to indicate DL_Active state, 0b otherwise.
LINK_BW_MANAGEMENT_STATUS (R)	14	0x0	This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit. - Hardware has changed the Link speed of width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process.
LINK_AUTONOMOUS_BW_STATUS (R)	15	0x0	This bit is set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation.

The Link Status register provides information about PCI Express Link specific parameters.

DEVICE_CAP2 - RW - 32 bits - AXCFG_Reg:0x7C			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_RANGE_SUPPORTED (R)	3:0	0x0	PCIe® completion timeout range supported
CPL_TIMEOUT_DIS_SUPPORTED (R)	4	0x0	PCIe completion timeout disabled supported
ARI_FORWARDING_SUPPORTED (R)	5	0x0	ARI Forwarding supported

The Device Capabilities 2 register identifies PCI Express device specific capabilities.

DEVICE_CNTL2 - RW - 16 bits - AXCFG_Reg:0x80			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_VALUE	3:0	0x0	PCIe completion timeout value
CPL_TIMEOUT_DIS	4	0x0	Disable PCIe completion timeout
ARI_FORWARDING_EN (R)	5	0x0	ARI Forwarding enable

The Device Control 2 register controls PCI Express device specific parameters.

DEVICE_STATUS2 - RW - 16 bits - AXCFG_Reg:0x82			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	Reserved

The Device Status 2 register provides information about PCI Express device specific parameters.

LINK_CAP2 - RW - 32 bits - AXCFG_Reg:0x84			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	Reserved

LINK_CAP2 - RW - 32 bits - AXCFG_Reg:0x84			
Field Name	**Bits**	**Default**	**Description**

The Link Capabilities 2 register identifies PCI Express Link specific capabilities.

LINK_CNTL2 - RW - 16 bits - AXCFG_Reg:0x88			
Field Name	**Bits**	**Default**	**Description**
TARGET_LINK_SPEED	3:0	0x1	The upper limit on the operational speed. This field restricts the data rate values advertised by an upstream component.
ENTER_COMPLIANCE	4	0x0	This bit forces a port's transmitter to enter Compliance.
HW_AUTONOMOUS_SPEED_DISABLE	5	0x0	Controls the component's ability to autonomously direct changes in link speed.
SELECTABLE_DEEMPHASIS (R)	6	0x0	Selectable de-emphasis (in GEN 2 data rate) 0 : -6dB, 1 : -3.6dB
XMIT_MARGIN	9:7	0x0	These bits control the value of the non-deemphasized voltage level at the transmitter pins.
ENTER_MOD_COMPLIANCE	10	0x0	LTSSM transmits modified compliance pattern in Polling.Compliance if this bit is set to 1.
COMPLIANCE_SOS	11	0x0	When set to 1, the LTSSM is required to send SOS periodically in between the (modified) compliance patterns.
COMPLIANCE_DEEMPHASIS	12	0x0	This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the `enter compliance' bit being 1b. When the link is operating at 2.5 GT/s, the setting of this bit has no effect. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. 0=-6 dB 1=-3dB

The Link Control 2 register controls PCI Express Link specific parameters.

LINK_STATUS2 - RW - 16 bits - AXCFG_Reg:0x8A			
Field Name	**Bits**	**Default**	**Description**
CUR_DEEMPHASIS_LEVEL (R)	0	0x0	When the link is operating at 5GT/s speed, this bit reflects the level of de-emphasis.

The Link Status 2 register provides information about PCI Express Link specific parameters.

MSI_CAP_LIST - R - 16 bits - AXCFG_Reg:0xA0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x5	Register identifies if a device function is MSI capable
NEXT_PTR	15:8	0x0	Pointer to the next item on the capabilities list

Message Signaled Interrupt Capability Registers

MSI_MSG_CNTL - RW - 16 bits - AXCFG_Reg:0xA2			
Field Name	**Bits**	**Default**	**Description**
MSI_EN	0	0x0	Enable MSI messaging 0=Disable 1=Enable

MSI_MSG_CNTL - RW - 16 bits - AXCFG_Reg:0xA2			
Field Name	**Bits**	**Default**	**Description**
MSI_MULTI_CAP (R)	3:1	0x0	Multiple Message Capable register is read to determine the number of requested messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_MULTI_EN	6:4	0x0	Multiple Message Enable register is written to indicate the number of allocated messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_64BIT (R)	7	0x0	Signifies if a device function is capable of generating a 64-bit message address 0=Not capable of generating 1 64-bit message address 1=Capable of generating 1 64-bit message address

Message Signaled Interrupts Control Register

MSI_MSG_ADDR_LO - RW - 32 bits - AXCFG_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_LO	31:2	0x0	Message Lower Address - use lower 32-bits of address

Message Lower Address

MSI_MSG_ADDR_HI - RW - 32 bits - AXCFG_Reg:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_HI	31:0	0x0	Message Upper Address - use upper 32-bit of address

Message Upper Address

MSI_MSG_DATA_64 - RW - 16 bits - AXCFG_Reg:0xAC			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA_64	15:0	0x0	Message Data. System specified.

64-bit MSI Message Data

MSI_MSG_DATA - RW - 32 bits - AXCFG_Reg:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA	15:0	0x0	Message Data. System specified.

MSI Message Data

PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST - R - 32 bits – AXCFG_Reg:0x100			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xb	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.

PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST - R - 32 bits – AXCFG_Reg:0x100			
Field Name	**Bits**	**Default**	**Description**
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x110	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Vendor Specific Capability

PCIE_VENDOR_SPECIFIC_HDR - R - 32 bits - AXCFG_Reg:0x104			
Field Name	**Bits**	**Default**	**Description**
VSEC_ID	15:0	0x1	Vendor-defined ID number.
VSEC_REV	19:16	0x1	Vendor-defined revision number.
VSEC_LENGTH	31:20	0x10	Number of bytes in the entire VSEC structure.

Vendor Specific Header

PCIE_VENDOR_SPECIFIC1 - RW - 32 bits - AXCFG_Reg:0x108			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCIe® scratch register.

Vendor-Specific Scratch Register 1

PCIE_VENDOR_SPECIFIC2 - RW - 32 bits - AXCFG_Reg:0x10C			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCIe scratch register.

Vendor-Specific Scratch Register 2

PCIE_VC_ENH_CAP_LIST - R - 32 bits - AXCFG_Reg:0x110			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x2	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x140	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Virtual Channel Enhanced Capability Header

PCIE_PORT_VC_CAP_REG1 - R - 32 bits - AXCFG_Reg:0x114			
Field Name	**Bits**	**Default**	**Description**
EXT_VC_COUNT	2:0	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. This field is valid for all devices.
LOW_PRIORITY_EXT_VC_COUNT	6:4	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC group.
REF_CLK	9:8	0x0	Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration.
PORT_ARB_TABLE_ENTRY_SIZE	11:10	0x0	Indicates the size (in bits) of Port Arbitration table entry in the device.

Port VC Capability Register 1

PCIE_PORT_VC_CAP_REG2 - R - 32 bits - AXCFG_Reg:0x118			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_CAP	7:0	0x0	Indicates the types of VC Arbitration supported by the device for the Low Priority Virtual Channel group.
VC_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the VC Arbitration Table.

Port VC Capability Register 2

PCIE_PORT_VC_CNTL - RW - 16 bits - AXCFG_Reg:0x11C			
Field Name	**Bits**	**Default**	**Description**
LOAD_VC_ARB_TABLE (R)	0	0x0	Used for software to update the VC Arbitration Table.
VC_ARB_SELECT	3:1	0x0	Used for software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes.

Port VC Control Register

PCIE_PORT_VC_STATUS - R - 16 bits - AXCFG_Reg:0x11E			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the VC Arbitration Table

Port VC Status Register

PCIE_VC0_RESOURCE_CAP - R - 32 bits - AXCFG_Reg:0x120			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x0	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC.
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting.
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.

VC0 Resource Capability Register

PCIE_VC0_RESOURCE_CNTL - RW - 32 bits - AXCFG_Reg:0x124			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x1	This field indicates the TCs that are mapped to the VC resource.
TC_VC_MAP_TC1_7	7:1	0x7f	This field indicates the TCs that are mapped to the VC resource.
LOAD_PORT_ARB_TABLE (R)	16	0x0	This bit, when set, updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	This field configures the VC resource to provide a particular Port Arbitration service.
VC_ID (R)	26:24	0x0	This field assigns a VC ID to the VC resource.
VC_ENABLE (R)	31	0x1	This field, when set, enables a Virtual Channel.

VC0 Resource Control Register

PCIE_VC0_RESOURCE_STATUS - R - 16 bits - AXCFG_Reg:0x12A			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	This bit indicates the coherency status of the Port Arbitration Table associated with the VC resource.
VC_NEGOTIATION_PENDING	1	0x1	This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state.

VC0 Resource Status Register

PCIE_VC1_RESOURCE_CAP - R - 32 bits - AXCFG_Reg:0x12C			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC.
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting.
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.

VC1 Resource Capability Register

PCIE_VC1_RESOURCE_CNTL - RW - 32 bits - AXCFG_Reg:0x130			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x0	This field indicates the TCs that are mapped to the VC resource.
TC_VC_MAP_TC1_7	7:1	0x0	This field indicates the TCs that are mapped to the VC resource.
LOAD_PORT_ARB_TABLE (R)	16	0x0	This bit, when set, updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	This field configures the VC resource to provide a particular Port Arbitration service.
VC_ID	26:24	0x0	This field assigns a VC ID to the VC resource.
VC_ENABLE	31	0x0	This field, when set, enables a Virtual Channel.

VC1 Resource Control Register

PCIE_VC1_RESOURCE_STATUS - R - 16 bits - AXCFG_Reg:0x136			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	This bit indicates the coherency status of the Port Arbitration Table associated with the VC resource.
VC_NEGOTIATION_PENDING	1	0x1	This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state.

VC1 Resource Status Register

PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST - R - 32 bits - AXCFG_Reg:0x140			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x3	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x150	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Device Serial Number Enhanced Capability header

PCIE_DEV_SERIAL_NUM_DW1 - R - 32 bits - AXCFG_Reg:0x144			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_LO	31:0	0x0	Lower 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)

PCI-Express Device Serial Number (1st DW)

PCIE_DEV_SERIAL_NUM_DW2 - R - 32 bits - AXCFG_Reg:0x148			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_HI	31:0	0x0	Upper 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)

PCI-Express Device Serial Number (2nd DW)

PCIE_ADV_ERR_RPT_ENH_CAP_LIST - R - 32 bits - AXCFG_Reg:0x150			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x1	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x190	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Advanced Error Reporting Enhanced Capability header

PCIE_UNCORR_ERR_STATUS - RW - 32 bits - AXCFG_Reg:0x154			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_STATUS	4	0x0	Data Link Protocol Error Status
SURPDN_ERR_STATUS (R)	5	0x0	Surprise Down Error Status
PSN_ERR_STATUS	12	0x0	Poisoned TLP Status
FC_ERR_STATUS (R)	13	0x0	Flow Control Protocol Error Status
CPL_TIMEOUT_STATUS	14	0x0	Completion Timeout Status
CPL_ABORT_ERR_STATUS	15	0x0	Completer Abort Status
UNEXP_CPL_STATUS	16	0x0	Unexpected Completion Status
RCV_OVFL_STATUS (R)	17	0x0	Receiver Overflow Status
MAL_TLP_STATUS	18	0x0	Malformed TLP Status
ECRC_ERR_STATUS	19	0x0	ECRC Error Status
UNSUPP_REQ_ERR_STATUS	20	0x0	Unsupported Request Error Status
ACS_VIOLATION_STATUS	21	0x0	ACS Violation Error Status

The Uncorrectable Error Status register reports error status of individual error sources on a PCI Express device.

PCIE_UNCORR_ERR_MASK - RW - 32 bits – AXCFG_Reg:0x158			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_MASK	4	0x0	Data Link Protocol Error Mask
SURPDN_ERR_MASK (R)	5	0x0	Surprise Down Error Mask
PSN_ERR_MASK	12	0x0	Poisoned TLP Mask
FC_ERR_MASK (R)	13	0x0	Flow Control Protocol Error Mask
CPL_TIMEOUT_MASK	14	0x0	Completion Timeout Mask
CPL_ABORT_ERR_MASK	15	0x0	Completer Abort Mask
UNEXP_CPL_MASK	16	0x0	Unexpected Completion Mask

PCIE_UNCORR_ERR_MASK - RW - 32 bits – AXCFG_Reg:0x158			
Field Name	**Bits**	**Default**	**Description**
RCV_OVFL_MASK (R)	17	0x0	Receiver Overflow Mask
MAL_TLP_MASK	18	0x0	Malformed TLP Mask
ECRC_ERR_MASK	19	0x0	ECRC Error Mask
UNSUPP_REQ_ERR_MASK	20	0x0	Unsupported Request Error Mask
ACS_VIOLATION_MASK	21	0x0	ACS Violation Mask

The Uncorrectable Error Mask register controls reporting of individual errors by the device to the PCI Express Root Complex via a PCI Express error Message.

PCIE_UNCORR_ERR_SEVERITY - RW - 32 bits - AXCFG_Reg:0x15C			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_SEVERITY	4	0x1	Data Link Protocol Error Severity
SURPDN_ERR_SEVERITY (R)	5	0x1	Surprise Down Error Severity
PSN_ERR_SEVERITY	12	0x0	Poisoned TLP Severity
FC_ERR_SEVERITY (R)	13	0x1	Flow Control Protocol Error Severity
CPL_TIMEOUT_SEVERITY	14	0x0	Completion Timeout Error Severity
CPL_ABORT_ERR_SEVERITY	15	0x0	Completer Abort Error Severity
UNEXP_CPL_SEVERITY	16	0x0	Unexpected Completion Error Severity
RCV_OVFL_SEVERITY (R)	17	0x1	Receiver Overflow Error Severity
MAL_TLP_SEVERITY	18	0x1	Malformed TLP Severity
ECRC_ERR_SEVERITY	19	0x0	ECRC Error Severity
UNSUPP_REQ_ERR_SEVERITY	20	0x0	Unsupported Request Error Severity
ACS_VIOLATION_SEVERITY	21	0x0	ACS Violation Severity

The Uncorrectable Error Severity register controls whether an individual error is reported as a Nonfatal or Fatal error.

PCIE_CORR_ERR_STATUS - RW - 32 bits - AXCFG_Reg:0x160			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_STATUS (R)	0	0x0	Receiver Error Status
BAD_TLP_STATUS	6	0x0	Bad TLP Status
BAD_DLLP_STATUS	7	0x0	Bad DLLP Status
REPLAY_NUM_ROLLOVER_STATUS	8	0x0	REPLAY_NUM Rollover Status
REPLAY_TIMER_TIMEOUT_STATUS	12	0x0	Replay Timer Timeout Status
ADVISORY_NONFATAL_ERR_STATUS	13	0x0	Advisory Non-Fatal Status

The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device.

PCIE_CORR_ERR_MASK - RW - 32 bits - AXCFG_Reg:0x164			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_MASK (R)	0	0x0	Receiver Error Mask
BAD_TLP_MASK	6	0x0	Bad TLP Mask
BAD_DLLP_MASK	7	0x0	Bad DLLP Mask
REPLAY_NUM_ROLLOVER_MASK	8	0x0	REPLAY_NUM Rollover Mask

PCIE_CORR_ERR_MASK - RW - 32 bits - AXCFG_Reg:0x164			
Field Name	**Bits**	**Default**	**Description**
REPLAY_TIMER_TIMEOUT_MASK	12	0x0	Replay Timer Timeout Mask
ADVISORY_NONFATAL_ERR_MASK	13	0x1	Advisory Non-Fatal Mask

The Correctable Error Mask register controls reporting of individual correctable errors by device to the PCI Express Root Complex via a PCI Express error Message.

PCIE_ADV_ERR_CAP_CNTL - RW - 32 bits - AXCFG_Reg:0x168			
Field Name	**Bits**	**Default**	**Description**
FIRST_ERR_PTR (R)	4:0	0x0	The First Error Pointer is a read-only register that identifies the bit position of the first error reported in the Uncorrectable Error Status register.
ECRC_GEN_CAP (R)	5	0x0	This bit indicates that the device is capable of generating ECRC.
ECRC_GEN_EN	6	0x0	This bit when set enables ECRC generation. Default value of this field is 0.
ECRC_CHECK_CAP (R)	7	0x0	This bit indicates that the device is capable of checking ECRC.
ECRC_CHECK_EN	8	0x0	This bit when set enables ECRC checking. Default value of this field is 0.

Advanced Error Capabilities and Control Register

PCIE_HDR_LOG0 - R - 32 bits - AXCFG_Reg:0x16C			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 1st DW

Header Log Register captures the Header for the TLP corresponding to a detected error;

PCIE_HDR_LOG1 - R - 32 bits - AXCFG_Reg:0x170			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 2nd DW

Header Log Register

PCIE_HDR_LOG2 - R - 32 bits - AXCFG_Reg:0x174			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 3rd DW

Header Log Register

PCIE_HDR_LOG3 - R - 32 bits - AXCFG_Reg:0x178			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 4th DW

Header Log Register

PCIE_ACS_ENH_CAP_LIST - R - 32 bits - AXCFG_Reg:0x190			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xd	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.

PCIE_ACS_ENH_CAP_LIST - R - 32 bits - AXCFG_Reg:0x190			
Field Name	**Bits**	**Default**	**Description**
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x0	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

ACS Enhanced Capability header

PCIE_ACS_CAP - R - 16 bits - AXCFG_Reg:0x194			
Field Name	**Bits**	**Default**	**Description**
SOURCE_VALIDATION	0	0x0	When set, it indicates that the component implements ACS Source Validation.
TRANSLATION_BLOCKING	1	0x0	When set, it indicates that the component implements ACS Translation Blocking.
P2P_REQUEST_REDIRECT	2	0x0	When set, it indicates that the component implements ACS P2P Request Redirect.
P2P_COMPLETION_REDIRECT	3	0x0	When set, it indicates that the component implements ACS P2P Completion Redirect.
UPSTREAM_FORWARDING	4	0x0	When set, it indicates that the component implements ACS Upstream Forwarding.
P2P_EGRESS_CONTROL	5	0x0	When set, it indicates that the component implements ACS P2P Egress Control.
DIRECT_TRANSLATED_P2P	6	0x0	When set, it indicates that the component implements ACS Direct Translated P2P.
EGRESS_CONTROL_VECTOR_SIZE	15:8	0x0	Encodings 01h-FFh directly indicate the number of applicable bits in the Egress Control Vector; the encoding 00h indicates 256 bits.

ACS Capability register

PCIE_ACS_CNTL - RW - 16 bits - AXCFG_Reg:0x196			
Field Name	**Bits**	**Default**	**Description**
SOURCE_VALIDATION_EN	0	0x0	When set, the component validates the Bus Number from the Requester ID of Upstream Requests against the secondary / subordinate Bus Numbers.
TRANSLATION_BLOCKING_EN	1	0x0	When set, the component blocks all Upstream Memory Requests whose Address Translation field is not set to the default value.
P2P_REQUEST_REDIRECT_EN	2	0x0	In conjunction with ACS P2P Egress Control and ACS Direct Translated P2P mechanisms, determines when the component redirects P2P Requests Upstream.
P2P_COMPLETION_REDIRECT_EN	3	0x0	Determines when the component redirects P2P Completions Upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
UPSTREAM_FORWARDING_EN	4	0x0	When set, the component forwards Upstream any Request or Completion TLPs it receives that were redirected Upstream by a component lower in the hierarchy.
P2P_EGRESS_CONTROL_EN (R)	5	0x0	In conjunction with the Egress Control Vector plus the ACS P2P Request Redirect and ACS Direct Translated P2P mechanisms, determines when to allow, disallow, or redirect P2P Requests.

PCIE_ACS_CNTL - RW - 16 bits - AXCFG_Reg:0x196			
Field Name	**Bits**	**Default**	**Description**
DIRECT_TRANSLATED_P2P_EN	6	0x0	When set, overrides the ACS P2P Request Redirect and ACS P2P Egress Control mechanisms with P2P Memory Requests whose Address Translation field indicates a Translated address.

ACS Control register

4.2.3 AXINDC Registers

AXINDC are the indirect access registers to control the UMI link core registers. AXINDC is the register block for the common control registers.

Accessing AXINDC requires a second level of indirect procedures. Registers in these spaces are addressed through registers AX_INDXC/AX_DATAC.

Register Name	Address Offset
AX_INDXC	30h
AX_DATAC	34h

AX_INDXC – RW – 32 bits – [RegSpace:000b, RegAddr: 30h]			
Field Name	**Bits**	**Default**	**Description**
Register Address	7:0	00h	
Reserved	31:8	000000h	Reserved

AX_DATAC – RW – 32 bits – [RegSpace:000b, RegAddr: 34h]			
Field Name	**Bits**	**Default**	**Description**
Data	31:0	00000000h	

To access an AXINDC register, the register address is first written to AX_INDXC with RegSpace=”000b” (AB_INDX[31:29]) and offset 30h. The specified AXINDC register is then accessed through a read or a write to AX_DATAC with RegSpace=”000b” (AB_INDX[31:29]) and offset 34h. However, AX_INDXC and AX_DATAC cannot be addressed directly, but are rather addressed through AB_INDX/AB_DATA. As a result, there are two levels of indirect procedures involved in accessing the AXINDC registers. A programming example is provided below to illustrate this.

Example: Read AXINDC:10h to TMP

```
OUT AB_INDX, 00000030h     // Set AB_INDX RegSpace=000, RegAddr=30h.
OUT AB_DATA, 00000010h     // Set AX_INDXC to 00000010h through AB_DATA.
OUT AB_INDX, 00000034h     // Set AB_INDX RegSpace=000, RegAddr=34h.
IN  AB_DATA, TMP           // Read AXINDC:10h through AB_DATA.
```

Register Name	Address Offset
PCIE_RESERVED	00h
PCIE_SCRATCH	01h
PCIE_HW_DEBUG	02h
PCIE_RX_NUM_NAK	0Eh
PCIE_RX_NUM_NAK_GENERATED	0Fh
PCIE_CNTL	10h
PCIE_CONFIG_CNTL	11h
PCIE_DEBUG_CNTL	12h
PCIE_RTR_CPL_TIMEOUT_STATUS	13h
PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL	14h
PCIE_CI_MST_R_RTR_TIMEOUT_CNTL	15h
PCIE_CI_MST_C_RTR_TIMEOUT_CNTL	16h
PCIE_REG_R_RTR_TIMEOUT_CNTL	17h
PCIE_TX_SLVCPL_TIMEOUT_CNTL	18h
PCIE_INT_CNTL	1Ah
PCIE_INT_STATUS	1Bh
PCIE_CNTL2	1Ch
PCIE_CI_CNTL	20h
PCIE_BUS_CNTL	21h
PCIE_LC_STATE6	22h
PCIE_LC_STATE7	23h
PCIE_LC_STATE8	24h
PCIE_LC_STATE9	25h
PCIE_LC_STATE10	26h
PCIE_LC_STATE11	27h
PCIE_LC_STATUS1	28h
PCIE_LC_STATUS2	29h
PCIE_WPR_CNTL	30h
PCIE_RX_LAST_TLP0	31h
PCIE_RX_LAST_TLP1	32h
PCIE_RX_LAST_TLP2	33h
PCIE_RX_LAST_TLP3	34h
PCIE_TX_LAST_TLP0	35h
PCIE_TX_LAST_TLP1	36h
PCIE_TX_LAST_TLP2	37h
PCIE_TX_LAST_TLP3	38h
PCIE_I2C_DEBUG_BUS	39h
PCIE_I2C_REG_ADDR_EXPAND	3Ah
PCIE_I2C_REG_DATA	3Bh
PCIE_CFG_CNTL	3Ch
PCIE_P_CNTL	40h
PCIE_P_BUF_STATUS	41h
PCIE_P_DECODER_STATUS	42h
PCIE_P_MISC_STATUS	43h
PCIE_P_PLL_CNTL	44h
PCIE_P_RCV_L0S_FTS_DET	50h
PCIE_P_IMP_CNTL_STRENGTH	60h
PCIE_P_IMP_CNTL_UPDATE	61h
PCIE_P_STR_CNTL_UPDATE	62h
PCIE_P_PAD_MISC_CNTL	63h
PCIE_P_PAD_FORCE_EN	64h
PCIE_P_PAD_FORCE_DIS	65h
PCIE_PERF_COUNT_CNTL	80h

Register Name	Address Offset
PCIE_PERF_CNTL_TXCLK	81h
PCIE_PERF_COUNT0_TXCLK	82h
PCIE_PERF_COUNT1_TXCLK	83h
PCIE_PERF_CNTL_MST_R_CLK	84h
PCIE_PERF_COUNT0_MST_R_CLK	85h
PCIE_PERF_COUNT1_MST_R_CLK	86h
PCIE_PERF_CNTL_MST_C_CLK	87h
PCIE_PERF_COUNT0_MST_C_CLK	88h
PCIE_PERF_COUNT1_MST_C_CLK	89h
PCIE_PERF_CNTL_SLV_R_CLK	8Ah
PCIE_PERF_COUNT0_SLV_R_CLK	8Bh
PCIE_PERF_COUNT1_SLV_R_CLK	8Ch
PCIE_PERF_CNTL_SLV_S_C_CLK	8Dh
PCIE_PERF_COUNT0_SLV_S_C_CLK	8Eh
PCIE_PERF_COUNT1_SLV_S_C_CLK	8Fh
PCIE_PERF_CNTL_SLV_NS_C_CLK	90h
PCIE_PERF_COUNT0_SLV_NS_C_CLK	91h
PCIE_PERF_COUNT1_SLV_NS_C_CLK	92h
PCIE_PERF_CNTL_EVENT0_PORT_SEL	93h
PCIE_PERF_CNTL_EVENT1_PORT_SEL	94h
PCIE_PERF_CNTL_TXCLK2	95h
PCIE_PERF_COUNT0_TXCLK2	96h
PCIE_PERF_COUNT1_TXCLK2	97h
PCIE_PERF_MAS_ACC_START_LO	A0h
PCIE_PERF_MAS_ACC_END_LO	A1h
PCIE_PERF_MAS_ACC_START_END_HI	A2h
PCIE_PERF_SLV_ACC_LO	A3h
PCIE_PERF_SLV_ACC_HI	A4h
PCIE_STRAP_MISC	C0h
PCIE_STRAP_MISC2	C1h
PCIE_STRAP_PI	C2h
PCIE_B_P90_CNTL	C3h
PCIE_STRAP_I2C_BD	C4h
PCIE_P90RX_PRBS10_CNTL	C6h
PCIE_P90_BRX_PRBS10_ER	C7h
PCIE_PRBS_CLR	C8h
PCIE_PRBS_STATUS1	C9h
PCIE_PRBS_STATUS2	CAh
PCIE_PRBS_FREERUN	CBh
PCIE_PRBS_MISC	CCh
PCIE_PRBS_USER_PATTERN	CDh
PCIE_PRBS_LO_BITCNT	CEh
PCIE_PRBS_HI_BITCNT	CFh
PCIE_PRBS_ERRCNT_0	D0h
PCIE_PRBS_ERRCNT_1	D1h
PCIE_PRBS_ERRCNT_2	D2h
PCIE_PRBS_ERRCNT_3	D3h
PCIE_PRBS_ERRCNT_4	D4h
PCIE_PRBS_ERRCNT_5	D5h
PCIE_PRBS_ERRCNT_6	D6h
PCIE_PRBS_ERRCNT_7	D7h
PCIE_PRBS_ERRCNT_8	D8h
PCIE_PRBS_ERRCNT_9	D9h

Register Name	Address Offset
PCIE_PRBS_ERRCNT_10	DAh
PCIE_PRBS_ERRCNT_11	DBh
PCIE_PRBS_ERRCNT_12	DCh
PCIE_PRBS_ERRCNT_13	DDh
PCIE_PRBS_ERRCNT_14	DEh
PCIE_PRBS_ERRCNT_15	DFh

PCIE_RESERVED - R - 32 bits - AXINDC_Reg:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIE_RESERVED	31:0	0xffffffff	RESERVED

Reserved

PCIE_SCRATCH - RW - 32 bits - AXINDC_Reg:0x1			
Field Name	**Bits**	**Default**	**Description**
PCIE_SCRATCH	31:0	0x0	Software test register.

Software test register

PCIE_HW_DEBUG - RW - 32 bits - AXINDC_Reg:0x2			
Field Name	**Bits**	**Default**	**Description**
HW_00_DEBUG	0	0x0	Ignore DLLPs during L1 so that TXCLK can be turned off.
HW_01_DEBUG	1	0x0	bit1
HW_02_DEBUG	2	0x0	bit2
HW_03_DEBUG	3	0x0	Used to enable the PLL power down when all lanes are inactive. It should be on in GPP.
HW_04_DEBUG	4	0x0	Bit4
HW_05_DEBUG	5	0x0	Bit5
HW_06_DEBUG	6	0x0	Bit6
HW_07_DEBUG	7	0x0	Bit7
HW_08_DEBUG	8	0x0	Turns on the BUG fix for the race problem between LC wakeup from L1 and PLL calibration in GEN2.
HW_09_DEBUG	9	0x0	Bit9
HW_10_DEBUG	10	0x0	Bit10
HW_11_DEBUG	11	0x0	Bit11
HW_12_DEBUG	12	0x0	Bit12
HW_13_DEBUG	13	0x0	Bit13
HW_14_DEBUG	14	0x0	Bit14
HW_15_DEBUG	15	0x0	Selects between chip power state (1) and software power state (0).

Hardware debug register

PCIE_RX_NUM_NAK - R - 32 bits - AXINDC_Reg:0xE			
Field Name	**Bits**	**Default**	**Description**
RX_NUM_NAK	31:0	0x0	Total number of naks received

Num naks received

PCIE_RX_NUM_NAK_GENERATED - R - 32 bits - AXINDC_Reg:0xF			
Field Name	**Bits**	**Default**	**Description**
RX_NUM_NAK_GENERATED	31:0	0x0	Total number of naks generated

Num naks generated

PCIE_CNTL - RW - 32 bits - AXINDC_Reg:0x10			
Field Name	**Bits**	**Default**	**Description**
HWINIT_WR_LOCK	0	0x0	Hardware write lock 0=HWInit registers unlocked 1=Lock HWInit registers
UR_ERR_REPORT_DIS	7	0x0	UR error reporting disable for TX
PCIE_HT_NP_MEM_WRITE	9	0x0	Memory write mapping enable
RX_FCH_ADJ_PAYLOAD_SIZE	12:10	0x2	FCH payload size 2=16 bytes 3=32 bytes 4=64 bytes
RX_RCB_REORDER_EN	16	0x1	RCB ordering enable 0=No re-ordering 1=Re-ordering
RX_RCB_INVALID_SIZE_DIS	17	0x1	RCB invalid size disable
RX_RCB_UNEXP_CPL_DIS	18	0x0	RCB unexpected cpl disable
RX_RCB_CPL_TIMEOUT_TEST_MODE	19	0x0	RCB cpl timeout test mode
Reserved	20	-	
RX_RCB_WRONG_ATTR_DIS	21	0x1	RCB invalid attributes check for received completions disable
RX_RCB_WRONG_FUNCNUM_DIS	22	0x1	RCB invalid function number check for received completions disable
LC_PREVENT_SPD_CHG_OVERLAP	23	0x1	Don't allow two speed change requests in opposite directions during the same clock cycle.
TX_CPL_DEBUG	29:24	0x0	CPL debug
RX_CPL_POSTED_REQ_ORD_EN	31	0x0	CPL request ordering enable 0=Disable RX request ordering 1=Enable RX request ordering

PCIExpress control register

PCIE_CONFIG_CNTL - RW - 32 bits - AXINDC_Reg:0x11			
Field Name	**Bits**	**Default**	**Description**
DYN_CLK_LATENCY	3:0	0x7	Dynamic Clock Latency

PCIExpress Configuration Control Register

PCIE_DEBUG_CNTL - RW - 32 bits - AXINDC_Reg:0x12			
Field Name	**Bits**	**Default**	**Description**
DEBUG_PORT_EN	7:0	0x1	Debug Bus Port Enable 1=port A 2=port B 4=port C 8=port D 16=port E 32=port F 64=port G 128=port H

PCIE_DEBUG_CNTL - RW - 32 bits - AXINDC_Reg:0x12			
Field Name	**Bits**	**Default**	**Description**
DEBUG_SELECT	8	0x0	Debug Bus Select - for additional muxing (e.g. VC0 vs. VC1)
DEBUG_LANE_EN	31:16	0x1	Debug Lane Enable : lane0=1, lane1=2, lane2=4, lane3=8, lane4=16, lane5=32, lane6=64, lane7=128, lane8=256, lane9=512, lane10=1024, lane11=2048, lane12=4096, lane13=8192, lane14=16384, lane15=32768

Debug Bus Control Register

PCIE_RTR_CPL_TIMEOUT_STATUS - RW - 32 bits - AXINDC_Reg:0x13			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_R_RTR_ERROR	0	0x0	Slave req interface - 1 indicates slv RTR was de-asserted for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1.
CI_MST_R_RTR_ERRO R	1	0x0	Master req interface - 1 indicates mst req RTR was de-asserted for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1.
CI_MST_C_RTR_ERRO R	2	0x0	Master completion interface - 1 indicates mst cpl RTR was de-asserted for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1.
REG_R_RTR_ERROR	3	0x0	Register req interface - 1 indicates reg req RTR was de-asserted for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1.
TX_SLVCPL_TIMEOUT_ ERROR	4	0x0	Slave completion interface - 1 indicates slv cpl hasn't been received for more than the # of cycles programmed in the CNTL register. This bit remains asserted until it is cleared by writing a 1. For RC this bit is for the Snoop channel.
CI_SLV_R_RTR_STATU S (R)	16	0x0	For testability only. The bit is set when CI_SLV_R interface RTR is deasserted for the programmed number of clock cycles.
CI_MST_R_RTR_STATU S (R)	17	0x0	For testability only. The bit is set when CI_MST_R interface RTR is deasserted for the programmed number of clock cycles.
CI_MST_C_RTR_STATU S (R)	18	0x0	For testability only. The bit is set when CI_MST_C interface RTR is deasserted for the programmed number of clock cycles.
REG_R_RTR_STATUS (R)	19	0x0	For testability only. The bit is set when REG_R interface RTR is deasserted for the programmed number of clock cycles.
TX_SLVCPL_TIMEOUT_ STATUS (R)	20	0x0	The bit is set when the slave completions (snoop) are not received during the programmed timeout.
TX_SLVCPL_NS_TIMEO UT_STATUS (R)	21	0x0	The bit is set when the slave completions (non-snoop) are not received during the programmed timeout.

Status register for rtr/cpl timeout

PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL - RW - 32 bits - AXINDC_Reg:0x14			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_R_RTR_TIMEO UT_RST (W)	0	0x0	Writing a 1 to this bit resets the slv req RTR timer.

PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL - RW - 32 bits - AXINDC_Reg:0x14			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in SLV_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1).

Control register for slave request RTR timeout

PCIE_CI_MST_R_RTR_TIMEOUT_CNTL - RW - 32 bits - AXINDC_Reg:0x15			
Field Name	**Bits**	**Default**	**Description**
CI_MST_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the master req RTR timer
CI_MST_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in MST_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1).

Control register for master request RTR timeout

PCIE_CI_MST_C_RTR_TIMEOUT_CNTL - RW - 32 bits - AXINDC_Reg:0x16			
Field Name	**Bits**	**Default**	**Description**
CI_MST_C_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the master cpl RTR timer.
CI_MST_C_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in MST_C_CLK) how long the RTR must be de-asserted before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1).

Control register for master completion RTR timeout

PCIE_REG_R_RTR_TIMEOUT_CNTL - RW - 32 bits - AXINDC_Reg:0x17			
Field Name	**Bits**	**Default**	**Description**
REG_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the register req RTR timer.
REG_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in REG_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1).

Control register for register request RTR timeout

PCIE_TX_SLVCPL_TIMEOUT_CNTL - RW - 32 bits - AXINDC_Reg:0x18			
Field Name	**Bits**	**Default**	**Description**
TX_SLVCPL_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slave cpl timer.
TX_SLVCPL_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in SLV_C_CLK/SLV_S_CCLK) how long to wait for cpl before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1).

Control register for slave completion timeout - snoop channel for RC

PCIE_INT_CNTL - RW - 32 bits - AXINDC_Reg:0x1A			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_INT_EN	0	0x0	Enable correctable error interrupt generation - corr error must be enabled through pcie cfg.

PCIE_INT_CNTL - RW - 32 bits - AXINDC_Reg:0x1A			
Field Name	**Bits**	**Default**	**Description**
NON_FATAL_ERR_INT_EN	1	0x0	Enable non-fatal error interrupt generation - non-fatal error must be enabled through pcie cfg.
FATAL_ERR_INT_EN	2	0x0	Enable fatal error interrupt generation - fatal error must be enabled through pcie cfg.
USR_DETECTED_INT_EN	3	0x0	Enable usr detected interrupt generation - usr detection must be enabled through pcie cfg.
MISC_ERR_INT_EN	4	0x0	Enable misc error interrupt generation.
SLOT_POWER_CHG_INT_EN	5	0x0	Enable slot power change interrupt generation.
POWER_STATE_CHG_INT_EN	6	0x0	Enable power state change interrupt generation.
LINK_BW_INT_EN	7	0x0	Enable link BW interrupt generation.

Interrupt Control

PCIE_INT_STATUS - RW - 32 bits - AXINDC_Reg:0x1B			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_INT_STATUS (R)	0	0x0	Correctable error interrupt - to disable interrupt, write 1 to DEVICE_STATUS.CORR_ERR.
NON_FATAL_ERR_INT_STATUS (R)	1	0x0	Non-fatal error interrupt - to disable interrupt, write 1 to DEVICE_STATUS.NON_FATAL_ERR.
FATAL_ERR_INT_STATUS (R)	2	0x0	Fatal error interrupt - to disable interrupt, write 1 to DEVICE_STATUS.FATAL_ERR.
USR_DETECTED_INT_STATUS (R)	3	0x0	USR detected interrupt - to disable interrupt, write 1 to DEVICE_STATUS.USER_DETECTED.
MISC_ERR_INT_STATUS (R)	4	0x0	Misc error interrupt - to disable interrupt, write 1 to the RW1C fields in PCIE_RTR_CPL_TIMEOUT_STATUS or PCIE_TX_CREDITS_STATUS.
SLOT_POWER_CHG_INT_STATUS	5	0x0	Slot power changed interrupt - to disable interrupt write 1 to this field.
POWER_STATE_CHG_INT_STATUS	6	0x0	Power State Change interrupt - to disable interrupt write 1 to this field.
LINK_BW_INT_STATUS	7	0x0	Link BW interrupt - to disable interrupt write 1 to this field.

Interrupt Status

PCIE_CNTL2 - RW - 32 bits - AXINDC_Reg:0x1C			
Field Name	**Bits**	**Default**	**Description**
TX_ARB_ROUND_ROBIN_EN (R)	0	0x0	TX round-robin arbitration enabled - for RC only
TX_ARB_SLV_LIMIT (R)	5:1	0x0	TX slave arbitration limit
TX_ARB_MST_LIMIT (R)	10:6	0x0	TX master arbitration limit

PCIExpress control register2

PCIE_CI_CNTL - RW - 32 bits - AXINDC_Reg:0x20			
Field Name	**Bits**	**Default**	**Description**
CI_SLAVE_SPLIT_MODE	2	0x0	0=RC - Full completions from Channel A or B 1=RC - Completions split on Channel A and B evenly
CI_SLAVE_GEN_USR_DIS	3	0x0	Sends USR for invalid addresses 0=Sends USR for invalid addresses 1=Disables slave from sending USR, and instead sends a successful CMPLT_D with dummy data.
CI_MST_CMPL_DUMMY_DATA	4	0x1	0xDEADBEEF or 0xFFFFFFFF 0=0xDEADBEEF 1=0xFFFFFFFF

PCIE_CI_CNTL - RW - 32 bits - AXINDC_Reg:0x20			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_RC_RD_REQ_SIZE	7:6	0x1	Slave read requests supported size to client. 0=32/64 byte requests supported 1=64 byte requests only 2=16/32/64
CI_SLV_ORDERING_DIS	8	0x0	Disable slave ordering logic 0=Enable slave ordering logic 1=Disable slave ordering logic
CI_RC_ORDERING_DIS	9	0x0	Disable RC ordering logic 0=Enable RC ordering logic 1=Disable RC ordering logic
CI_SLV_CPL_ALLOC_DIS	10	0x0	Slave CPL buffer is sub-divided or not 0=Slave CPL buffer is sub-divided between ports based on number of lanes active 1=Slave CPL buffer is not sub-divided
CI_SLV_CPL_ALLOC_MODE (R)	11	0x0	Slave Cpl buffer method for sub-division. 0 - dynamic, 1 - register limits CI_SLV_CPL_STATIC_ALLOC_LIMIT_(N)S
TX_SLV_CPL_DELAY_EN (R)	13	0x0	Enable Delay on Slave Completion Data path. RC only
TX_SLV_CPL_DELAY_TIMER (R)	23:14	0x0	Delay timeout. Effective delay = 7 * TIMER * SLV_S_C_CLK_period
CI_SLV_REQ_DELAY_EN (R)	24	0x0	Enable Delay on Slave Request path
CI_SLV_REQ_DELAY_TIMER (R)	30:25	0x0	Delay timeout. Effective delay = 4 * TIMER * SLV_R_CLK_period

Chip Interface Control Register

PCIE_BUS_CNTL - RW - 32 bits - AXINDC_Reg:0x21			
Field Name	**Bits**	**Default**	**Description**
BUS_DBL_RESYNC	0	0x1	Double flop the sync module. 0=Normal 1=Add extra resynchronizing clock
PMI_INT_DIS	6	0x0	PMI Interrupt Disable 0=Normal 1=Disable
IMMEDIATE_PMI_DIS	7	0x0	Immediate PMI Disable 0=Enable 1=Disable

PCI Express Bus Control Register

PCIE_LC_STATE6 - R - 32 bits - AXINDC_Reg:0x22			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE24	5:0	0x0	24th previous state
LC_PREV_STATE25	13:8	0x0	25th previous state
LC_PREV_STATE26	21:16	0x0	26th previous state
LC_PREV_STATE27	29:24	0x0	27th previous state

Link Control State Registers

PCIE_LC_STATE7 - R - 32 bits - AXINDC_Reg:0x23			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE28	5:0	0x0	28th previous state
LC_PREV_STATE29	13:8	0x0	29th previous state
LC_PREV_STATE30	21:16	0x0	30th previous state
LC_PREV_STATE31	29:24	0x0	31st previous state

Link Control State Registers

PCIE_LC_STATE8 - R - 32 bits - AXINDC_Reg:0x24			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE32	5:0	0x0	32nd previous state
LC_PREV_STATE33	13:8	0x0	33rd previous state
LC_PREV_STATE34	21:16	0x0	34th previous state
LC_PREV_STATE35	29:24	0x0	35th previous state

Link Control State Registers

PCIE_LC_STATE9 - R - 32 bits - AXINDC_Reg:0x25			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE36	5:0	0x0	36th previous state
LC_PREV_STATE37	13:8	0x0	37th previous state
LC_PREV_STATE38	21:16	0x0	38th previous state
LC_PREV_STATE39	29:24	0x0	39th previous state

Link Control State Registers

PCIE_LC_STATE10 - R - 32 bits - AXINDC_Reg:0x26			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE40	5:0	0x0	40th previous state
LC_PREV_STATE41	13:8	0x0	41st previous state
LC_PREV_STATE42	21:16	0x0	42nd previous state
LC_PREV_STATE43	29:24	0x0	43rd previous state

Link Control State Registers

PCIE_LC_STATE11 - R - 32 bits - AXINDC_Reg:0x27			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE44	5:0	0x0	44th previous state
LC_PREV_STATE45	13:8	0x0	45th previous state
LC_PREV_STATE46	21:16	0x0	46th previous state
LC_PREV_STATE47	29:24	0x0	47th previous state

Link Control State Registers

PCIE_LC_STATUS1 - R - 32 bits - AXINDC_Reg:0x28			
Field Name	**Bits**	**Default**	**Description**
LC_REVERSE_RCVR	0	0x0	Receiver reversal status. When asserted, received data is reversed (i.e. logical lane 0 is not received on physical lane 0).
LC_REVERSE_XMIT	1	0x0	Transmitter reversal status. When asserted, transmitted data is reversed (i.e. logical lane 0 is not transmitted on physical lane 0).
LC_OPERATING_LINK_WIDTH	4:2	0x0	Current width of the Link.
LC_DETECTED_LINK_WIDTH	7:5	0x0	Detected width of the Link. This identifies the maximum possible link width that is physically allowed.

Link Control Status Register 1

PCIE_LC_STATUS2 - R - 32 bits - AXINDC_Reg:0x29			
Field Name	**Bits**	**Default**	**Description**
LC_TOTAL_INACTIVE_LANES	15:0	0x0	Lanes that are not being used.

PCIE_LC_STATUS2 - R - 32 bits - AXINDC_Reg:0x29			
Field Name	**Bits**	**Default**	**Description**
LC_TURN_ON_LANE	31:16	0x0	Lanes that are available for link width negotiation. Not all available lanes will always be used (actual number depends on lanes supported by other end of the link).

Link Control Status Register 2

PCIE_WPR_CNTL - RW - 32 bits - AXINDC_Reg:0x30			
Field Name	**Bits**	**Default**	**Description**
WPR_RESET_HOT_RST_EN	0	0x1	Enable Hot Reset feature.
WPR_RESET_LNK_DWN_EN	1	0x0	Enable Link down reset feature.
WPR_RESET_LNK_DIS_EN	2	0x1	Enable Link disable reset feature.
WPR_RESET_COR_EN	3	0x0	Enable external CORE reset feature.
WPR_RESET_REG_EN	4	0x0	Enable external REGISTER reset feature.
WPR_RESET_STY_EN	5	0x0	Enable external Stickybit Register reset feature.
WPR_RESET_PHY_EN	6	0x0	Enable external PHY reset feature.

WPR Control Register

PCIE_RX_LAST_TLP0 - R - 32 bits - AXINDC_Reg:0x31			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP0	31:0	0x0	Bits 31:0

Last received TLP

PCIE_RX_LAST_TLP1 - R - 32 bits - AXINDC_Reg:0x32			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP1	31:0	0x0	Bits 63:32

Last received TLP

PCIE_RX_LAST_TLP2 - R - 32 bits - AXINDC_Reg:0x33			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP2	31:0	0x0	Bits 95:64

Last received TLP

PCIE_RX_LAST_TLP3 - R - 32 bits - AXINDC_Reg:0x34			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP3	31:0	0x0	Bits 127:96

Last received TLP

PCIE_TX_LAST_TLP0 - R - 32 bits - AXINDC_Reg:0x35			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP0	31:0	0x0	Bits 31:0

Last transmitted TLP

PCIE_TX_LAST_TLP1 - R - 32 bits - AXINDC_Reg:0x36			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP1	31:0	0x0	Bits 63:32

Last transmitted TLP

PCIE_TX_LAST_TLP2 - R - 32 bits - AXINDC_Reg:0x37			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP2	31:0	0x0	Bits 95:64

Last transmitted TLP

PCIE_TX_LAST_TLP3 - R - 32 bits - AXINDC_Reg:0x38			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP3	31:0	0x0	Bits 127:96

Last transmitted TLP

PCIE_I2C_DEBUG_BUS - R - 32 bits - AXINDC_Reg:0x39			
Field Name	**Bits**	**Default**	**Description**
DEBUG_SEL_BLK1	5:0	0x0	Set Debug Bus Block ID for Debug Block1.
DEBUG_SEL_BLK2	11:6	0x0	Set Debug Bus Block ID for Debug Block2.
DEBUG_MUX_BLK1	17:12	0x0	Set Debug mux number for Debug Block1.
DEBUG_MUX_BLK2	23:18	0x0	Set Debug mux to Debug Block2.
DEBUG_BUS_BLK1	24	0x0	Set upper/lower debug port for Debug Block1.
DEBUG_BUS_BLK2	25	0x0	Upper/lower debug port for Debug Block2.
DEBUG_EN	26	0x0	Enable debug daisy chain.
DEBUG_MULTIBLOCK_EN	27	0x0	Enable multiple debug blocks.
DEBUG_RESERVE	31:28	0x0	Reserved

I2C Backdoor Debug Bus Control.

PCIE_I2C_REG_ADDR_EXPAND - RW - 32 bits - AXINDC_Reg:0x3A			
Field Name	**Bits**	**Default**	**Description**
I2C_REG_ADDR (R)	16:0	0x0	Read-only register for reading back the accessing register address.
BDI2C_CPLDATA_RTN_EXPAND	20:17	0x0	Retime the cpl_valid for crossing clock domain from REC_C_CLK to REG_R_CLK in I2C backdoor.
BDREG_CPLDATA_RTN_EXPAND	24:21	0x3	Retime the REG_READ_REQUEST for crossing clock domain from REG_C_CLK to REG_R_CLK in REG_SYNC.

I2C Register Address Expand

PCIE_I2C_REG_DATA - R - 32 bits - AXINDC_Reg:0x3B			
Field Name	**Bits**	**Default**	**Description**
I2C_REG_DATA	31:0	0x0	Register write/read data.

I2C Register Data Register.

PCIE_CFG_CNTL - RW - 32 bits - AXINDC_Reg:0x3C			
Field Name	**Bits**	**Default**	**Description**
CFG_EN_DEC_TO_GEN2_HIDDEN_REG	0	0x0	Enable decoding of GEN2 hidden registers

PCIE_CFG_CNTL - RW - 32 bits - AXINDC_Reg:0x3C			
Field Name	**Bits**	**Default**	**Description**
CFG_EN_DEC_TO_HIDDEN_REG	1	0x0	Enable decoding of hidden registers (excluding GEN2)

Configuration space control register

PCIE_P_CNTL - RW - 32 bits - AXINDC_Reg:0x40			
Field Name	**Bits**	**Default**	**Description**
P_PWRDN_EN	0	0x0	Enable powering down transmitter and receiver pads along with PLL macros.
P_SYMALIGN_MODE	1	0x0	Data Valid generation bit – 0=Relax Mode - Update symbol lock right away when detected bit shifts without waiting for confirmation 1=Aggressive Mode - Always need confirmation for asserting Data Valid
P_ENABLE_PLL_LOCKING_IN_QUICKSIM	2	0x0	Enable actual PLL locking time (30us) when QUICKSIM=1 for simulation purpose. 0=PLL locking time is minimal when QUICKSIM=1 1=Enable normal PLL locking time when QUICKSIM=1
P_PLL_PWRDN_IN_L1L23	3	0x0	Enable PLL powerdown in L1 or L23 Ready states - only if all the associated LC's are in Sates L1 / L23 corresponding to 4 / 2 lanes based on mpConfig and architecture 0=PLL is always running regardless of Link States 1=PLL will be turned off during L1
P_PLL_BUF_PDNB	4	0x1	Disable 10X clock pad on a per PLL basis - should be 1'b0 in order to activate this powersafe feature. 0=Enable PLL Buffer to power down during L1 1=Always keep PLL Buffer running
P_TXCLK_SND_PWRDN	5	0x0	Enable powering down TXCLK clock pads on the transmit side. Each clock pad corresponds to logic associated with 4 lanes.
P_TXCLK_RCV_PWRDN	6	0x0	Enable powering down TXCLK clock pads on the receive side. Each clock pad corresponds to logic associated with 4 lanes.
B_PG2RX_CR_EN_MODE	7	0x0	PHY's CDR Locking (CR_EN) mode 0=CR_EN is LTSSM driven. 1=CR_EN is PHY driven, based on P90_BRX_ELEC_IDLE_ASYNC
P_MASK_RCVR_EIDLE_EN	8	0x0	Enable EIDLE mask for powered down receivers. 0=Don't intercept ELEC_IDLE in power down 1=Intercept ELEC_IDLE in RX power down
P_PLL_PDNB	9	0x1	Enable PLL only (not the buffer) to power down in L1 or L23ready states. 0=Enable PLL to power down during L1 1=Always keep PLL running
P_SYMALIGN_HW_DEBUG	10	0x0	Symbol Alignment HW Debug: 0 = 10-bit compare, 1 = 7-bit compare
P_ELASTDESKEW_HW_DEBUG	11	0x0	HW Debug
P_ALLOW_PRX_FRONTEND_SHUTOFF	12	0x0	Enable PHY's RX FRONTEND to shut off during L1 when PLL power down is enabled. 0=RX Frontend is always power on 1=RX Frontend is shutoff during L1 when PLL power down is enabled

PCIE_P_CNTL - RW - 32 bits - AXINDC_Reg:0x40			
Field Name	**Bits**	**Default**	**Description**
P_ALWAYS_USE_FAST_TXCLK	13	0x0	Bypass TXCLK_SWITCH and use 500MHz TXCLK from PLL for both GEN1 and GEN2 speed. 0=TXCLK will be either 250MHz or 500MHz depends on port speeds 1=Bypass TXCLK_SWITCH and always use 500MHz TXCLK
P_ELEC_IDLE_MODE	15:14	0x0	Electrical Idle Mode for PI (Physical Layer). 0=GEN1 - entry:PHY, exit:PHY ; GEN2 - entry:infer, exit:PHY 1=GEN1 - entry:infer, exit:PHY; GEN2 - entry:infer, exit PHY 2=GEN1 - entry:PHY, exit:PHY ; GEN2 - entry:PHY, exit:PHY 3=Reserved
P_CLK_SWITCH_MODE	17:16	0x0	TXCLK Clock Speed Switch mode. 0=None - switch anytime and bypass skid buffer 1=Wait TX idle - switch when TX is idle 2=Enable skid buffer - switch anytime and enable skid buffer 3=reserved
P_RXEN_GATER	27:24	0x2	Clock cycle delay for muxing back RXCLK when RX_EN is re-asserted again.

PHY Control Register

PCIE_P_BUF_STATUS - RW - 32 bits - AXINDC_Reg:0x41			
Field Name	**Bits**	**Default**	**Description**
P_OVERFLOW_ERR	15:0	0x0	Buffer Overflow Status - one bit per lane (RW1C)
P_UNDERFLOW_ERR	31:16	0x0	Buffer Underflow Status - one bit per lane (RW1C)

Elastic-Deskew Buffer Status Register

PCIE_P_DECODER_STATUS - RW - 32 bits - AXINDC_Reg:0x42			
Field Name	**Bits**	**Default**	**Description**
P_DECODE_ERR	15:0	0x0	Decode Error Status - one bit per lane (RW1C)

Decode8b10b Status Register

PCIE_P_MISC_STATUS - RW - 32 bits - AXINDC_Reg:0x43			
Field Name	**Bits**	**Default**	**Description**
P_DESKEW_ERR	7:0	0x0	Deskew Error Status - one bit per port (RW1C)
P_SYMUNLOCK_ERR	31:16	0x0	Symbol Unlock Status - one bit per lane (RW1C)

Miscellaneous Status Register

PCIE_P_PLL_CNTL - RW - 32 bits - AXINDC_Reg:0x44			
Field Name	**Bits**	**Default**	**Description**
P_VCOREF	1:0	0x0	Control signal generation used in calibrating PLLs 0=OFF 1=VDD/4 2=VDD/2 3=3VDD/4

PCIE_P_PLL_CNTL - RW - 32 bits - AXINDC_Reg:0x44			
Field Name	**Bits**	**Default**	**Description**
P_CALREF	3:2	0x0	Control signal generation used in calibrating PLLs 0=OFF 1=VDD/2 2=2VDD/3 3=5VDD/6

PHY PLL Control Register

PCIE_P_RCV_L0S_FTS_DET - RW - 32 bits - AXINDC_Reg:0x50			
Field Name	**Bits**	**Default**	**Description**
P_RCV_L0S_FTS_DET_MIN (R)	7:0	0xff	Min # of FTS order set detected during RCV L0s
P_RCV_L0S_FTS_DET_MAX (R)	15:8	0x0	Max # of FTS order set detected during RCV L0s

Number of FTS order set detected during RCV L0s (write to reset)

PCIE_P_IMP_CNTL_STRENGTH - RW – 32 bits - AXINDC_Reg:0x60			
Field Name	**Bits**	**Default**	**Description**
P_TX_STR_CNTL_READ_BACK (R)	3:0	0x0	Store the readback value of current controller
P_TX_IMP_CNTL_READ_BACK (R)	7:4	0x0	Store the readback value of TX impedance controller
P_RX_IMP_CNTL_READ_BACK (R)	11:8	0x0	Store the readback value of RX impedance controller
P_TX_STR_CNTL	19:16	0x7	Set the initial default current strength to 4'b0111
P_TX_IMP_CNTL	23:20	0x6	Default TX impedance control value
P_RX_IMP_CNTL	27:24	0x6	Default RX impedance control value
P_PAD_MANUAL_OVERRIDE	31	0x0	Enable Current and Impedance control values to override 0=Allow normal impedance compensation operation 1=Default to manual settings

PHY IMPEDANCE CONTROL STRENGTH REGISTER

PCIE_P_IMP_CNTL_UPDATE - RW - 32 bits - AXINDC_Reg:0x61			
Field Name	**Bits**	**Default**	**Description**
P_IMP_PAD_UPDATE_RATE	4:0	0xe	PAD's update interval 0=PHY130 default 0xf 1=PHY90 default 0xe
P_IMP_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_IMP_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution
P_IMP_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution

Impedance PAD defaults

PCIE_P_STR_CNTL_UPDATE - RW - 32 bits - AXINDC_Reg:0x62			
Field Name	**Bits**	**Default**	**Description**
P_STR_PAD_UPDATE_RATE	4:0	0xf	PAD's update interval 0=PHY130 default 0xf 1=PHY90 default 0xe

PCIE_P_STR_CNTL_UPDATE - RW - 32 bits - AXINDC_Reg:0x62			
Field Name	**Bits**	**Default**	**Description**
P_STR_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_STR_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution
P_STR_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution

Current PAD defaults

PCIE_P_PAD_MISC_CNTL - RW - 32 bits - AXINDC_Reg:0x63			
Field Name	**Bits**	**Default**	**Description**
P_PAD_I_DUMMYOUT (R)	0	0x0	Input from analog - 0 if PMOS cur is stronger
P_PAD_IMP_DUMMYOUT (R)	1	0x0	Input from analog - 0 if PMOS imp is stronger
P_PAD_IMP_TESTOUT (R)	2	0x0	Input from analog - 1 if NMOS imp is stronger
P_PLLCAL_INC_LOWER_PHASE	6:4	0x1	0=0us 1=1us 2=2us 3=4us 4=8us 5=12us 6=16us 7=24us

Pad Miscellaneous Control Registers

PCIE_P_PAD_FORCE_EN - RW - 32 bits - AXINDC_Reg:0x64			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FEN	7:0	0x0	Force B_PTX_PDNB to enable TX pad
B_PRX_PDNB_FEN	15:8	0x0	Force B_PRX_RDNB to enable RX pad
B_PPLL_PDNB_FEN	19:16	0x0	Force B_PPLL_PDNB to enable PLL
B_PPLL_BUF_PDNB_FEN	23:20	0x0	Force B_PPLL_BUF_PDNB to enable 10x driver in PLL
B_PI_DREN_FEN (R)	24	0x0	Force B_PI_DREN to enable current calibration pad
B_PBG_PDNB_FEN (R)	25	0x0	Force B_PBG_PDNB to enable Bandgap circuit in current calibration pad
B_PIMP_TX_PDNB_FEN	26	0x0	Force B_PIMP_TX_PDNB to enable TX impedance calibration pad
B_PIMP_RX_PDNB_FEN	27	0x0	Force B_PIMP_RX_PDNB to enable RX impedance calibration pad

Powerdown enable signals used by the wrapper

PCIE_P_PAD_FORCE_DIS - RW - 32 bits - AXINDC_Reg:0x65			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FDIS	7:0	0x0	Force B_PTX_PDNB to disable TX pad
B_PRX_PDNB_FDIS	15:8	0x0	Force B_PRX_PDNB to disable RX pad
B_PPLL_PDNB_FDIS	19:16	0x0	Force B_PPLL_PDNB to disable PLL
B_PPLL_BUF_PDNB_FDIS	23:20	0x0	Force B_PPLL_BUF_PDNB to disable 10x driver in PLL
B_PI_DREN_FDIS (R)	24	0x0	Force B_PI_DREN to disable current calibration pad
B_PBG_PDNB_FDIS (R)	25	0x0	Force B_PBG_PDNB to disable Bandgap circuit in current calibration pad
B_PIMP_TX_PDNB_FDIS	26	0x0	Force B_PIMP_TX_PDNB to disable TX impedance calibration pad

PCIE_P_PAD_FORCE_DIS - RW - 32 bits - AXINDC_Reg:0x65			
Field Name	**Bits**	**Default**	**Description**
B_PIMP_RX_PDNB_FDIS	27	0x0	Force B_PIMP_TX_PDNB to disable RX impedance calibration pad

Powerdown disable signals used by the wrapper

PCIE_PERF_COUNT_CNTL - RW - 32 bits - AXINDC_Reg:0x80			
Field Name	**Bits**	**Default**	**Description**
GLOBAL_COUNT_EN	0	0x0	Global counter stop/start 0=Stop all counters 1=Start all counters
GLOBAL_SHADOW_WR (W)	1	0x0	Global shadow write
GLOBAL_COUNT_RESET (W)	2	0x0	Global counter reset

Performance Counter Control register

PCIE_PERF_CNTL_TXCLK - RW - 32 bits - AXINDC_Reg:0x81			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - TXCLK domain

PCIE_PERF_COUNT0_TXCLK - R - 32 bits - AXINDC_Reg:0x82			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - TXCLK Domain

PCIE_PERF_COUNT1_TXCLK - R - 32 bits - AXINDC_Reg:0x83			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - TXCLK Domain

PCIE_PERF_CNTL_MST_R_CLK - RW - 32 bits - AXINDC_Reg:0x84			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control

PCIE_PERF_COUNT0_MST_R_CLK - R - 32 bits - AXINDC_Reg:0x85			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - MST_R_CLK domain

PCIE_PERF_COUNT1_MST_R_CLK - R - 32 bits - AXINDC_Reg:0x86			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - MST_R_CLK domain

PCIE_PERF_CNTL_MST_C_CLK - RW - 32 bits - AXINDC_Reg:0x87			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - MST_C_CLK domain

PCIE_PERF_COUNT0_MST_C_CLK - R - 32 bits - AXINDC_Reg:0x88			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - MST_C_CLK domain

PCIE_PERF_COUNT1_MST_C_CLK - R - 32 bits - AXINDC_Reg:0x89			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - MST_C_CLK domain

PCIE_PERF_CNTL_SLV_R_CLK - RW - 32 bits - AXINDC_Reg:0x8A			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - SLV_R_CLK

PCIE_PERF_COUNT0_SLV_R_CLK - R - 32 bits - AXINDC_Reg:0x8B			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - SLV_R_CLK domain

PCIE_PERF_COUNT1_SLV_R_CLK - R - 32 bits - AXINDC_Reg:0x8C			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - SLV_R_CLK domain

PCIE_PERF_CNTL_SLV_S_C_CLK - RW - 32 bits - AXINDC_Reg:0x8D			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - SLV_S_C_CLK domain

PCIE_PERF_COUNT0_SLV_S_C_CLK - R - 32 bits - AXINDC_Reg:0x8E			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - SLV_S_C_CLK domain

PCIE_PERF_COUNT1_SLV_S_C_CLK - R - 32 bits - AXINDC_Reg:0x8F			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - SLV_S_C_CLK domain

PCIE_PERF_CNTL_SLV_NS_C_CLK - RW - 32 bits - AXINDC_Reg:0x90			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - SLV_NS_C_CLK domain

PCIE_PERF_COUNT0_SLV_NS_C_CLK - R - 32 bits - AXINDC_Reg:0x91			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - SLV_NS_C_CLK

PCIE_PERF_COUNT1_SLV_NS_C_CLK - R - 32 bits - AXINDC_Reg:0x92			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - SLV_NS_C_CLK

PCIE_PERF_CNTL_EVENT0_PORT_SEL - RW - 32 bits - AXINDC_Reg:0x93			
Field Name	**Bits**	**Default**	**Description**
PERF0_PORT_SEL_TXCLK	3:0	0x0	Select port for TXCLK counters
PERF0_PORT_SEL_MST_R_CLK	7:4	0x0	Select port for MST_R_CLK counters
PERF0_PORT_SEL_MST_C_CLK	11:8	0x0	Select port for MST_C_CLK counters
PERF0_PORT_SEL_SLV_R_CLK	15:12	0x0	Select port for SLV_R_CLK counters
PERF0_PORT_SEL_SLV_S_C_CLK	19:16	0x0	Select port for SLV_S_C_CLK counters
PERF0_PORT_SEL_SLV_NS_C_CLK	23:20	0x0	Select port for SLV_NS_C_CLK counters
PERF0_PORT_SEL_TXCLK2	27:24	0x0	Select port for 2nd TXCLK counters

Performance Counter 0 Port Select Register

PCIE_PERF_CNTL_EVENT1_PORT_SEL - RW - 32 bits - AXINDC_Reg:0x94			
Field Name	**Bits**	**Default**	**Description**
PERF1_PORT_SEL_TXCLK	3:0	0x0	Select port for TXCLK counters
PERF1_PORT_SEL_MST_R_CLK	7:4	0x0	Select port for MST_R_CLK counters
PERF1_PORT_SEL_MST_C_CLK	11:8	0x0	Select port for MST_C_CLK counters
PERF1_PORT_SEL_SLV_R_CLK	15:12	0x0	Select port for SLV_R_CLK counters
PERF1_PORT_SEL_SLV_S_C_CLK	19:16	0x0	Select port for SLV_S_C_CLK counters
PERF1_PORT_SEL_SLV_NS_C_CLK	23:20	0x0	Select port for SLV_NS_C_CLK counters
PERF1_PORT_SEL_TXCLK2	27:24	0x0	Select port for 2nd TXCLK counters

Performance Counter 1 Port Select Register

PCIE_PERF_CNTL_TXCLK2 - RW - 32 bits - AXINDC_Reg:0x95			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - TXCLK domain (2nd set of TXCLK)

PCIE_PERF_COUNT0_TXCLK2 - R - 32 bits - AXINDC_Reg:0x96			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - TXCLK Domain

PCIE_PERF_COUNT1_TXCLK2 - R - 32 bits – AXINDC_Reg:0x97			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - TXCLK Domain

PCIE_PERF_MAS_ACC_START_LO - RW - 32 bits - AXINDC_Reg:0xA0			
Field Name	**Bits**	**Default**	**Description**
PERF_MAS_ACC_START_LO	31:2	0x0	Start addr value (bits 31:2)

Master access start addr (bits 31:2) for performance event only - master access outside aperture will be counted

PCIE_PERF_MAS_ACC_END_LO - RW - 32 bits - AXINDC_Reg:0xA1			
Field Name	**Bits**	**Default**	**Description**
PERF_MAS_ACC_END_LO	31:2	0x0	End addr value (bits 31:2)

Master access end addr (bits 31:2) aperture for performance event only - master access outside aperture will be counted

PCIE_PERF_MAS_ACC_START_END_HI - RW - 32 bits - AXINDC_Reg:0xA2			
Field Name	**Bits**	**Default**	**Description**
PERF_MAS_ACC_START_HI	7:0	0x0	Start addr upper bits (39:32)
PERF_MAS_ACC_END_HI	15:8	0x0	End addr upper bits (39:32)

Master access upper addr value for performance event only - master access outside aperture will be counted

PCIE_PERF_SLV_ACC_LO - RW - 32 bits - AXINDC_Reg:0xA3			
Field Name	**Bits**	**Default**	**Description**
PERF_SLV_ACC_LO	31:2	0x0	Addr lower bits (31:2)

Slave access addr value for performance counter only - slave access to defined addr will be counted

PCIE_PERF_SLV_ACC_HI - RW - 32 bits - AXINDC_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
PERF_SLV_ACC_HI	31:0	0x0	Upper addr bits(63:32)

Slave access addr value for performance counter only - slave access to defined addr will be counted

PCIE_STRAP_MISC - RW - 32 bits – AXINDC_Reg:0xC0			
Field Name	**Bits**	**Default**	**Description**
STRAP_LINK_CONFIG	3:0	0x0	Provides an override for STRAP_LINK_CONFIG
RESERVED1 (R)	4	0x0	
STRAP_BYPASS_SCRAMBLER	6	0x0	Provides an override for STRAP_BYPASS_SCRAMBLER
STRAP_PHY_RCVRDET_3NF	7	0x0	Provides an override for STRAP_PHY_RCVRDET_3NF
STRAP_F0_AER_EN	8	0x0	Provides an override for STRAP_F0_AER_EN
STRAP_F0_EN	9	0x0	Provides an override for STRAP_F0_EN
STRAP_F0_MSI_EN	10	0x0	Provides an override for STRAP_F0_MSI_EN
STRAP_F0_VC_EN	11	0x0	Provides an override for STRAP_F0_VC_EN
STRAP_F0_LEGACY_DEVICE_TYPE_EN	12	0x0	Provides an override for STRAP_F0_LEGACY_DEVICE_TYPE_EN
STRAP_FIRST_RCVD_ERR_LOG	23	0x0	Provides an override for STRAP_FIRST_RCVD_ERR_LOG 0=FIRST DETECTED ERROR LOGGING 1=FIRST RECEIVED ERROR LOGGING
STRAP_CLK_PM_EN	24	0x0	Provides an override for STRAP_CLK_PM_EN
STRAP_ECN1P1_EN	25	0x0	Provides an override for STRAP_ECN1P1_EN
STRAP_EXT_VC_COUNT	26	0x0	Provides an override for STRAP_EXT_VC_COUNT
RESERVED2 (R)	27	0x0	
STRAP_REVERSE_ALL	28	0x0	Provides an override for STRAP_REVERSE_ALL
STRAP_MST_ADR64_EN	29	0x0	Provides an override for STRAP_MST_ADR64_EN

Misc strap loadable register values

PCIE_STRAP_MISC2 - RW - 32 bits - AXINDC_Reg:0xC1			
Field Name	**Bits**	**Default**	**Description**
STRAP_GEN2_COMPLIANCE	1	0x0	Provides an override for STRAP_GEN2_COMPLIANCE
STRAP_MSTCPL_TIMEOUT_EN	2	0x0	Provides an override for STRAP_MSTCPL_TIMEOUT_EN

Misc strap loadable register values 2

PCIE_STRAP_PI - RW - 32 bits - AXINDC_Reg:0xC2			
Field Name	**Bits**	**Default**	**Description**
STRAP_QUICKSIM_START	0	0x0	Provides an override for STRAP_QUICKSIM_START
STRAP_BACKGROUND_IMP_CAL	1	0x0	Provides an override for STRAP_BACKGROUND_IMP_CAL
STRAP_IMP_MANUAL_OVERRIDE	2	0x0	Provides an override for STRAP_IMP_MANUAL_OVERRIDE
STRAP_PAD_RX_MANUAL_IMPEDANCE	6:3	0x0	Provides an override for STRAP_PAD_RX_MANUAL_IMPEDANCE
STRAP_PAD_TX_MANUAL_IMPEDANCE	10:7	0x0	Provides an override for STRAP_PAD_TX_MANUAL_IMPEDANCE
STRAP_STAGGER_CNTL	16:15	0x0	Provides an override for STRAP_STAGGER_CNTL
STRAP_TX_PDNB_MODE	17	0x0	Provides an override for STRAP_TX_PDNB_MODE
STRAP_VCO_MODE	19:18	0x0	Provides an override for STRAP_VCO_MODE
STRAP_INC_PLLCAL_PHASE	24:21	0x0	Provides an override for STRAP_INC_PLLCAL_PHASE
STRAP_PHY_RX_INCAL_FORCE	25	0x0	Provides an override for STRAP_PHY_RX_INCAL_FORCE
STRAP_TEST_TOGGLE_PATTERN	28	0x0	Provides an override for STRAP_TEST_TOGGLE_PATTERN
STRAP_TEST_TOGGLE_MODE	29	0x0	Provides an override for STRAP_TEST_TOGGLE_MODE

Misc PI strap loadable register values

PCIE_B_P90_CNTL - RW - 32 bits - AXINDC_Reg:0xC3			
Field Name	**Bits**	**Default**	**Description**
B_P90IMP_BACKUP	3:0	0x0	Impedance Control Backup
B_P90PLL_BACKUP	7:4	0x0	PLL Control Backup

PHY90 Extra Control Registers

PCIE_STRAP_I2C_BD - RW - 32 bits - AXINDC_Reg:0xC4			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_I2C_SLV_ADR	6:0	0x0	Provides an override for STRAP_BIF_I2C_SLV_ADR
STRAP_BIF_DBG_I2C_EN	7	0x0	Provides an override for STRAP_BIF_DBG_I2C_EN

I2C Straps

PCIE_P90RX_PRBS10_CNTL - RW - 32 bits - AXINDC_Reg:0xC6			
Field Name	**Bits**	**Default**	**Description**
P90RX_PRBS10_CLR	15:0	0x0	Clear PRBS10_ERRCNT on lane[x]
P90TX_PRBS10_EN	31:16	0x0	Enable PRBS10 checker on lane[x]

PRBS10 Control Register

PCIE_P90_BRX_PRBS10_ER - R - 32 bits - AXINDC_Reg:0xC7			
Field Name	**Bits**	**Default**	**Description**
P90_BRX_PRBS10_ER	15:0	0x0	Status bit indicates that a PRBS10 error has occurred on lane[x]

PRBS10 Error Counter Status

PCIE_PRBS_CLR - RW - 32 bits - AXINDC_Reg:0xC8			
Field Name	**Bits**	**Default**	**Description**
PRBS_CLR	15:0	0x0	Clear PRBS_ERRCNT_x on lane[x]
PRBS_CHECKER_DEBUG_BUS_SELECT	19:16	0x0	Select prbs_chk debug signals of different lanes. 0=Checker 0 debug bus 1=Checker 1 debug bus 2=etc

Clear PRBS Error Counters

PCIE_PRBS_STATUS1 - R - 32 bits - AXINDC_Reg:0xC9			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRSTAT	15:0	0x0	Status bit indicates that a PRBS23 error has occurred on lane[x]
PRBS_LOCKED	31:16	0x0	Status bit indicates that the PRBS pattern has locked on lane[x]

PRBS Status Register

PCIE_PRBS_STATUS2 - R – 32 bits - AXINDC_Reg:0xCA			
Field Name	**Bits**	**Default**	**Description**
PRBS_BITCNT_DONE	15:0	0x0	Indicate PRBS test finished in non-free-run mode for lane[x].

PRBS Status Register2

PCIE_PRBS_FREERUN - RW - 32 bits - AXINDC_Reg:0xCB			
Field Name	**Bits**	**Default**	**Description**
PRBS_FREERUN	15:0	0x0	The PRBS23 error checker is free running on lane[x].

PRBS Freerun Status Register

PCIE_PRBS_MISC - RW - 32 bits - AXINDC_Reg:0xCC			
Field Name	**Bits**	**Default**	**Description**
PRBS_EN	0	0x0	Enable the prbs generator and checkers 0=PRBS GEN disable 1=PRBS GEN enable
PRBS_TEST_MODE	2:1	0x0	Set different test modes: 0=00 - PRBS23 1=01 - PRBS31 2=10 - COUNTER 3=11 - USER DEFINED
PRBS_USER_PATTERN_TOGGLE	3	0x0	Toggle two 8-bit user-defined patterns in 8-bit mode, the 1st pattern is in PRBS_USER_PATTERN[7:0] and the 2nd pattern is in PRBS_USER_PATTERN[15:8]. 0=0 - Replicate user pattern1 1=1 - Toggle user pattern1 and pattern2
PRBS_8BIT_SEL	4	0x0	Set the 8bit and 10bit modes: 0=0 - 10 BIT 1=1 - 8 BIT
PRBS_COMMA_NUM	6:5	0x0	Program the number of COMMA symbols in prbs_gen for recovering bit lock in 8-bit mode. 0=00 - 4 1=01 - 8 2=10 - 16 3=11 - 32
PRBS_LOCK_CNT	11:7	0x0	Program the number of clock cycles for prbs checker to setup bit lock.

PCIE_PRBS_MISC - RW - 32 bits - AXINDC_Reg:0xCC			
Field Name	**Bits**	**Default**	**Description**
PRBS_GEN2_SPEED	15	0x0	Program the signal speed: 0=0 - GEN1 speed 1=1 - GEN2 speed
PRBS_CHK_ERR_MASK	31:16	0x0	Mask PRBS_CHK_ERR output of prbs_chk for lane[x].

PRBS Miscellaneous Control Register

PCIE_PRBS_USER_PATTERN - RW - 32 bits - AXINDC_Reg:0xCD			
Field Name	**Bits**	**Default**	**Description**
PRBS_USER_PATTERN	29:0	0x0	30-bit PRBS User Defined Pattern

PRBS User Defined Pattern

PCIE_PRBS_LO_BITCNT - RW - 32 bits - AXINDC_Reg:0xCE			
Field Name	**Bits**	**Default**	**Description**
PRBS_LO_BITCNT	31:0	0x0	Number of bits to check by the PRBS23 error checkers

PRBS23 Bit Counter Lane 1

PCIE_PRBS_HI_BITCNT - RW - 32 bits - AXINDC_Reg:0xCF			
Field Name	**Bits**	**Default**	**Description**
PRBS_HI_BITCNT	7:0	0x0	Number of bits to check by the PRBS23 error checkers

PRBS23 Bit Counter Lane 1

PCIE_PRBS_ERRCNT_0 - R - 32 bits - AXINDC_Reg:0xD0			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_0	31:0	0x0	Number of errors detected on lane 0

PRBS Error Counter Lane 0

PCIE_PRBS_ERRCNT_1 - R - 32 bits - AXINDC_Reg:0xD1			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_1	31:0	0x0	Number of errors detected on lane 1

PRBS Error Counter Lane 1

PCIE_PRBS_ERRCNT_2 - R - 32 bits - AXINDC_Reg:0xD2			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_2	31:0	0x0	Number of errors detected on lane 2

PRBS Error Counter Lane 2

PCIE_PRBS_ERRCNT_3 - R - 32 bits - AXINDC_Reg:0xD3			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_3	31:0	0x0	Number of errors detected on lane 3

PRBS Error Counter Lane 3

PCIE_PRBS_ERRCNT_4 - R - 32 bits - AXINDC_Reg:0xD4			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_4	31:0	0x0	Number of errors detected on lane 4

PRBS Error Counter Lane 4

PCIE_PRBS_ERRCNT_5 - R - 32 bits - AXINDC_Reg:0xD5			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_5	31:0	0x0	Number of errors detected on lane 5

PRBS Error Counter Lane 5

PCIE_PRBS_ERRCNT_6 - R - 32 bits - AXINDC_Reg:0xD6			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_6	31:0	0x0	Number of errors detected on lane 6

PRBS Error Counter Lane 6

PCIE_PRBS_ERRCNT_7 - R - 32 bits - AXINDC_Reg:0xD7			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_7	31:0	0x0	Number of errors detected on lane 7

PRBS Error Counter Lane 7

PCIE_PRBS_ERRCNT_8 - R - 32 bits - AXINDC_Reg:0xD8			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_8	31:0	0x0	Number of errors detected on lane 8

PRBS Error Counter Lane 8

PCIE_PRBS_ERRCNT_9 - R - 32 bits - AXINDC_Reg:0xD9			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_9	31:0	0x0	Number of errors detected on lane 9

PRBS Error Counter Lane 9

PCIE_PRBS_ERRCNT_10 - R - 32 bits - AXINDC_Reg:0xDA			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_10	31:0	0x0	Number of errors detected on lane 10

PRBS Error Counter Lane 10

PCIE_PRBS_ERRCNT_11 - R - 32 bits - AXINDC_Reg:0xDB			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_11	31:0	0x0	Number of errors detected on lane 11

PRBS Error Counter Lane 11

PCIE_PRBS_ERRCNT_12 - R - 32 bits - AXINDC_Reg:0xDC			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_12	31:0	0x0	Number of errors detected on lane 12

PRBS Error Counter Lane 12

PCIE_PRBS_ERRCNT_13 - R - 32 bits - AXINDC_Reg:0xDD			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_13	31:0	0x0	Number of errors detected on lane 13

PRBS Error Counter Lane 13

PCIE_PRBS_ERRCNT_14 - R - 32 bits - AXINDC_Reg:0xDE			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_14	31:0	0x0	Number of errors detected on lane 14

PRBS Error Counter Lane 14

PCIE_PRBS_ERRCNT_15 - R - 32 bits - AXINDC_Reg:0xDF			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_15	31:0	0x0	Number of errors detected on lane 15

PRBS Error Counter Lane 15

4.2.4 AXINDP Registers

AXINDP is the indirect access register block to control the UMI link port. It is the register block for the per port base control registers, there is only one single port control for the Hudson-1 UMI.

Accessing AXINDP registers requires a second level of indirect procedures. Registers in these spaces are addressed through registers AX_INDXP/AX_DATAP.

Register Name	Address Offset
AX_INDXP	38h
AX_DATAP	3Ch

AX_INDXP – RW – 32 bits – [RegSpace:010b, RegAddr: 38h]			
Field Name	**Bits**	**Default**	**Description**
Register Address	7:0	00h	
Reserved	31:8	000000h	Reserved

AX_DATAP – RW – 32 bits – [RegSpace:010b, RegAddr: 3Ch]			
Field Name	**Bits**	**Default**	**Description**
Data	31:0	00000000h	

Registers in the AXINDP space are addressed through a similar two level method of indirection. The example below illustrates this.

Example: Write TMP to AXINDP:A0h

```
OUT AB_INDX, 40000038h     // Set AB_INDX RegSpace=010, RegAddr=38h.
OUT AB_DATA, 000000A0h     // Set AX_INDXP to 000000A0h through AB_DATA.
OUT AB_INDX, 4000003Ch     // Set AB_INDX RegSpace=010, RegAddr=3Ch.
OUT AB_DATA, TMP           // Write TMP to AXINDP:A0h through AB_DATA.
```

Register Name	Address Offset

Register Name	Address Offset
PCIEP_RESERVED	00h
PCIEP_SCRATCH	01h
PCIEP_HW_DEBUG	02h
PCIEP_PORT_CNTL	10h
PCIE_TX_CNTL	20h
PCIE_TX_REQUESTER_ID	21h
PCIE_TX_VENDOR_SPECIFIC	22h
PCIE_TX_REQUEST_NUM_CNTL	23h
PCIE_TX_SEQ	24h
PCIE_TX_REPLAY	25h
PCIE_TX_ACK_LATENCY_LIMIT	26h
PCIE_TX_CREDITS_ADVT_P	30h
PCIE_TX_CREDITS_ADVT_NP	31h
PCIE_TX_CREDITS_ADVT_CPL	32h
PCIE_TX_CREDITS_INIT_P	33h
PCIE_TX_CREDITS_INIT_NP	34h
PCIE_TX_CREDITS_INIT_CPL	35h
PCIE_TX_CREDITS_STATUS	36h
PCIE_TX_CREDITS_FCU_THRESHOLD	37h
PCIE_P_PORT_LANE_STATUS	50h
PCIE_FC_P	60h
PCIE_FC_NP	61h
PCIE_FC_CPL	62h
PCIE_ERR_CNTL	6Ah
PCIE_RX_CNTL	70h
PCIE_RX_EXPECTED_SEQNUM	71h
PCIE_RX_VENDOR_SPECIFIC	72h
PCIE_RX_CREDITS_ALLOCATED_P	80h
PCIE_RX_CREDITS_ALLOCATED_NP	81h
PCIE_RX_CREDITS_ALLOCATED_CPL	82h
PCIE_RX_CREDITS_RECEIVED_P	83h
PCIE_RX_CREDITS_RECEIVED_NP	84h
PCIE_RX_CREDITS_RECEIVED	85h
PCIE_LC_CNTL	A0h
PCIE_LC_TRAINING_CNTL	A1h
PCIE_LC_LINK_WIDTH_CNTL	A2h
PCIE_LC_N_FTS_CNTL	A3h
PCIE_LC_SPEED_CNTL	A4h
PCIE_LC_STATE0	A5h
PCIE_LC_STATE1	A6h
PCIE_LC_STATE2	A7h
PCIE_LC_STATE3	A8h
PCIE_LC_STATE4	A9h
PCIE_LC_STATE5	AAh
PCIE_LC_CNTL2	B1h
PCIE_LC_BW_CHANGE_CNTL	B2h
PCIE_LC_CDR_CNTL	B3h
PCIE_LC_LANE_CNTL	B4h
PCIE_LC_CNTL3	B5h
PCIEP_STRAP_LC	C0h
PCIEP_STRAP_MISC	C1h

PCIEP_RESERVED - R - 32 bits - AXINDP_Reg:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIEP_RESERVED	31:0	0xffffffff	Reserved

RESERVED

PCIEP_SCRATCH - RW - 32 bits - AXINDP_Reg:0x1			
Field Name	**Bits**	**Default**	**Description**
PCIEP_SCRATCH	31:0	0x0	Scratch Register

Scratch Register

PCIEP_HW_DEBUG - RW - 32 bits - AXINDP_Reg:0x2			
Field Name	**Bits**	**Default**	**Description**
HW_00_DEBUG	0	0x0	bit0
HW_01_DEBUG	1	0x0	bit1
HW_02_DEBUG	2	0x0	bit2
HW_03_DEBUG	3	0x0	bit3
HW_04_DEBUG	4	0x0	bit4
HW_05_DEBUG	5	0x0	bit5
HW_06_DEBUG	6	0x0	bit6
HW_07_DEBUG	7	0x0	bit7
HW_08_DEBUG	8	0x0	bit8
HW_09_DEBUG	9	0x0	bit9
HW_10_DEBUG	10	0x0	bit10
HW_11_DEBUG	11	0x0	bit11
HW_12_DEBUG	12	0x0	bit12
HW_13_DEBUG	13	0x0	bit13
HW_14_DEBUG	14	0x0	REGS_LC_NO_TSx_PAD_RCVD_DIS: Training sets can contain link and lane numbers set to PAD when transitioning from Polling.Active to Detect.Idle.
HW_15_DEBUG	15	0x0	REGS_LC_ALLOW_TX_L1_CONTROL: Allow TX to prevent LC from going to L1 when there are outstanding completions.

Hardware Debug Register

PCIEP_PORT_CNTL - RW - 32 bits - AXINDP_Reg:0x10			
Field Name	**Bits**	**Default**	**Description**
SLV_PORT_REQ_EN	0	0x1	Suspend all slave requests to client 0=Allow slave to be suspended 1=Ignore slave suspend signal
CI_SNOOP_OVERRIDE	1	0x0	Force all slave requests to be snoop requests 0=Do not force all slave requests to be snoop requests 1=Force all slave requests to be snoop requests
HOTPLUG_MSG_EN (R)	2	0x0	Enable hot-plug messages 0=Disable hot-plug messages 1=Enable hot-plug messages
NATIVE_PME_EN (R)	3	0x0	Enable native PME 0=Disable native PME 1=Enable native PME
PWR_FAULT_EN (R)	4	0x0	Enable power fault detection. 0=Disable 1=Enable

PCIEP_PORT_CNTL - RW - 32 bits - AXINDP_Reg:0x10			
Field Name	**Bits**	**Default**	**Description**
PMI_BM_DIS	5	0x0	Disable bus master for power saving state. 0=Normal 1=Disable
SEQNUM_DEBUG_MODE	6	0x0	Enable debug sequence number 0=Normal operation 1=Enable debug sequence number test mode
CI_SLV_CPL_STATIC_ALLOC_LIMIT_S (R)	14:8	0x0	Limit for outstanding Slave Snooped Non-Posted request to Slave 0=128
CI_SLV_CPL_STATIC_ALLOC_LIMIT_NS (R)	22:16	0x0	Limit for outstanding Slave Non-Snooped Non-Posted request to Slave 0=128

Port Control Register

PCIE_TX_CNTL - RW - 32 bits - AXINDP_Reg:0x20			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM_COUNT (R)	9:0	0x0	TX Replay Number Counter - counter to keep track of the number of replays that have occurred
TX_SNR_OVERRIDE	11:10	0x0	Snoop Not Required Override - control of the Snoop bit for master requests 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_RO_OVERRIDE	13:12	0x0	Relaxed Ordering Override - control relaxed ordering bit for master requests 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_PACK_PACKET_DIS	14	0x0	Packet Packing Disable - back-to-back packing of TLP and DLLP 0=Place packets as close as allowable 1=Place STP/SDP in lane 0 only
TX_GAP_BTW_PKTS	18:16	0x0	Number of idle cycles between DLLP and TLP
TX_FLUSH_TLP_DIS	19	0x1	Disable flushing TLPs when Data Link is down 0=Normal 1=Disable
TX_CPL_PASS_P	20	0x0	Ordering rule: Let Completion Pass Posted 0=no pass 1=CPL pass
TX_NP_PASS_P	21	0x0	Ordering rule: Let Non-Posted Pass Posted 0=no pass 1=NP pass
TX_CLEAR_EXTRA_PM_REQS	22	0x1	Enable to clear excess PM DLLPs from pipe 0=Traditional PM request behaviour 1=Clear PM DLLPs from pipe when link transitions from L1_Entry or L23_Entry to Rcv_L0
TX_FC_UPDATE_TIMEOUT_SEL	25:24	0x2	To adjust the length of the timeout interval before sending out flow control update 0=Disable flow control 1=4x clock cycle 2=1024x clock cycle 3=4096x clock cycle
TX_FC_UPDATE_TIMEOUT	31:26	0x7	Interval length to send flow control update

PCIE_TX_CNTL - RW - 32 bits - AXINDP_Reg:0x20			
Field Name	**Bits**	**Default**	**Description**

TX Control Register

PCIE_TX_REQUESTER_ID - RW - 32 bits - AXINDP_Reg:0x21			
Field Name	**Bits**	**Default**	**Description**
TX_REQUESTER_ID_FUNCTION (R)	2:0	0x0	Function ID of Requester for Master transactions or Completer for Slave Completions
TX_REQUESTER_ID_DEVICE (R)	7:3	0x0	Device ID of Requester for Master transactions or Completer for Slave Completions
TX_REQUESTER_ID_BUS (R)	15:8	0x0	Bus ID of Requester for Master transactions or Completer for Slave Completions

TX Requester ID Register

PCIE_TX_VENDOR_SPECIFIC - RW - 32 bits - AXINDP_Reg:0x22			
Field Name	**Bits**	**Default**	**Description**
TX_VENDOR_DATA	23:0	0x0	Writing to this register generates a Vendor Specific DLLP using Vendor Data for the payload

TX Vendor Specific DLLP

PCIE_TX_REQUEST_NUM_CNTL - RW - 32 bits - AXINDP_Reg:0x23			
Field Name	**Bits**	**Default**	**Description**
TX_NUM_OUTSTANDING_NP	29:24	0x20	Number of Non-posted (VC0 and VC1) requests sent out before completion
TX_NUM_OUTSTANDING_NP_VC1_EN	30	0x0	Enable for number of Non-posted VC1 requests sent out before completion
TX_NUM_OUTSTANDING_NP_EN	31	0x0	Enable for number of Non-posted requests sent out before completion

TX Request Num Control Register

PCIE_TX_SEQ - R - 32 bits - AXINDP_Reg:0x24			
Field Name	**Bits**	**Default**	**Description**
TX_NEXT_TRANSMIT_SEQ	11:0	0x0	Next Transmit Sequence Number to send out
TX_ACKD_SEQ	27:16	0x0	Last Acknowledged Sequence Number

TX Sequence Register

PCIE_TX_REPLAY - RW - 32 bits - AXINDP_Reg:0x25			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM	9:0	0x3	Register to control Replay Number before Link goes to Retrain
TX_REPLAY_TIMER_OVERWRITE	15	0x0	Trigger for Replay Timer
TX_REPLAY_TIMER	31:16	0x90	Replay Timer - when expired do Replay

TX Replay Register

PCIE_TX_ACK_LATENCY_LIMIT - RW - 32 bits - AXINDP_Reg:0x26			
Field Name	**Bits**	**Default**	**Description**
TX_ACK_LATENCY_LIMIT	7:0	0x0	ACK Latency Limit for scheduling ACK DLLP transmission

PCIE_TX_ACK_LATENCY_LIMIT - RW - 32 bits - AXINDP_Reg:0x26			
Field Name	**Bits**	**Default**	**Description**
TX_ACK_LATENCY_LIMIT_OVERWRITE	8	0x0	Use register value instead of hardware value from link width

TX ACK Latency Limit

PCIE_TX_CREDITS_ADVT_P - R - 32 bits - AXINDP_Reg:0x30			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_PD	11:0	0x0	Posted data credits
TX_CREDITS_ADVT_PH	23:16	0x0	Posted header credits

Posted advertised credits

PCIE_TX_CREDITS_ADVT_NP - R - 32 bits - AXINDP_Reg:0x31			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_NPD	11:0	0x0	Non-posted data credits
TX_CREDITS_ADVT_NPH	23:16	0x0	Non-posted header credits

Non-posted advertised credits

PCIE_TX_CREDITS_ADVT_CPL - R - 32 bits - AXINDP_Reg:0x32			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_CPLD	11:0	0x0	Completion data credits
TX_CREDITS_ADVT_CPLH	23:16	0x0	Completion header credits

Completion advertised credits

PCIE_TX_CREDITS_INIT_P - R - 32 bits - AXINDP_Reg:0x33			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_PD	11:0	0x0	Posted data credits
TX_CREDITS_INIT_PH	23:16	0x0	Posted header credits

Posted initial credits

PCIE_TX_CREDITS_INIT_NP - R - 32 bits - AXINDP_Reg:0x34			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_NPD	11:0	0x0	Non-posted data credits
TX_CREDITS_INIT_NPH	23:16	0x0	Non-posted header credits

Non-posted initial credits

PCIE_TX_CREDITS_INIT_CPL - R - 32 bits - AXINDP_Reg:0x35			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_CPLD	11:0	0x0	Completion data credits
TX_CREDITS_INIT_CPLH	23:16	0x0	Completion header credits

Completion initial credits

PCIE_TX_CREDITS_STATUS - RW - 32 bits - AXINDP_Reg:0x36			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ERR_PD	0	0x0	RW1C - Posted Data Credits Error
TX_CREDITS_ERR_PH	1	0x0	RW1C - Posted Header Credits Error
TX_CREDITS_ERR_NPD	2	0x0	RW1C - Non-posted Data Credits Error
TX_CREDITS_ERR_NPH	3	0x0	RW1C - Non-posted Header Credits Error
TX_CREDITS_ERR_CPLD	4	0x0	RW1C - Cpl Data Credits Error
TX_CREDITS_ERR_CPLH	5	0x0	RW1C - Cpl Header Credits Error
TX_CREDITS_CUR_STATUS_PD (R)	16	0x0	The current status of the posted data credits
TX_CREDITS_CUR_STATUS_PH (R)	17	0x0	The current status of the posted header credits
TX_CREDITS_CUR_STATUS_NPD (R)	18	0x0	The current status of the non-posted data credits
TX_CREDITS_CUR_STATUS_NPH (R)	19	0x0	The current status of the non-posted header credits
TX_CREDITS_CUR_STATUS_CPLD (R)	20	0x0	The current status of the cpl data credits
TX_CREDITS_CUR_STATUS_CPLH (R)	21	0x0	The current status of the cpl header credits

TX Credits status. When set to 1, remaining credits > init credits. Status bit will remain 1 until a 1 is written to it.

PCIE_TX_CREDITS_FCU_THRESHOLD - RW - 32 bits - AXINDP_Reg:0x37			
Field Name	**Bits**	**Default**	**Description**
TX_FCU_THRESHOLD_P_VC0	2:0	0x3	For VC0 posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_NP_VC0	6:4	0x3	For VC0 non-posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_CPL_VC0	10:8	0x3	For VC0 completion header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1

PCIE_TX_CREDITS_FCU_THRESHOLD - RW - 32 bits - AXINDP_Reg:0x37			
Field Name	**Bits**	**Default**	**Description**
TX_FCU_THRESHOLD_P_VC1	18:16	0x3	For VC1 posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_NP_VC1	22:20	0x3	For VC1 non-posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_CPL_VC1	26:24	0x3	For VC1 completion header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1

TX Credits Flow Control Update Threshold

PCIE_P_PORT_LANE_STATUS - RW - 32 bits - AXINDP_Reg:0x50			
Field Name	**Bits**	**Default**	**Description**
PORT_LANE_REVERSAL (R)	0	0x0	Reverse lanes and control signals associated with a port 0=Port Lane order is normal 1=Port Lane order is reversed
PHY_LINK_WIDTH (R)	6:1	0x0	Link Width 0=6'b00_0000 disabled 1=6'b00_0001 x1 2=6'b00_0010 x2 3=6'b00_0100 x4 4=6'b00_1000 x8 5=6'b01_0000 x12 6=6'b10_0000 x16

Port-Lane Status Register

PCIE_FC_P - RW - 32 bits - AXINDP_Reg:0x60			
Field Name	**Bits**	**Default**	**Description**
PD_CREDITS	7:0	0x8	Posted Data Flow Control Advertised Credits
PH_CREDITS	15:8	0x2	Posted Header Flow Control Advertised Credits

Posted Flow Control Registers

PCIE_FC_NP - RW - 32 bits - AXINDP_Reg:0x61			
Field Name	**Bits**	**Default**	**Description**
NPD_CREDITS	7:0	0x2	Non-Posted Data Flow Control Advertised Credits
NPH_CREDITS	15:8	0x2	Non-Posted Header Flow Control Advertised Credits

Non-Posted Flow Control Registers

PCIE_FC_CPL - RW - 32 bits - AXINDP_Reg:0x62			
Field Name	**Bits**	**Default**	**Description**
CPLD_CREDITS	7:0	0x0	Completion Data Flow Control Credits
CPLH_CREDITS	15:8	0x0	Completion Header Flow Control Credits

Completion Flow Control Registers

PCIE_ERR_CNTL - RW - 32 bits - AXINDP_Reg:0x6A			
Field Name	**Bits**	**Default**	**Description**
ERR_REPORTING_DIS	0	0x0	Disable PCI Express Advanced Error Reporting
TX_GENERATE_LCRC_ ERR (W)	4	0x0	Generate LCRC error for the next transmitted TLP.
RX_GENERATE_LCRC_ ERR (W)	5	0x0	Generate LCRC error for the next received TLP.
TX_GENERATE_ECRC_ ERR (W)	6	0x0	Generate ECRC error for the next transmitted TLP.
RX_GENERATE_ECRC_ ERR (W)	7	0x0	Generate ECRC error for the next received TLP.

Error Control Registers

PCIE_RX_CNTL - RW - 32 bits - AXINDP_Reg:0x70			
Field Name	**Bits**	**Default**	**Description**
RX_IGNORE_IO_ERR	0	0x0	Ignore Malformed I/O TLP Errors
RX_IGNORE_BE_ERR	1	0x0	Ignore Malformed Byte Enable TLP Errors
RX_IGNORE_MSG_ERR	2	0x0	Ignore Malformed Message Error
RX_IGNORE_CRC_ERR (R)	3	0x0	Ignore CRC Errors
RX_IGNORE_CFG_ERR	4	0x0	Ignore Malformed Configuration Errors
RX_IGNORE_CPL_ERR	5	0x0	Ignore Malformed Completion Errors
RX_IGNORE_EP_ERR	6	0x0	Ignore Malformed EP Errors
RX_IGNORE_LEN_MISM ATCH_ERR	7	0x0	Ignore Malformed Length Mismatch Errors
RX_IGNORE_MAX_PAYL OAD_ERR	8	0x0	Ignore Malformed Maximum Payload Errors
RX_IGNORE_TC_ERR	9	0x0	Ignore Malformed Traffic Class Errors
RX_IGNORE_CFG_UR	10	0x0	RESERVED
RX_IGNORE_IO_UR	11	0x0	RESERVED
RX_IGNORE_VEND0_UR	12	0x0	Ignore Vendor Type 0 Messages
RX_NAK_IF_FIFO_FULL (R)	13	0x0	Send NAK if RX internal FIFO is full
RX_GEN_ONE_NAK	14	0x1	Generate NAK only for the first bad packet until replayed
RX_FC_INIT_FROM_RE G	15	0x0	Flow Control Initialization from registers 0=Init FC from FIFO sizes 1=Init FC from registers

PCIE_RX_CNTL - RW - 32 bits - AXINDP_Reg:0x70			
Field Name	**Bits**	**Default**	**Description**
RX_RCB_CPL_TIMEOUT	18:16	0x0	RCB cpl timeout 0=Disable 1=50us 2=10ms 3=25ms 4=50ms 5=100ms 6=500ms 7=1ms
RX_RCB_CPL_TIMEOUT_MODE	19	0x0	RCB CPL timeout on link down
RX_PCIE_CPL_TIMEOUT_DIS	20	0x0	PCIe® CPL timeout on link down disable 1=Disable the timeout feature.

RX Control Register

PCIE_RX_EXPECTED_SEQNUM - R - 32 bits - AXINDP_Reg:0x71			
Field Name	**Bits**	**Default**	**Description**
RX_EXPECTED_SEQNUM	11:0	0x0	Next Expected sequence number

RX Next Expected Sequence Number Register

PCIE_RX_VENDOR_SPECIFIC - R - 32 bits - AXINDP_Reg:0x72			
Field Name	**Bits**	**Default**	**Description**
RX_VENDOR_DATA	23:0	0x0	Writing to this register will re-arm to capture the next Vendor Specific DLLP
RX_VENDOR_STATUS	24	0x0	Indicates that a Vendor Specific DLLP was decoded, and Vendor Data was captured

RX Vendor Specific DLLP

PCIE_RX_CREDITS_ALLOCATED_P - R - 32 bits - AXINDP_Reg:0x80			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_PD	11:0	0x0	For posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_PH	23:16	0x0	For posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256

RX Credits Allocated Register (Posted)

PCIE_RX_CREDITS_ALLOCATED_NP - R - 32 bits - AXINDP_Reg:0x81			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256

RX Credits Allocated Register (Non-Posted)

PCIE_RX_CREDITS_ALLOCATED_CPL - R - 32 bits - AXINDP_Reg:0x82			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_CPLD	11:0	0x0	For completion TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_CPLH	23:16	0x0	For completion TLP header, the number of FC units granted to transmitter since initialization, modulo 256

PCIE_RX_CREDITS_ALLOCATED_CPL - R - 32 bits - AXINDP_Reg:0x82			
Field Name	**Bits**	**Default**	**Description**

RX Credits Allocated Register (Completion)

PCIE_RX_CREDITS_RECEIVED_P - R - 32 bits - AXINDP_Reg:0x83			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_PD	11:0	0x0	For posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096
RX_CREDITS_RECEIVED_PH	23:16	0x0	For posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256

RX Credits Received Register (Posted)

PCIE_RX_CREDITS_RECEIVED_NP - R - 32 bits - AXINDP_Reg:0x84			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096
RX_CREDITS_RECEIVED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256

RX Credits Received Register (Non-Posted)

PCIE_RX_CREDITS_RECEIVED_CPL – R - 32 bits - AXINDP_Reg:0x85			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_CPLD	11:0	0x0	For completion TLP data, the number of FC units consumed by valid TLP received since initialization, module 4096
RX_CREDITS_RECEIVED_CPLH	23:16	0x0	For completion TLP header, the number of FC units consumed by valid TLP received since initialization, module 256

RX Credits Received Register (Completion)

PCIE_LC_CNTL - RW – 32 bits - AXINDP_Reg:0xA0			
Field Name	**Bits**	**Default**	**Description**
LC_CM_HI_ENABLE_COUNT	0	0x0	Enable count for CM_HIGH - when transmitter is to be turned on stop when the counter reaches CM_HI_COUNT_LIMIT_ON. If number of lanes = 1 or 2: CM_HI_COUNT_LIMIT_ON = 12 or 10. If number of lanes = 3 or 4: CM_HI_COUNT_LIMIT_ON = 10 or 12. If number of lanes > 4: CM_HI_COUNT_LIMIT_ON = 10 or 15.
LC_DONT_ENTER_L23_IN_D0	1	0x0	Do not enter L23 in D0 state.
LC_RESET_L_IDLE_COUNT_EN	2	0x0	Enable reset of electrical idle counter.
LC_RESET_LINK	3	0x0	Reset an individual link without resetting the other ports.
LC_16X_CLEAR_TX_PIPE	7:4	0x5	Adjust the time that the LC waits for the pipe to be idle. Setting this field to 0 results in the maximum time. Otherwise, the delay increases as this field is incremented.

PCIE_LC_CNTL - RW – 32 bits - AXINDP_Reg:0xA0			
Field Name	**Bits**	**Default**	**Description**
LC_L0S_INACTIVITY	11:8	0x0	L0s inactivity timer setting 0=L0s is disabled 1=40ns 2=80ns 3=120ns 4=200ns 5=400ns 6=1us 7=2us 8=4us 9=10us 10=40us 11=100us 12=400us 13=1ms 14=4ms
LC_L1_INACTIVITY	15:12	0x0	L1 inactivity timer setting 0=L1 is disabled 1=1us 2=2us 3=4us 4=10us 5=20us 6=40us 7=100us 8=400us 9=1ms 10=4ms 11=10ms 12=40ms 13=100ms 14=400ms
LC_PMI_TO_L1_DIS	16	0x0	Disable the transition to L1 caused by programming PMI_STATE to non-D0
LC_INC_N_FTS_EN	17	0x0	Enable incrementing N_FTS for each transition to recovery
LC_LOOK_FOR_IDLE_IN_L1L23	19:18	0x0	Controls the number of clocks to wait for Electrical Idle set in L1, L23 0=250 1=100 2=10000 3=3000000
LC_FACTOR_IN_EXT_SYNC	20	0x0	Factor in the extended sync bit in the calculation for the replay timer adjustment
LC_WAIT_FOR_PM_ACK_DIS	21	0x0	Disables waiting for PM_ACK in L23 ready entry handshake
LC_WAKE_FROM_L23	22	0x0	For upstream component, wake the link from L23 ready
LC_L1_IMMEDIATE_ACK	23	0x0	Always ACK an ASPM L1 entry DLLP (i.e. never generate PM_NAK)
LC_ASPM_TO_L1_DIS	24	0x0	Disable ASPM L1
LC_DELAY_COUNT	26:25	0x0	Controls minimum amount of time to stay in L0s or L1 0=255/ 4095 (Power-down) 1=1250 / 16383 (Power-down) 2=5000/ 65535 (Power-down) 3=25000 / 262143 (Power-down)
LC_DELAY_L0S_EXIT	27	0x0	Enable staying in L0s for a minimum time
LC_DELAY_L1_EXIT	28	0x0	Enable staying in L1 for a minimum time
LC_EXTEND_WAIT_FOR_EL_IDLE	29	0x1	Wait for Electrical idle in L1/L23 ready value
LC_ESCAPE_L1L23_EN	30	0x1	Enable L1/L23 entry escape arcs

PCIE_LC_CNTL - RW – 32 bits - AXINDP_Reg:0xA0			
Field Name	**Bits**	**Default**	**Description**
LC_GATE_RCVR_IDLE	31	0x0	Ignore PHY Electrical idle detector 0=LC will look for PE_LC_IdleDetected 1=To gate off PE_LC_IdleDetected to LC, so that LC never sees receivers enter EIDLE

Link Control Register

PCIE_LC_TRAINING_CNTL - RW - 32 bits - AXINDP_Reg:0xA1			
Field Name	**Bits**	**Default**	**Description**
LC_TRAINING_CNTL	3:0	0x0	Training control bits in training sets - 0:Reserved, 1:Disable Link, 2:Loopback, 3:Disable Scrambling. The training control signal will be asserted in the TS when the associated bit is set to 1.
LC_COMPLIANCE_RECEIVE	4	0x0	Control for the Compliance Receive bit in Training Sequence 1 Ordered Sets.
LC_LOOK_FOR_MORE_NON_MATCHING_TS1	5	0x0	Look for more non-matching TS1 ordered sets.
LC_L0S_L1_TRAINING_CNTL_EN	6	0x0	Enable transition from L0s & L1 to Recovery if a Hot Reset or Link Disable is initiated.
LC_L1_LONG_WAKE_FIX_EN	7	0x1	Enable fix for FTS going to L1 problem.
LC_POWER_STATE (R)	10:8	0x0	Link Power state
LC_DONT_GO_TO_L0S_IF_L1_ARMED	11	0x0	Prevent the LTSSM from going to Rcv_L0s if it has already acknowledged a request to go to L1 but it hasn't transitioned there yet.
LC_INIT_SPD_CHG_WITH_CSR_EN	12	0x1	Control PCIe® 2.0 clause that states that directed_speed_change should be set if the Retrain Link bit is set to 1 and the Target Link Speed is not equal to the current link speed. 0=Speed negotiation will not be initiated by RETRAIN_LINK Configuration bit. 1=Speed Negotiation can be initiated if RETRAIN_LINK is set and Target Link Speed does not equal the current link speed.
LC_EXTEND_WAIT_FOR_SKP	16	0x1	Extend the timer when in Rcv_L0s_Skp state. Bit is inverted before being used.
LC_AUTONOMOUS_CHANGE_OFF	17	0x0	'Autonomous Change' Data Rate Identifier Control 0='Autonomous Change' is reported as defined in the PCIE 2.0 specification. 1=Do not report 'Autonomous Change'.
LC_UPCONFIGURE_CAP_OFF	18	0x0	'Upconfigure Capability' Data Rate Identifier Control 0='Upconfigure Capability' is reported as defined in the PCIE 2.0 specification. 1=Do not report 'Upconfigure Capability'.
LC_HW_LINK_DIS_EN	19	0x0	Control for the HW or Chip-induced Link Disable feature. Applies to RC only. 0=Allow chip to force link to Link Disable. 1=Turn off chip-induced Link Disable.
LC_LINK_DIS_BY_HW	20	0x0	HW or Chip-induced Link Disable status. Note that this bit is Sticky & RW1C. 0=Chip forced Link to the Link Disable state. 1=Chip-induced Link Disable cleared or never happened.
LC_STATIC_TX_PIPE_COUNT_EN	21	0x0	Use the same WAIT_FOR_EMPTY_PIPE values for all link widths when going to L1 or L23.

PCIE_LC_TRAINING_CNTL - RW - 32 bits - AXINDP_Reg:0xA1			
Field Name	**Bits**	**Default**	**Description**
LC_ASPM_L1_NAK_TIMER_SEL	23:22	0x0	Select timer value to be used when a request to go to L1 is declined i.e. NAK is sent. 0=9.5us 1=3.2us 2=1.6us 3=0.8us
LC_DONT_DEASSERT_RX_EN_IN_R_SPEED	24	0x0	To prevent deassertion of RX_EN during Recovery.Speed.
LC_DONT_DEASSERT_RX_EN_IN_TEST	25	0x0	To prevent deassertion of RX_EN during Polling.Compliance and Loopback.
LC_RESET_ASPM_L1_NAK_TIMER	26	0x1	Prevent L1 Nak Counter from being continuously reset before it has expired (i.e. reached 9.5us) if additional ASPM L1 requests received. 0=Don't reset the 9.5us L1 Nak Counter if additional ASPM L1 requests received. 1=Reset the 9.5us L1 Nak Counter if additional ASPM L1 requests received before counter finishes.
LC_DEBUG_1	27	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_2	28	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_3	29	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_4	30	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_5	31	0x0	Added this bit in case fields needed after registers are frozen.

LC Training Control Register

PCIE_LC_LINK_WIDTH_CNTL - RW - 32 bits - AXINDP_Reg:0xA2			
Field Name	**Bits**	**Default**	**Description**
LC_LINK_WIDTH	2:0	0x6	Link width required.
LC_LINK_WIDTH_RD (R)	6:4	0x0	Read back link width
LC_RECONFIG_ARC_MISSING_ESCAPE	7	0x0	Expedite transition from Recovery.Idle to Detect during a long reconfiguration.
LC_RECONFIG_NOW	8	0x0	Initiate link width change.
LC_RENEGOTIATION_SUPPORT (R)	9	0x0	Advertise link width renegotiation support. 0=Other end does not support link width renegotiation. 1=Other end does support link width renegotiation.
LC_RENEGOTIATE_EN	10	0x0	Enable re-negotiation.
LC_SHORT_RECONFIG_EN	11	0x0	Enable short reconfiguration.
LC_UPCONFIGURE_SUPPORT	12	0x0	Control for the PCIe® 2.0 defined link width change.
LC_UPCONFIGURE_DIS	13	0x0	Override all other control signals of the PCIe 2.0 defined link width change feature.
LC_UPCFG_WAIT_FOR_RCVR_DIS	14	0x0	Disable waiting for all receivers during a link width upconfigure. 0=Enable 1=Disable
LC_UPCFG_TIMER_SEL	15	0x0	Time that state machine waits to receive TS on all receivers during a link width upconfigure. 0=1 msec 1=Use LC_WAIT_FOR_LANES_IN_LW_NEG values
LC_DEASSERT_TX_PDNB	16	0x0	TX_PDNB Control for unused lanes 0=Keep TX_PDNB asserts for unused lanes. 1=Deassert TX_PDNB for unused lanes
LC_L1_RECONFIG_EN	17	0x0	Control for link width change in L1 state. 0=Link width reconfiguration can not be initiated from L1. 1=Link width reconfiguration can be initiated from L1.

PCIE_LC_LINK_WIDTH_CNTL - RW - 32 bits - AXINDP_Reg:0xA2			
Field Name	**Bits**	**Default**	**Description**
LC_DYNLINK_MST_EN	18	0x0	HW initiated link width change feature. 0=Disable 1=Enable HW initiated link width change interface
LC_DUAL_END_RECONFIG_EN	19	0x0	Control Link Width Reconfiguration so that either end is allowed to initiate a link width change to the maximum supported width when the other end has initiated a change to a smaller link width. 0=Allow single end link reconfiguration 1=Allow link width reconfiguration to be simultaneously initiated by either end of the Link
LC_UPCONFIGURE_CAPABLE (R)	20	0x0	Represents upconfigure_capable variable defined in the PCIe® 2.0 specification. 0=PCIe 2.0 Upconfigure feature NOT supported by both ends. 1=PCIe 2.0 Upconfigure feature IS supported by both ends of the Link.

Link Width Control

PCIE_LC_N_FTS_CNTL - RW - 32 bits - AXINDP_Reg:0xA3			
Field Name	**Bits**	**Default**	**Description**
LC_XMIT_N_FTS	7:0	0xc	Number of FTS to override the strap value
LC_XMIT_N_FTS_OVERRIDE_EN	8	0x0	Enable the previous field to override the strap value.
LC_XMIT_FTS_BEFORE_RECOVERY	9	0x1	Transmit FTS before Recovery.
LC_XMIT_N_FTS_LIMIT	23:16	0xff	Limit that the number of FTS can increment to when incrementing is enabled.
LC_N_FTS (R)	31:24	0x0	Number of FTS captured from the other end of the link.

LC Number of FTS Control

PCIE_LC_SPEED_CNTL - RW - 32 bits - AXINDP_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_GEN2_EN_STRAP	0	0x0	PCIE Generation 2 enable bit. Strap Loadable. 0=Gen1 only support. 1=Gen2 supported.
LC_TARGET_LINK_SPEED_OVERRIDE_EN	1	0x0	Enable the overriding of the Target Link Speed configuration register. 0=Disable override. 1=Override Target Link Speed with LC_TARGET_LINK_SPEED_OVERRIDE.
LC_TARGET_LINK_SPEED_OVERRIDE	2	0x0	Value used instead of Target Link Speed when override enable is set. 0=Gen2 not supported when override is enabled. 1=Gen2 supported when override is enabled.
LC_FORCE_EN_SW_SPEED_CHANGE	3	0x0	Force the bif_core to allow speed changes initiated by private registers.
LC_FORCE_DIS_SW_SPEED_CHANGE	4	0x0	Disable speed changes initiated by the bif_core private registers.
LC_FORCE_EN_HW_SPEED_CHANGE	5	0x0	Force the bif_core to allow speed changes initiated by the chip interface (based on voltage levels).
LC_FORCE_DIS_HW_SPEED_CHANGE	6	0x1	Disable speed changes initiated by the chip interface (based on voltage levels).
LC_INITIATE_LINK_SPEED_CHANGE	7	0x0	Initiate speed negotiation when allowed by the register settings.
LC_SPEED_CHANGE_ATTEMPTS_ALLOWED	9:8	0x0	Determines the number of speed change attempts that are allowed.

PCIE_LC_SPEED_CNTL - RW - 32 bits - AXINDP_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_SPEED_CHANGE_ATTEMPT_FAILED (R)	10	0x0	Number of speed change attempts allowed has been reached. This bit and the related counter can be cleared using the LC_CLR_FAILED_SPD_CHANGE_CNT bit.
LC_CURRENT_DATA_RATE (R)	11	0x0	Current data rate of the Link. 0=Gen1 1=Gen2
LC_HW_VOLTAGE_IF_CONTROL	13:12	0x0	Control the chip/bif_core speed control interface. 0=Ignore CHIP/BIF voltage interface. Voltage level is always assumed to be high. 1=CHIP/BIF voltage interface is enabled. 2=CHIP only allowed to lower or raise the voltage when the BIF is running at Gen1 data rate. CHIP must be running at high voltage if BIF is running at Gen2 data rate.
LC_VOLTAGE_TIMER_SEL	17:14	0xa	Controls the circuit that filters noise out of the chip/bif_core voltage interface. 0=No Delay. 1=10ns 2=100ns 3=1us 4=10us 5=100us 6=1ms 7=10ms 8=100ms 9=500ms 10=1sec 11=2sec 12=5sec 13=10sec 14=15sec 15=20sec
LC_GO_TO_RECOVERY	18	0x0	Force the Link to Recovery. Only applicable when link in L0 state.
LC_N_EIE_SEL	19	0x0	Selects the number of EIE (K28.7) symbols that are going to be sent when running at Gen2 speed and the link is exiting L0s. 0=Send 4 EIE (K28.7) symbols before transmitting FTS when exiting L0s at Gen2 speed. 1=Send 8 EIE (K28.7) symbols before transmitting FTS when exiting L0s at Gen2 speed.
LC_DONT_CLR_TARGET_SPD_CHANGE_STATUS	20	0x0	Autonomous speed change control after a speed change attempt has failed. 0=Clear speed negotiation failure initiated by Target Link Speed in Detect. 1=Speed negotiation failure initiated by Target Link Speed is only allowed to fail once.
LC_CLR_FAILED_SPD_CHANGE_CNT	21	0x0	This field will clear the LC_SPEED_CHANGE_ATTEMPT_FAILED field when a '1' is written to it. 0=No Change 1=Clear LC_SPEED_CHANGE_ATTEMPT_FAILED register bit so that more SW or HW(Voltage) initiated speed negotiations can be initiated.

PCIE_LC_SPEED_CNTL - RW - 32 bits - AXINDP_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_1_OR_MORE_TS2_SPEED_ARC_EN	22	0x0	Enable transition from Recovery.RcvrCfg to Recovery.Speed when more than 1 but not all 8 TS2s (with required parameters for a speed change) are received. 0=Don't allow transition from Recovery.RcvrCfg to Recovery.Speed if 1 to 7 TS2s are received. 1=Allow the transition from Recovery.RcvrCfg to Recovery.Speed if 1 to 7 TS2s with speed_change are received.
LC_OTHER_SIDE_EVER_SENT_GEN2 (R)	23	0x0	Cumulative 5.0GT/s capability of the other end of the Link. 0=Other side of link has never advertised that it supports Gen2. 1=Other side of the link has ever advertised that it supports Gen2 - although it may not currently support Gen2.
LC_OTHER_SIDE_SUPPORTS_GEN2 (R)	24	0x0	Current 5.0GT/s capability of the other end of the Link. 0=Other side of the link does not currently advertise that it supports Gen2. 1=Other side of the link currently supports Gen2.
LC_AUTO_RECOVERY_DIS	25	0x1	Autonomous control of the speed advertised after a voltage change. 0=Automatically go to Recovery in order to advertise that a change in Gen2 support has occurred due to a voltage increase. 1=Do not automatically go to Recovery.
LC_SPEED_CHANGE_STATUS	26	0x0	This will gate a HW (i.e. voltage) initiated change to Gen2 when set to 1. 0=No status. 1=Tried to change to Gen2 speed and other end refused. Asserted when the other side no longer supports Gen2.
LC_DATA_RATE_ADVERTISED (R)	27	0x0	Data rate advertised by the port. 0=Only Gen1 support advertised. 1=Gen2 support advertised.
LC_CHECK_DATA_RATE	28	0x1	Determines if the LC is going to check the DATA RATE symbol if the LC_GEN2_EN_STRAP bit is not set. 0=Only check the DATA RATE identifiers when Gen2 is supported. 1=Always check the DATA RATE identifiers regardless of Gen2.
LC_MULT_UPSTREAM_AUTO_SPD_CHNG_EN	29	0x0	Allows the upstream component to initiate speed changes to the highest link speed supported by both ends of the link. Note that multiple speed changes are only allowed if there aren't any failures in previous speed change attempts. Also, note that the STRAP_BIF_AUTO_RC_SPEED_NEGOTIATION_DIS must be 0. 0=The upstream component will only try to automatically change the link to the highest link speed supported by both ends once - regardless of whether the change is successful or not. 1=The upstream component can automatically initiate multiple speed changes.
LC_INIT_SPEED_NEG_IN_L0s_EN	30	0x0	Speed negotiation during L0s control. 0=Do not allow a speed change to be initialized when in the L0s state. 1=Allow speed change negotiations to be initialized from L0s.

PCIE_LC_SPEED_CNTL - RW - 32 bits - AXINDP_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_INIT_SPEED_NEG_IN_L1_EN	31	0x0	Speed negotiation during L1 control. 0=Do not allow a speed change to be initialized when in the L1 state. 1=Allow speed change negotiations to be initialized from L1.

Data Rate Control

PCIE_LC_STATE0 - R – 32 bits - AXINDP_Reg:0xA5			
Field Name	**Bits**	**Default**	**Description**
LC_CURRENT_STATE	5:0	0x0	Current LC State
LC_PREV_STATE1	13:8	0x0	1st Previous LC State
LC_PREV_STATE2	21:16	0x0	2nd Previous LC State
LC_PREV_STATE3	29:24	0x0	3rd Previous LC State

Link Control State Register

PCIE_LC_STATE1 - R – 32 bits - AXINDP_Reg:0xA6			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE4	5:0	0x0	4th Previous LC State
LC_PREV_STATE5	13:8	0x0	5th Previous LC State
LC_PREV_STATE6	21:16	0x0	6th Previous LC State
LC_PREV_STATE7	29:24	0x0	7th Previous LC State

Link Control State Register

PCIE_LC_STATE2 - R - 32 bits - AXINDP_Reg:0xA7			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE8	5:0	0x0	8th Previous LC State
LC_PREV_STATE9	13:8	0x0	9th Previous LC State
LC_PREV_STATE10	21:16	0x0	10th Previous LC State
LC_PREV_STATE11	29:24	0x0	11th Previous LC State

Link Control State Register

PCIE_LC_STATE3 - R - 32 bits - AXINDP_Reg:0xA8			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE12	5:0	0x0	12th Previous LC State
LC_PREV_STATE13	13:8	0x0	13th Previous LC State
LC_PREV_STATE14	21:16	0x0	14th Previous LC State
LC_PREV_STATE15	29:24	0x0	15th Previous LC State

Link Control State Register

PCIE_LC_STATE4 - R - 32 bits - AXINDP_Reg:0xA9			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE16	5:0	0x0	16th Previous LC State
LC_PREV_STATE17	13:8	0x0	17th Previous LC State
LC_PREV_STATE18	21:16	0x0	18th Previous LC State
LC_PREV_STATE19	29:24	0x0	19th Previous LC State

Link Control State Register

PCIE_LC_STATE5 - R - 32 bits - AXINDP_Reg:0xAA			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE20	5:0	0x0	20th Previous LC State
LC_PREV_STATE21	13:8	0x0	21st Previous LC State
LC_PREV_STATE22	21:16	0x0	22nd Previous LC State
LC_PREV_STATE23	29:24	0x0	23rd Previous LC State

Link Control State Register

PCIE_LC_CNTL2 - RW - 32 bits - AXINDP_Reg:0xB1			
Field Name	**Bits**	**Default**	**Description**
LC_TIMED_OUT_STATE (R)	5:0	0x0	State that the LC was in when the deadman timer expired.
LC_STATE_TIMED_OUT	6	0x0	Deadman timer expired.
LC_LOOK_FOR_BW_REDUCTION	7	0x1	Enable check for bandwidth change when reporting Link Bandwidth Notification Status. 0=Do not check if bandwidth was reduced. 1=Check if bandwidth was reduced.
LC_MORE_TS2_EN	8	0x0	Send out 128 sets instead of 16.
LC_X12_NEGOTIATION_DIS	9	0x1	Disable x12 negotiation.
LC_LINK_UP_REVERSAL_EN	10	0x0	Allow reversal for a wider width in link up.
LC_ILLEGAL_STATE	11	0x0	The LC is in an illegal state.
LC_ILLEGAL_STATE_RESTART_EN	12	0x0	Enable the LC to be restarted when it is in an illegal state.
LC_WAIT_FOR_OTHER_LANES_MODE	13	0x0	Eliminate delay introduced by waiting for other lanes. 0=Identical Training Set based (wait time limited by counter) 1=Timer based
LC_ELEC_IDLE_MODE	15:14	0x0	Electrical Idle Mode for LC. 0=GEN1 - entry:PHY, exit:PHY ; GEN2 - entry:infer, exit:PHY 1=GEN1 - entry:infer, exit:PHY; GEN2 - entry:infer, exit PHY 2=GEN1 - entry:PHY, exit:PHY ; GEN2 - entry:PHY, exit:PHY 3=Reserved
LC_DISABLE_INFERRED_ELEC_IDLE_DET	16	0x0	Disable Inferred Electrical Idle detection. 0=Inferred Electrical Idle Detection is enabled 1=Inferred Electrical Idle Detection is disabled
LC_ALLOW_PDWN_IN_L1	17	0x0	Set the BIF_CHIP_CLK_PDWN output to 1 when the LC is in the L1 state.
LC_ALLOW_PDWN_IN_L23	18	0x0	Set the BIF_CHIP_CLK_PDWN output to 1 when the LC is in the L23_Ready state.
LC_DEASSERT_RX_EN_IN_L0S	19	0x0	Turn off transmitters when the link is in L0s.
LC_BLOCK_EL_IDLE_IN_L0	20	0x0	Prevent the Electrical Idle from causing a transition from Rcv_L0 to Rcv_L0s.
LC_RCV_L0_TO_RCV_L0S_DIS	21	0x0	Disable transition from Rcv_L0 to Rcv_L0s
LC_ASSERT_INACTIVE_DURING_HOLD	22	0x0	Assert the INACTIVE_LANES signals when CHIP_BIF_hold_training is high.
LC_WAIT_FOR_LANES_IN_LW_NEG	24:23	0x0	Mode used to wait for TS on all lanes in link width negotiation.
LC_PWR_DOWN_NEG_OFF_LANES	25	0x1	Power down unused lanes.
LC_DISABLE_LOST_SYM_LOCK_ARCS	26	0x1	Control transition to Recovery.RcvrLock from Configuration.Idle or Recovery.Idle when a training set is received. Similar to 'idle_to_rlock_transitioned' variable.

PCIE_LC_CNTL2 - RW - 32 bits - AXINDP_Reg:0xB1			
Field Name	**Bits**	**Default**	**Description**
LC_LINK_BW_NOTIFICATION_DIS (R)	27	0x0	Control for the Link Bandwidth Notification Feature.
LC_ENABLE_RX_CR_EN_DEASSERTION	28	0x0	To enable deassertion of PG2RX_CR_EN to lock clock recovery parameter when lane is in electrical idle 0=CR_EN is always asserted 1=CR_EN is deasserted when RX_EN is deasserted during L0s/L1 and inactive lanes
LC_TEST_TIMER_SEL	30:29	0x0	State timeout select 0=LTSSM uses spec compliant timeout values. 1=LTSSM uses simulation timeout values. 2=LTSSM uses decreased timeout values for lab testing. 3=Reserved
LC_ENABLE_INFERRED_ELEC_IDLE_FOR_PI	31	0x1	Enable Inferred Electrical Idle Detection for PI (Physical Layer blocks) 0=Inferred Electrical Idle Detection is disabled for PI (Physical Layer block) 1=Inferred Electrical Idle Detection is enabled for PI (Physical Layer block)

Link Control Register 2

PCIE_LC_BW_CHANGE_CNTL - RW - 32 bits - AXINDP_Reg:0xB2			
Field Name	**Bits**	**Default**	**Description**
LC_BW_CHANGE_INT_EN	0	0x0	Enable Interrupt when the link bandwidth changes.
LC_HW_INIT_SPEED_CHANGE	1	0x0	Link speed changed due to a hardware-initiated speed negotiation.
LC_SW_INIT_SPEED_CHANGE	2	0x0	Link speed changed due to a software-initiated speed negotiation.
LC_OTHER_INIT_SPEED_CHANGE	3	0x0	Link speed changed due to a speed negotiation initiated by the other end of the link.
LC_RELIABILITY_SPEED_CHANGE	4	0x0	Link speed changed due to a reliability issue at the current speed.
LC_FAILED_SPEED_NEG	5	0x0	Link speed change failed and link speed was reverted to initial speed.
LC_LONG_LW_CHANGE	6	0x0	Link width was changed due to a long dynamic link width reconfiguration.
LC_SHORT_LW_CHANGE	7	0x0	Link width was changed due to a short dynamic link width reconfiguration.
LC_LW_CHANGE_OTHER	8	0x0	Link width changed and the change was initiated by the other end of the link.\
LC_LW_CHANGE_FAILED	9	0x0	Link width change was initiated by the width was not changed.
LC_LINK_BW_NOTIFICATION_DETECT_MODE	10	0x0	Control Link Bandwidth Management for speed changes in Detect. 0=Disable Link Bandwidth Management Capabilities in Detect. 1=Update LINK_BW_MANAGEMENT_STATUS when speed changes in Detect.

LC Bandwidth Change Notification Control Register

PCIE_LC_CDR_CNTL - RW - 32 bits - AXINDP_Reg:0xB3			
Field Name	**Bits**	**Default**	**Description**
LC_CDR_TEST_OFF	11:0	0x60	Enable CDR Test Mode.
LC_CDR_TEST_SETS	23:12	0x18	Select the number of sets that are transmitted during CDR test mode.

PCIE_LC_CDR_CNTL - RW - 32 bits - AXINDP_Reg:0xB3			
Field Name	**Bits**	**Default**	**Description**
LC_CDR_SET_TYPE	25:24	0x1	Select for the type of set that is transmitted during CDR test mode.

CDR Control Register

PCIE_LC_LANE_CNTL - RW - 32 bits - AXINDP_Reg:0xB4			
Field Name	**Bits**	**Default**	**Description**
LC_CORRUPTED_LANES (R)	15:0	0x0	Each bit indicates if the associated lane had trouble during training.
LC_LANE_DIS	31:16	0x0	Permanently disable associated lane.

Lane Status and Control Register

PCIE_LC_CNTL3 - RW - 32 bits - AXINDP_Reg:0xB5			
Field Name	**Bits**	**Default**	**Description**
LC_SELECT_DEEMPHASIS	0	0x0	Downstream De-Emphasis 0=-6dB De-emphasis required. 1=-3.5dB De-emphasis required.
LC_SELECT_DEEMPHASIS_CNTL	2:1	0x0	Upstream De-Emphasis control 0=Use De-emphasis from CSR. 1=Use De-emphasis from downstream component. 2=Use -6dB De-emphasis. 3=Use -3.5dB De-emphasis.
LC_RCVD_DEEMPHASIS (R)	3	0x0	De-emphasis setting advertised by other end.
LC_COMP_TO_DETECT	4	0x0	Modified Compliance Pattern control 0=No action taken. 1=Transition LTSSM from Polling. Compliance to Detect if sending out Modified Compliance Pattern due to receipt of TS1s.
LC_RESET_TSX_CNT_IN_RLOCK_EN	5	0x1	TS Ordered Set Counter Control in Recovery.RcvrLock 0=No change in Training Sequence counter when DIRECTED_SPEED_CHANGE asserted in Recovery.RcvrLock. 1=Reset Training Sequence counter when DIRECTED_SPEED_CHANGE is asserted in Recovery.RcvrLock.
LC_AUTO_SPEED_CHANGE_ATTEMPTS_ALLOWED	7:6	0x0	Number of unsuccessful Autonomous Speed Changes that are allowed. N/A for downstream components. 0=1 1=2 2=3 3=4
LC_AUTO_SPEED_CHANGE_ATTEMPT_FAILED (R)	8	0x0	Number of maximum unsuccessful Autonomous Speed Change attempts reached. N/A for downstream components. 0=Autonomous changes by RC allowed. 1=Maximum allowable number of autonomous speed changes reached.
LC_CLR_FAILED_AUTO_SPD_CHANGE_CNT	9	0x0	Clear Autonomous Speed Change counter. N/A for downstream components. 0=No action taken. 1=Clear LC_AUTO_SPEED_CHANGE_ATTEMPT_FAILED register bit so that the RC can autonomously initiate more speed negotiations.

Link Control Register 3

PCIEP_STRAP_LC - RW - 32 bits - AXINDP_Reg:0xC0			
Field Name	**Bits**	**Default**	**Description**
STRAP_FTS_yTSx_COUNT	1:0	0x0	Provides an override for STRAP_FTS_yTSx_COUNT
STRAP_LONG_yTSx_COUNT	3:2	0x0	Provides an override for STRAP_LONG_yTSx_COUNT
STRAP_MED_yTSx_COUNT	5:4	0x0	Provides an override for STRAP_MED_yTSx_COUNT
STRAP_SHORT_yTSx_COUNT	7:6	0x0	Provides an override for STRAP_SHORT_yTSx_COUNT
STRAP_SKIP_INTERVAL	10:8	0x0	Provides an override for STRAP_SKIP_INTERVAL
STRAP_BYPASS_RCVR_DET	11	0x0	Provides an override for STRAP_BYPASS_RCVR_DET
STRAP_COMPLIANCE_DIS	12	0x0	Provides an override for STRAP_COMPLIANCE_DIS
STRAP_FORCE_COMPLIANCE	13	0x0	Provides an override for STRAP_FORCE_COMPLIANCE
STRAP_REVERSE_LC_LANES	14	0x0	Provides an override for STRAP_REVERSE_LC_LANES
STRAP_AUTO_RC_SPEED_NEGOTIATION_DIS	15	0x0	Provides an override for STRAP_AUTO_RC_SPEED_NEGOTIATION_DIS
STRAP_LANE_NEGOTIATION	18:16	0x0	Provides an override for STRAP_LANE_NEGOTIATION 0=Compliant mode, widest possible link 1=Compliant mode, fix missing lane 0 2=Compliant mode, reverse only 3=Compliant mode, reverse only, don't require the sets to be contiguous 4=Old mode, reverse only 5=Easy training mode, reverse only 6=Reliable mode, reverse only - means to reliably train, in a reliable system 7=Reserved

Misc LC strap loadable register value

PCIEP_STRAP_MISC - RW - 32 bits - AXINDP_Reg:0xC1			
Field Name	**Bits**	**Default**	**Description**
STRAP_EXIT_LATENCY	3:0	0x0	Provides an override for STRAP_EXIT_LATENCY
STRAP_REVERSE_LANES	4	0x0	Provides an override for STRAP_REVERSE_LANES

Misc port strap loadable register values

4.2.5 RCINDC Registers

Accessing RCINDC registers does not require second level of indirect procedures. Registers in these spaces are addressed through registers AB_INDX/AB_DATA.

To access an RCINDC register, the register address is first written to the RegAddr (AB_INDX[16:0]) and with RegSpace (AB_INDX[31:29]) set to 001. The specified RCINDC register is then accessed through a read or a write to AB_DATA. A programming example is provided below to illustrate this.

Example: Read RCINDC:10h to TMP

```
OUT AB_INDX, 20000010h     // Set AB_INDX RegSpace=001, RCINDC=10h
IN  AB_DATA, TMP           // Read RCINDC:10h through AB_DATA.
```

Register Name	Address Offset
PCIE_RESERVED	00h
PCIE_SCRATCH	01h
PCIE_HW_DEBUG	02h
PCIE_RX_NUM_NAK	0Eh
PCIE_RX_NUM_NAK_GENERATED	0Fh
PCIE_CNTL	10h
PCIE_CONFIG_CNTL	11h
PCIE_DEBUG_CNTL	12h
PCIE_RTR_CPL_TIMEOUT_STATUS	13h
PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL	14h
PCIE_CI_MST_R_RTR_TIMEOUT_CNTL	15h
PCIE_CI_MST_C_RTR_TIMEOUT_CNTL	16h
PCIE_REG_R_RTR_TIMEOUT_CNTL	17h
PCIE_TX_SLVCPL_TIMEOUT_CNTL	18h
PCIE_TX_SLVCPL_NS_TIMEOUT_CNTL	19h
PCIE_CNTL2	1Ch
PCIE_CI_CNTL	20h
PCIE_BUS_CNTL	21h
PCIE_LC_STATE6	22h
PCIE_LC_STATE7	23h
PCIE_LC_STATE8	24h
PCIE_LC_STATE9	25h
PCIE_LC_STATE10	26h
PCIE_LC_STATE11	27h
PCIE_LC_STATUS1	28h
PCIE_LC_STATUS2	29h
PCIE_WPR_CNTL	30h
PCIE_RX_LAST_TLP0	31h
PCIE_RX_LAST_TLP1	32h
PCIE_RX_LAST_TLP2	33h
PCIE_RX_LAST_TLP3	34h
PCIE_TX_LAST_TLP0	35h
PCIE_TX_LAST_TLP1	36h
PCIE_TX_LAST_TLP2	37h
PCIE_TX_LAST_TLP3	38h
PCIE_I2C_DEBUG_BUS	39h
PCIE_I2C_REG_ADDR_EXPAND	3Ah
PCIE_I2C_REG_DATA	3Bh
PCIE_CFG_CNTL	3Ch
PCIE_P_CNTL	40h
PCIE_P_BUF_STATUS	41h
PCIE_P_DECODER_STATUS	42h
PCIE_P_MISC_STATUS	43h
PCIE_P_PLL_CNTL	44h
PCIE_P_RCV_L0S_FTS_DET	50h
PCIE_P_IMP_CNTL_STRENGTH	60h
PCIE_P_IMP_CNTL_UPDATE	61h
PCIE_P_STR_CNTL_UPDATE	62h
PCIE_P_PAD_MISC_CNTL	63h
PCIE_P_PAD_FORCE_EN	64h
PCIE_P_PAD_FORCE_DIS	65h
PCIE_PERF_COUNT_CNTL	80h
PCIE_PERF_CNTL_TXCLK	81h

Register Name	Address Offset
PCIE_PERF_COUNT0_TXCLK	82h
PCIE_PERF_COUNT1_TXCLK	83h
PCIE_PERF_CNTL_MST_R_CLK	84h
PCIE_PERF_COUNT0_MST_R_CLK	85h
PCIE_PERF_COUNT1_MST_R_CLK	86h
PCIE_PERF_CNTL_MST_C_CLK	87h
PCIE_PERF_COUNT0_MST_C_CLK	88h
PCIE_PERF_COUNT1_MST_C_CLK	89h
PCIE_PERF_CNTL_SLV_R_CLK	8Ah
PCIE_PERF_COUNT0_SLV_R_CLK	8Bh
PCIE_PERF_COUNT1_SLV_R_CLK	8Ch
PCIE_PERF_CNTL_SLV_S_C_CLK	8Dh
PCIE_PERF_COUNT0_SLV_S_C_CLK	8Eh
PCIE_PERF_COUNT1_SLV_S_C_CLK	8Fh
PCIE_PERF_CNTL_SLV_NS_C_CLK	90h
PCIE_PERF_COUNT0_SLV_NS_C_CLK	91h
PCIE_PERF_COUNT1_SLV_NS_C_CLK	92h
PCIE_PERF_CNTL_EVENT0_PORT_SEL	93h
PCIE_PERF_CNTL_EVENT1_PORT_SEL	94h
PCIE_PERF_CNTL_TXCLK2	95h
PCIE_PERF_COUNT0_TXCLK2	96h
PCIE_PERF_COUNT1_TXCLK2	97h
PCIE_PERF_MAS_ACC_START_LO	A0h
PCIE_PERF_MAS_ACC_END_LO	A1h
PCIE_PERF_MAS_ACC_START_END_HI	A2h
PCIE_PERF_SLV_ACC_LO	A3h
PCIE_PERF_SLV_ACC_HI	A4h
PCIE_STRAP_MISC	C0h
PCIE_STRAP_MISC2	C1h
PCIE_STRAP_PI	C2h
PCIE_B_P90_CNTL	C3h
PCIE_STRAP_I2C_BD	C4h
PCIE_P90RX_PRBS10_CNTL	C6h
PCIE_P90_BRX_PRBS10_ER	C7h
PCIE_PRBS_CLR	C8h
PCIE_PRBS_STATUS1	C9h
PCIE_PRBS_STATUS2	CAh
PCIE_PRBS_FREERUN	CBh
PCIE_PRBS_MISC	CCh
PCIE_PRBS_USER_PATTERN	CDh
PCIE_PRBS_LO_BITCNT	CEh
PCIE_PRBS_HI_BITCNT	CFh
PCIE_PRBS_ERRCNT_0	D0h
PCIE_PRBS_ERRCNT_1	D1h
PCIE_PRBS_ERRCNT_2	D2h
PCIE_PRBS_ERRCNT_3	D3h
PCIE_PRBS_ERRCNT_4	D4h
PCIE_PRBS_ERRCNT_5	D5h
PCIE_PRBS_ERRCNT_6	D6h
PCIE_PRBS_ERRCNT_7	D7h
PCIE_PRBS_ERRCNT_8	D8h
PCIE_PRBS_ERRCNT_9	D9h
PCIE_PRBS_ERRCNT_10	DAh
PCIE_PRBS_ERRCNT_11	DBh
PCIE_PRBS_ERRCNT_12	DCh
PCIE_PRBS_ERRCNT_13	DDh
PCIE_PRBS_ERRCNT_14	DEh
PCIE_PRBS_ERRCNT_15	DFh

PCIE_RESERVED - R - 32 bits - RCINDC_Reg:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIE_RESERVED	31:0	0xffffffff	RESERVED

Reserved

PCIE_SCRATCH - RW - 32 bits - RCINDC_Reg:0x1			
Field Name	**Bits**	**Default**	**Description**
PCIE_SCRATCH	31:0	0x0	Software test register

Software test register

PCIE_HW_DEBUG - RW - 32 bits - RCINDC_Reg:0x2			
Field Name	**Bits**	**Default**	**Description**
HW_00_DEBUG	0	0x0	Ignore DLLPs during L1 so that TXCLK can be turned off.
HW_01_DEBUG	1	0x0	bit1
HW_02_DEBUG	2	0x0	bit2
HW_03_DEBUG	3	0x0	Used to enable the PLL power down when all lanes are inactive. It should be on in GPP.
HW_04_DEBUG	4	0x0	bit4
HW_05_DEBUG	5	0x0	bit5
HW_06_DEBUG	6	0x0	bit6
HW_07_DEBUG	7	0x0	bit7
HW_08_DEBUG	8	0x0	Turns on the BUG fix for the race problem between LC wakeup from L1 and PLL calibration in GEN2.
HW_09_DEBUG	9	0x0	bit9
HW_10_DEBUG	10	0x0	bit10
HW_11_DEBUG	11	0x0	bit11
HW_12_DEBUG	12	0x0	bit12
HW_13_DEBUG	13	0x0	bit13
HW_14_DEBUG	14	0x0	bit14
HW_15_DEBUG	15	0x0	Selects between chip power state (1) and software power state (0).

hardware debug register

PCIE_RX_NUM_NAK - R - 32 bits - RCINDC_Reg:0xE			
Field Name	**Bits**	**Default**	**Description**
RX_NUM_NAK	31:0	0x0	Total number of naks received

Num naks received

PCIE_RX_NUM_NAK_GENERATED - R - 32 bits - RCINDC_Reg:0xF			
Field Name	**Bits**	**Default**	**Description**
RX_NUM_NAK_GENERATED	31:0	0x0	Total number of naks generated

Num naks generated

PCIE_CNTL - RW - 32 bits - RCINDC_Reg:0x10			
Field Name	**Bits**	**Default**	**Description**
HWINIT_WR_LOCK	0	0x0	Hardware write lock 0=HWInit registers unlocked 1=Lock HWInit registers
UR_ERR_REPORT_DIS	7	0x0	UR error reporting disable for TX
PCIE_HT_NP_MEM_WRITE	9	0x0	Memory write mapping enable
RX_FCH_ADJ_PAYLOAD_SIZE	12:10	0x2	FCH payload size 2=16 bytes 3=32 bytes 4=64 bytes
RX_RCB_REORDER_EN	16	0x1	RCB ordering enable 0=No re-ordering 1=Re-ordering
RX_RCB_INVALID_SIZE_DIS	17	0x1	RCB invalid size disable
RX_RCB_UNEXP_CPL_DIS	18	0x0	RCB unexpected cpl disable
RX_RCB_CPL_TIMEOUT_TEST_MODE	19	0x0	RCB cpl timeout test mode
RX_RCB_CHANNEL_ORDERING	20	0x0	GFX only. 1- completion reordering within Snooped/Non-Snooped channel. 0- Completion reordering both channels together (default)
RX_RCB_WRONG_ATTR_DIS	21	0x1	RCB invalid attributes check for received completions disable
RX_RCB_WRONG_FUNCNUM_DIS	22	0x1	RCB invalid function number check for received completions disable
LC_PREVENT_SPD_CHG_OVERLAP	23	0x1	Don't allow two speed change requests in opposite directions during the same clock cycle.
TX_CPL_DEBUG	29:24	0x0	CPL debug
RX_CPL_POSTED_REQ_ORD_EN	31	0x1	CPL request ordering enable 0=Disable RX request ordering 1=Enable RX request ordering

PCIExpress control register

PCIE_CONFIG_CNTL - RW - 32 bits - RCINDC_Reg:0x11			
Field Name	**Bits**	**Default**	**Description**
DYN_CLK_LATENCY	3:0	0x7	Dynamic Clock Latency

PCIExpress Configuration Control Register

PCIE_DEBUG_CNTL - RW - 32 bits - RCINDC_Reg:0x12			
Field Name	**Bits**	**Default**	**Description**
DEBUG_PORT_EN	7:0	0x1	Debug Bus Port Enable 1=port A 2=port B 4=port C 8=port D 16=port E 32=port F 64=port G 128=port H
DEBUG_SELECT	8	0x0	Debug Bus Select - for additional muxing (e.g. VC0 vs. VC1)

PCIE_DEBUG_CNTL - RW - 32 bits - RCINDC_Reg:0x12			
Field Name	**Bits**	**Default**	**Description**
DEBUG_LANE_EN	31:16	0x1	Debug Lane Enable : lane0=1, lane1=2, lane2=4, lane3=8, lane4=16, lane5=32, lane6=64, lane7=128, lane8=256, lane9=512, lane10=1024, lane11=2048, lane12=4096, lane13=8192, lane14=16384, lane15=32768

Debug Bus Control Register

PCIE_RTR_CPL_TIMEOUT_STATUS - RW - 32 bits - RCINDC_Reg:0x13			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_R_RTR_ERROR	0	0x0	Slave req interface - 1 indicates slv RTR was de-asserted for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1.
CI_MST_R_RTR_ERROR	1	0x0	Master req interface - 1 indicates mst req RTR was de-asserted for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1.
CI_MST_C_RTR_ERROR	2	0x0	Master completion interface - 1 indicates mst cpl RTR was de-asserted for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1.
REG_R_RTR_ERROR	3	0x0	Register req interface - 1 indicates reg req RTR was de-asserted for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1.
TX_SLVCPL_TIMEOUT_ERROR	4	0x0	Slave completion interface - 1 indicates slv cpl hasn't been received for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1. For RC this bit is for the Snoop channel.
TX_SLVCPL_NS_TIMEOUT_ERROR	5	0x0	Slave completion interface - 1 indicates slv cpl hasn't been received for more than the # of cycles programmed in the CNTL register, this bit remains asserted until it is cleared by writing a 1. For RC this bit is for the Non-Snoop channel.
CI_SLV_R_RTR_STATUS (R)	16	0x0	For testability only. The bit is set when CI_SLV_R interface RTR is deasserted for the programmed number of clock cycles.
CI_MST_R_RTR_STATUS (R)	17	0x0	For testability only. The bit is set when CI_MST_R interface RTR is deasserted for the programmed number of clock cycles.
CI_MST_C_RTR_STATUS (R)	18	0x0	For testability only. The bit is set when CI_MST_C interface RTR is deasserted for the programmed number of clock cycles.
REG_R_RTR_STATUS (R)	19	0x0	For testability only. The bit is set when REG_R interface RTR is deasserted for the programmed number of clock cycles.
TX_SLVCPL_TIMEOUT_STATUS (R)	20	0x0	The bit is set when the slave completions (snoop) are not received during the programmed timeout.
TX_SLVCPL_NS_TIMEOUT_STATUS (R)	21	0x0	The bit is set when the slave completions (non-snoop) are not received during the programmed timeout.

Status register for rtr/cpl timeout

PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL - RW - 32 bits - RCINDC_Reg:0x14			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slv req RTR timer

PCIE_CI_SLV_R_RTR_TIMEOUT_CNTL - RW - 32 bits - RCINDC_Reg:0x14			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in SLV_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1).

Control register for slave request RTR timeout

PCIE_CI_MST_R_RTR_TIMEOUT_CNTL - RW - 32 bits – RCINDC_Reg:0x15			
Field Name	**Bits**	**Default**	**Description**
CI_MST_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the master req RTR timer
CI_MST_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in MST_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1).

Control register for master request RTR timeout

PCIE_CI_MST_C_RTR_TIMEOUT_CNTL - RW - 32 bits – RCINDC_Reg:0x16			
Field Name	**Bits**	**Default**	**Description**
CI_MST_C_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the master cpl RTR timer.
CI_MST_C_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in MST_C_CLK) how long the RTR must be de-asserted before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1).

Control register for master completion RTR timeout

PCIE_REG_R_RTR_TIMEOUT_CNTL - RW - 32 bits - RCINDC_Reg:0x17			
Field Name	**Bits**	**Default**	**Description**
REG_R_RTR_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the register req RTR timer.
REG_R_RTR_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in REG_R_CLK) how long the RTR must be de-asserted before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1).

Control register for register request RTR timeout

PCIE_TX_SLVCPL_TIMEOUT_CNTL - RW - 32 bits - RCINDC_Reg:0x18			
Field Name	**Bits**	**Default**	**Description**
TX_SLVCPL_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slave cpl timer.
TX_SLVCPL_TIMEOUT_VC	3	0x0	Controls which virtual channel to monitor the cpl, 0: VC0, 1: VC1
TX_SLVCPL_TIMEOUT_VALUE	31:4	0xffff	Value that indicates the # of cycles (in SLV_C_CLK/SLV_S_CCLK) how long to wait for cpl before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1)

Control register for slave completion timeout - snoop channel for RC

PCIE_TX_SLVCPL_NS_TIMEOUT_CNTL - RW - 32 bits - RCINDC_Reg:0x19			
Field Name	**Bits**	**Default**	**Description**
TX_SLVCPL_NS_TIMEOUT_RST (W)	0	0x0	Writing a 1 to this bit resets the slave cpl timer
TX_SLVCPL_NS_TIMEOUT_VC	3	0x0	Controls which channel to monitor the cpl, 0: VC0 1: VC1
TX_SLVCPL_NS_TIMEOUT_VALUE	31:4	0xffff0	Value that indicates the # of cycles (in SLV_C_CLK/SLV_S_CCLK) how long to wait for cpl before an error is flagged. This value is 31:4, bits 3:0 are zero. The min # of cycles is 0x10 (programming this field to 0x1)

Control register for slave completion timeout - non-snoop channel

PCIE_CNTL2 - RW - 32 bits - RCINDC_Reg:0x1C			
Field Name	**Bits**	**Default**	**Description**
TX_ARB_ROUND_ROBIN_EN	0	0x0	TX round-robin arbitration enabled - for RC only
TX_ARB_SLV_LIMIT	5:1	0x0	TX slave arbitration limit
TX_ARB_MST_LIMIT	10:6	0x0	TX master arbitration limit

PCIExpress control register2

PCIE_CI_CNTL - RW - 32 bits - RCINDC_Reg:0x20			
Field Name	**Bits**	**Default**	**Description**
CI_SLAVE_SPLIT_MODE	2	0x0	0=RC - Full completions from Channel A or B 1=RC - Completions split on Channel A and B evenly
CI_SLAVE_GEN_USR_DIS	3	0x0	Sends USR for invalid addresses 0=Sends USR for invalid addresses 1=Disables slave from sending USR, and instead sends a successful CMPLT_D with dummy data.
CI_MST_CMPL_DUMMY_DATA	4	0x1	0xDEADBEEF or 0xFFFFFFFF 0=0xDEADBEEF 1=0xFFFFFFFF
CI_SLV_RC_RD_REQ_SIZE	7:6	0x1	Slave read requests supported size to client. 0=32/64 byte requests supported 1=64 byte requests only 2=16/32/64
CI_SLV_ORDERING_DIS	8	0x0	Disable slave ordering logic 0=Enable slave ordering logic 1=Disable slave ordering logic
CI_RC_ORDERING_DIS	9	0x0	Disable RC ordering logic 0=Enable RC ordering logic 1=Disable RC ordering logic
CI_SLV_CPL_ALLOC_DIS	10	0x0	Slave CPL buffer is sub-divided or not 0=Slave CPL buffer is sub-divided between ports based on number of lanes active 1=Slave CPL buffer is not sub-divided
CI_SLV_CPL_ALLOC_MODE	11	0x0	Slave Cpl buffer method for sub-division. 0 = dynamic 1 = register limits CI_SLV_CPL_STATIC_ALLOC_LIMIT_(N)S
TX_SLV_CPL_DELAY_EN	13	0x0	Enable Delay on Slave Completion Data path. RC only
TX_SLV_CPL_DELAY_TIMER	23:14	0x0	Delay timeout. Effective delay = 7 * TIMER * SLV_S_C_CLK_period
CI_SLV_REQ_DELAY_EN	24	0x0	Enable Delay on Slave Request path

PCIE_CI_CNTL - RW - 32 bits - RCINDC_Reg:0x20			
Field Name	**Bits**	**Default**	**Description**
CI_SLV_REQ_DELAY_TIMER	30:25	0x0	Delay timeout. Effective delay = 4 * TIMER * SLV_R_CLK_period

Chip Interface Control Register

PCIE_BUS_CNTL - RW - 32 bits - RCINDC_Reg:0x21			
Field Name	**Bits**	**Default**	**Description**
BUS_DBL_RESYNC	0	0x1	Double flop the sync module. 0=Normal 1=Add extra resynchronizing clock
PMI_INT_DIS	6	0x0	PMI Interrupt Disable 0=Normal 1=Disable
IMMEDIATE_PMI_DIS	7	0x0	Immediate PMI Disable 0=Enable 1=Disable

PCI Express Bus Control Register

PCIE_LC_STATE6 - R - 32 bits - RCINDC_Reg:0x22			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE24	5:0	0x0	24th previous state
LC_PREV_STATE25	13:8	0x0	25th previous state
LC_PREV_STATE26	21:16	0x0	26th previous state
LC_PREV_STATE27	29:24	0x0	27th previous state

Link Control State Registers

PCIE_LC_STATE7 - R - 32 bits - RCINDC_Reg:0x23			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE28	5:0	0x0	28th previous state
LC_PREV_STATE29	13:8	0x0	29th previous state
LC_PREV_STATE30	21:16	0x0	30th previous state
LC_PREV_STATE31	29:24	0x0	31st previous state

Link Control State Registers

PCIE_LC_STATE8 - R - 32 bits - RCINDC_Reg:0x24			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE32	5:0	0x0	32nd previous state
LC_PREV_STATE33	13:8	0x0	33rd previous state
LC_PREV_STATE34	21:16	0x0	34th previous state
LC_PREV_STATE35	29:24	0x0	35th previous state

Link Control State Registers

PCIE_LC_STATE9 - R - 32 bits - RCINDC_Reg:0x25			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE36	5:0	0x0	36th previous state
LC_PREV_STATE37	13:8	0x0	37th previous state
LC_PREV_STATE38	21:16	0x0	38th previous state
LC_PREV_STATE39	29:24	0x0	39th previous state

Link Control State Registers

PCIE_LC_STATE10 - R - 32 bits - RCINDC_Reg:0x26			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE40	5:0	0x0	40th previous state
LC_PREV_STATE41	13:8	0x0	41st previous state
LC_PREV_STATE42	21:16	0x0	42nd previous state
LC_PREV_STATE43	29:24	0x0	43rd previous state

Link Control State Registers

PCIE_LC_STATE11 - R - 32 bits - RCINDC_Reg:0x27			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE44	5:0	0x0	44th previous state
LC_PREV_STATE45	13:8	0x0	45th previous state
LC_PREV_STATE46	21:16	0x0	46th previous state
LC_PREV_STATE47	29:24	0x0	47th previous state

Link Control State Registers

PCIE_LC_STATUS1 - R - 32 bits - RCINDC_Reg:0x28			
Field Name	**Bits**	**Default**	**Description**
LC_REVERSE_RCVR	0	0x0	Receiver reversal status. When asserted, received data is reversed (i.e. logical lane 0 is not received on physical lane 0)
LC_REVERSE_XMIT	1	0x0	Transmitter reversal status. When asserted, transmitted data is reversed (i.e. logical lane 0 is not transmitted on physical lane 0).
LC_OPERATING_LINK_WIDTH	4:2	0x0	Current width of the Link.
LC_DETECTED_LINK_WIDTH	7:5	0x0	Detected width of the Link. This identifies the maximum possible link width that is physically allowed.

Link Control Status Register 1

PCIE_LC_STATUS2 - R - 32 bits - RCINDC_Reg:0x29			
Field Name	**Bits**	**Default**	**Description**
LC_TOTAL_INACTIVE_LANES	15:0	0x0	Lanes that are not being used.
LC_TURN_ON_LANE	31:16	0x0	Lanes that are available for link width negotiation. Not all available lanes will always be used (actual number depends on lanes supported by other end of the link).

Link Control Status Register 2

PCIE_WPR_CNTL - RW - 32 bits - RCINDC_Reg:0x30			
Field Name	**Bits**	**Default**	**Description**
WPR_RESET_HOT_RST_EN	0	0x1	Enable Hot Reset feature.
WPR_RESET_LNK_DWN_EN	1	0x0	Enable Link down reset feature.
WPR_RESET_LNK_DIS_EN	2	0x1	Enable Link disable reset feature.
WPR_RESET_COR_EN	3	0x0	Enable external CORE reset feature.
WPR_RESET_REG_EN	4	0x0	Enable external REGISTER reset feature.
WPR_RESET_STY_EN	5	0x0	Enable external Stickybit Register reset feature.
WPR_RESET_PHY_EN	6	0x0	Enable external PHY reset feature.

WPR Control Register

PCIE_RX_LAST_TLP0 - R - 32 bits - RCINDC_Reg:0x31			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP0	31:0	0x0	Bits 31:0

Last received TLP

PCIE_RX_LAST_TLP1 - R - 32 bits - RCINDC_Reg:0x32			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP1	31:0	0x0	Bits 63:32

Last received TLP

PCIE_RX_LAST_TLP2 - R - 32 bits - RCINDC_Reg:0x33			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP2	31:0	0x0	Bits 95:64

Last received TLP

PCIE_RX_LAST_TLP3 - R - 32 bits - RCINDC_Reg:0x34			
Field Name	**Bits**	**Default**	**Description**
RX_LAST_TLP3	31:0	0x0	Bits 127:96

Last received TLP

PCIE_TX_LAST_TLP0 - R - 32 bits - RCINDC_Reg:0x35			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP0	31:0	0x0	Bits 31:0

Last transmitted TLP

PCIE_TX_LAST_TLP1 - R - 32 bits - RCINDC_Reg:0x36			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP1	31:0	0x0	Bits 63:32

Last transmitted TLP

PCIE_TX_LAST_TLP2 - R - 32 bits - RCINDC_Reg:0x37			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP2	31:0	0x0	Bits 95:64

Last transmitted TLP

PCIE_TX_LAST_TLP3 - R - 32 bits - RCINDC_Reg:0x38			
Field Name	**Bits**	**Default**	**Description**
TX_LAST_TLP3	31:0	0x0	Bits 127:96

Last transmitted TLP

PCIE_I2C_DEBUG_BUS - R - 32 bits - RCINDC_Reg:0x39			
Field Name	**Bits**	**Default**	**Description**
DEBUG_SEL_BLK1	5:0	0x0	Set Debug Bus Block ID for Debug Block1.
DEBUG_SEL_BLK2	11:6	0x0	Set Debug Bus Block ID for Debug Block2.
DEBUG_MUX_BLK1	17:12	0x0	Set Debug mux number for Debug Block1.
DEBUG_MUX_BLK2	23:18	0x0	Set Debug mux to Debug Block2.
DEBUG_BUS_BLK1	24	0x0	Set upper/lower debug port for Debug Block1.

PCIE_I2C_DEBUG_BUS - R - 32 bits - RCINDC_Reg:0x39			
Field Name	**Bits**	**Default**	**Description**
DEBUG_BUS_BLK2	25	0x0	Upper/lower debug port for Debug Block2.
DEBUG_EN	26	0x0	Enable debug daisy chain.
DEBUG_MULTIBLOCK_EN	27	0x0	Enable multiple debug blocks.
DEBUG_RESERVE	31:28	0x0	RESERVED.

I2C Backdoor Debug Bus Control.

PCIE_I2C_REG_ADDR_EXPAND - RW - 32 bits - RCINDC_Reg:0x3A			
Field Name	**Bits**	**Default**	**Description**
I2C_REG_ADDR (R)	16:0	0x0	Read-only register for reading back the accessing register address
BDI2C_CPLDATA_RTN_EXPAND	20:17	0x0	Retime the cpl_valid for crossing clock domain from REC_C_CLK to REG_R_CLK in I2C backdoor
BDREG_CPLDATA_RTN_EXPAND	24:21	0x3	Retime the REG_READ_REQUEST for crossing clock domain from REG_C_CLK to REG_R_CLK in REG_SYNC.

I2C Register Address Expand

PCIE_I2C_REG_DATA - R - 32 bits - RCINDC_Reg:0x3B			
Field Name	**Bits**	**Default**	**Description**
I2C_REG_DATA	31:0	0x0	Register write/read data.

I2C Register Data Register.

PCIE_CFG_CNTL - RW - 32 bits - RCINDC_Reg:0x3C			
Field Name	**Bits**	**Default**	**Description**
CFG_EN_DEC_TO_GEN2_HIDDEN_REG	0	0x0	Enable decoding of GEN2 hidden registers
CFG_EN_DEC_TO_HIDDEN_REG	1	0x0	Enable decoding of hidden registers (excluding GEN2)

Configuration space control register

PCIE_P_CNTL - RW - 32 bits - RCINDC_Reg:0x40			
Field Name	**Bits**	**Default**	**Description**
P_PWRDN_EN	0	0x0	Enable powering down transmitter and receiver pads along with PLL macros
P_SYMALIGN_MODE	1	0x0	Data Valid generation bit - iMODE = 0 (Relax Mode): update its symbol right away when detect any bit shift, i.e. data_valid will always assert. iMODE = 1 (Aggressive Mode): need confirmation before muxing out the data 0=Relax Mode - Update symbol lock right away when detected bit shifts without waiting for confirmation 1=Aggressive Mode - Always need confirmation for asserting Data Valid
P_ENABLE_PLL_LOCKING_IN_QUICKSIM	2	0x0	Enable actual PLL locking time (30us) when QUICKSIM=1 for simulation purpose. 0=PLL locking time is minimal when QUICKSIM=1 1=Enable normal PLL locking time when QUICKSIM=1
P_PLL_PWRDN_IN_L1L23	3	0x0	Enable PLL powerdown in L1 or L23 Ready states - only if all the associated LC's are in Sates L1 / L23 corresponding to 4 / 2 lanes based on mpConfig and architecture 0=PLL is always running regardless of Link States 1=PLL will be turned off during L1

PCIE_P_CNTL - RW - 32 bits - RCINDC_Reg:0x40			
Field Name	**Bits**	**Default**	**Description**
P_PLL_BUF_PDNB	4	0x1	Disable 10X clock pad on a per PLL basis - should be 1'b0 in order to activate this powersafe feature. 0=Enable PLL Buffer to power down during L1 1=Always keep PLL Buffer running
P_TXCLK_SND_PWRDN	5	0x0	Enable powering down TXCLK clock pads on the transmit side. Each clock pad corresponds to logic associated with 4 lanes.
P_TXCLK_RCV_PWRDN	6	0x0	Enable powering down TXCLK clock pads on the receive side. Each clock pad corresponds to logic associated with 4 lanes.
B_PG2RX_CR_EN_MODE	7	0x0	PHY's CDR Locking (CR_EN) mode 0=CR_EN is LTSSM driven. 1=CR_EN is PHY driven, based on P90_BRX_ELEC_IDLE_ASYNC
P_MASK_RCVR_EIDLE_EN	8	0x0	Enable EIDLE mask for powered down receivers. 0=Don't intercept ELEC_IDLE in power down 1=Intercept ELEC_IDLE in RX power down
P_PLL_PDNB	9	0x1	Enable PLL only (not the buffer) to power down in L1 or L23ready states. 0=Enable PLL to power down during L1 1=Always keep PLL running
P_SYMALIGN_HW_DEBUG	10	0x0	Symbol Alignment HW Debug: 0 = 10-bit compare 1 = 7-bit compare
P_ELASTDESKEW_HW_DEBUG	11	0x0	HW Debug
P_ALLOW_PRX_FRONTEND_SHUTOFF	12	0x0	Enable PHY's RX FRONTEND to shut off during L1 when PLL power down is enabled. 0=RX Frontend is always power on 1=RX Frontend is shutoff during L1 when PLL power down is enabled
P_ALWAYS_USE_FAST_TXCLK	13	0x0	Bypass TXCLK_SWITCH and use 500MHz TXCLK from PLL for both GEN1 and GEN2 speed. 0=TXCLK will be either 250MHz or 500MHz depends on port speeds 1=Bypass TXCLK_SWITCH and always use 500MHz TXCLK
P_ELEC_IDLE_MODE	15:14	0x0	Electrical Idle Mode for PI (Physical Layer). 0=GEN1 - entry:PHY, exit:PHY ; GEN2 - entry:infer, exit:PHY 1=GEN1 - entry:infer, exit:PHY; GEN2 - entry:infer, exit PHY 2=GEN1 - entry:PHY, exit:PHY ; GEN2 - entry:PHY, exit:PHY 3=Reserved
P_CLK_SWITCH_MODE	17:16	0x0	TXCLK Clock Speed Switch mode. 0=None - switch anytime and bypass skid buffer 1=Wait TX idle - switch when TX is idle 2=Enable skid buffer - switch anytime and enable skid buffer 3=reserved
P_RXEN_GATER	27:24	0x2	Clock cycle delay for muxing back RXCLK when RX_EN is re-asserted again.

PHY Control Register

PCIE_P_BUF_STATUS - RW - 32 bits - RCINDC_Reg:0x41			
Field Name	**Bits**	**Default**	**Description**
P_OVERFLOW_ERR	15:0	0x0	Buffer Overflow Status - one bit per lane (RW1C)
P_UNDERFLOW_ERR	31:16	0x0	Buffer Underflow Status - one bit per lane (RW1C)

Elastic-Deskew Buffer Status Register

PCIE_P_DECODER_STATUS – RW - 32 bits - RCINDC_Reg:0x42			
Field Name	**Bits**	**Default**	**Description**
P_DECODE_ERR	15:0	0x0	Decode Error Status - one bit per lane (RW1C)

Decode8b10b Status Register

PCIE_P_MISC_STATUS - RW - 32 bits - RCINDC_Reg:0x43			
Field Name	**Bits**	**Default**	**Description**
P_DESKEW_ERR	7:0	0x0	Deskew Error Status - one bit per port (RW1C)
P_SYMUNLOCK_ERR	31:16	0x0	Symbol Unlock Status - one bit per lane (RW1C)

Miscellaneous Status Register

PCIE_P_PLL_CNTL - RW - 32 bits - RCINDC_Reg:0x44			
Field Name	**Bits**	**Default**	**Description**
P_VCOREF	1:0	0x0	Control signal generation used in calibrating PLLs 0=OFF 1=VDD/4 2=VDD/2 3=3VDD/4
P_CALREF	3:2	0x0	Control signal generation used in calibrating PLLs 0=OFF 1=VDD/2 2=2VDD/3 3=5VDD/6

PHY PLL Control Register

PCIE_P_RCV_L0S_FTS_DET - RW - 32 bits - RCINDC_Reg:0x50			
Field Name	**Bits**	**Default**	**Description**
P_RCV_L0S_FTS_DET_MIN (R)	7:0	0xff	Min # of FTS order set detected during RCV L0s
P_RCV_L0S_FTS_DET_MAX (R)	15:8	0x0	Max # of FTS order set detected during RCV L0s

Number of FTS order set detected during RCV L0s (write to reset)

PCIE_P_IMP_CNTL_STRENGTH - RW - 32 bits - RCINDC_Reg:0x60			
Field Name	**Bits**	**Default**	**Description**
P_TX_STR_CNTL_READ_BACK (R)	3:0	0x0	Store the readback value of current controller
P_TX_IMP_CNTL_READ_BACK (R)	7:4	0x0	Store the readback value of TX impedance controller
P_RX_IMP_CNTL_READ_BACK (R)	11:8	0x0	Store the readback value of RX impedance controller
P_TX_STR_CNTL	19:16	0x7	Set the initial default current strength to 4'b0111
P_TX_IMP_CNTL	23:20	0x6	Default TX impedance control value
P_RX_IMP_CNTL	27:24	0x6	Default RX impedance control value
P_PAD_MANUAL_OVERRIDE	31	0x0	Enable Current and Impedance control values to override 0=Allow normal impedance compensation operation 1=Default to manual settings

PHY IMPEDANCE CONTROL STRENGTH REGISTER

PCIE_P_IMP_CNTL_UPDATE - RW - 32 bits - RCINDC_Reg:0x61			
Field Name	**Bits**	**Default**	**Description**
P_IMP_PAD_UPDATE_RATE	4:0	0xe	PAD's update interval 0=PHY130 default 0xf 1=PHY90 default 0xe
P_IMP_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_IMP_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution
P_IMP_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution

Impedance PAD defaults

PCIE_P_STR_CNTL_UPDATE - RW - 32 bits - RCINDC_Reg:0x62			
Field Name	**Bits**	**Default**	**Description**
P_STR_PAD_UPDATE_RATE	4:0	0xf	PAD's update interval 0=PHY130 default 0xf 1=PHY90 default 0xe
P_STR_PAD_SAMPLE_DELAY	12:8	0x1	Sampling window
P_STR_PAD_INC_THRESHOLD	20:16	0x18	Incremental resolution
P_STR_PAD_DEC_THRESHOLD	28:24	0x8	Decremental resolution

Current PAD defaults

PCIE_P_PAD_MISC_CNTL - RW - 32 bits - RCINDC_Reg:0x63			
Field Name	**Bits**	**Default**	**Description**
P_PAD_I_DUMMYOUT (R)	0	0x0	Input from analog - 0 if PMOS cur is stronger
P_PAD_IMP_DUMMYOUT (R)	1	0x0	Input from analog - 0 if PMOS imp is stronger
P_PAD_IMP_TESTOUT (R)	2	0x0	Input from analog - 1 if NMOS imp is stronger
P_PLLCAL_INC_LOWER_PHASE	6:4	0x1	0=0us 1=1us 2=2us 3=4us 4=8us 5=12us 6=16us 7=24us

Pad Miscellaneous Control Registers

PCIE_P_PAD_FORCE_EN - RW – 32 bits - RCINDC_Reg:0x64			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FEN	7:0	0x0	Force B_PTX_PDNB to enable TX pad
B_PRX_PDNB_FEN	15:8	0x0	Force B_PRX_RDNB to enable RX pad
B_PPLL_PDNB_FEN	19:16	0x0	Force B_PPLL_PDNB to enable PLL

PCIE_P_PAD_FORCE_EN - RW – 32 bits - RCINDC_Reg:0x64			
Field Name	**Bits**	**Default**	**Description**
B_PPLL_BUF_PDNB_FEN	23:20	0x0	Force B_PPLL_BUF_PDNB to enable 10x driver in PLL
B_PI_DREN_FEN (R)	24	0x0	Force B_PI_DREN to enable current calibration pad
B_PBG_PDNB_FEN (R)	25	0x0	Force B_PBG_PDNB to enable Bandgap circuit in current calibration pad
B_PIMP_TX_PDNB_FEN	26	0x0	Force B_PIMP_TX_PDNB to enable TX impedance calibration pad
B_PIMP_RX_PDNB_FEN	27	0x0	Force B_PIMP_RX_PDNB to enable RX impedance calibration pad

Powerdown enable signals used by the wrapper

PCIE_P_PAD_FORCE_DIS - RW - 32 bits - RCINDC_Reg:0x65			
Field Name	**Bits**	**Default**	**Description**
B_PTX_PDNB_FDIS	7:0	0x0	Force B_PTX_PDNB to disable TX pad
B_PRX_PDNB_FDIS	15:8	0x0	Force B_PRX_PDNB to disable RX pad
B_PPLL_PDNB_FDIS	19:16	0x0	Force B_PPLL_PDNB to disable PLL
B_PPLL_BUF_PDNB_FDIS	23:20	0x0	Force B_PPLL_BUF_PDNB to disable 10x driver in PLL
B_PI_DREN_FDIS (R)	24	0x0	Force B_PI_DREN to disable current calibration pad
B_PBG_PDNB_FDIS (R)	25	0x0	Force B_PBG_PDNB to disable Bandgap circuit in current calibration pad
B_PIMP_TX_PDNB_FDIS	26	0x0	Force B_PIMP_TX_PDNB to disable TX impedance calibration pad
B_PIMP_RX_PDNB_FDIS	27	0x0	Force B_PIMP_TX_PDNB to disable RX impedance calibration pad

Powerdown disable signals used by the wrapper

PCIE_PERF_COUNT_CNTL - RW - 32 bits - RCINDC_Reg:0x80			
Field Name	**Bits**	**Default**	**Description**
GLOBAL_COUNT_EN	0	0x0	Global counter stop/start 0=Stop all counters 1=Start all counters
GLOBAL_SHADOW_WR (W)	1	0x0	Global shadow write
GLOBAL_COUNT_RESET (W)	2	0x0	Global counter reset

Performance Counter Control register

PCIE_PERF_CNTL_TXCLK - RW - 32 bits - RCINDC_Reg:0x81			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - TXCLK domain

PCIE_PERF_COUNT0_TXCLK - R - 32 bits - RCINDC_Reg:0x82			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - TXCLK Domain

PCIE_PERF_COUNT1_TXCLK - R - 32 bits - RCINDC_Reg:0x83			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - TXCLK Domain

PCIE_PERF_CNTL_MST_R_CLK - RW - 32 bits - RCINDC_Reg:0x84			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control

PCIE_PERF_COUNT0_MST_R_CLK - R - 32 bits - RCINDC_Reg:0x85			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - MST_R_CLK domain

PCIE_PERF_COUNT1_MST_R_CLK - R - 32 bits - RCINDC_Reg:0x86			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - MST_R_CLK domain

PCIE_PERF_CNTL_MST_C_CLK - RW - 32 bits - RCINDC_Reg:0x87			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - MST_C_CLK domain

PCIE_PERF_COUNT0_MST_C_CLK - R - 32 bits - RCINDC_Reg:0x88			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - MST_C_CLK domain

PCIE_PERF_COUNT1_MST_C_CLK - R - 32 bits - RCINDC_Reg:0x89			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - MST_C_CLK domain

PCIE_PERF_CNTL_SLV_R_CLK - RW - 32 bits - RCINDC_Reg:0x8A			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - SLV_R_CLK

PCIE_PERF_COUNT0_SLV_R_CLK - R - 32 bits - RCINDC_Reg:0x8B			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - SLV_R_CLK domain

PCIE_PERF_COUNT1_SLV_R_CLK - R - 32 bits - RCINDC_Reg:0x8C			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - SLV_R_CLK domain

PCIE_PERF_CNTL_SLV_S_C_CLK - RW - 32 bits - RCINDC_Reg:0x8D			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - SLV_S_C_CLK domain

PCIE_PERF_COUNT0_SLV_S_C_CLK - R - 32 bits - RCINDC_Reg:0x8E			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - SLV_S_C_CLK domain

PCIE_PERF_COUNT1_SLV_S_C_CLK - R - 32 bits - RCINDC_Reg:0x8F			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - SLV_S_C_CLK domain

PCIE_PERF_CNTL_SLV_NS_C_CLK - RW - 32 bits - RCINDC_Reg:0x90			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - SLV_NS_C_CLK domain

PCIE_PERF_COUNT0_SLV_NS_C_CLK - R - 32 bits - RCINDC_Reg:0x91			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - SLV_NS_C_CLK

PCIE_PERF_COUNT1_SLV_NS_C_CLK - R - 32 bits - RCINDC_Reg:0x92			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - SLV_NS_C_CLK

PCIE_PERF_CNTL_EVENT0_PORT_SEL - RW - 32 bits - RCINDC_Reg:0x93			
Field Name	**Bits**	**Default**	**Description**
PERF0_PORT_SEL_TXCLK	3:0	0x0	Select port for TXCLK counters
PERF0_PORT_SEL_MST_R_CLK	7:4	0x0	Select port for MST_R_CLK counters
PERF0_PORT_SEL_MST_C_CLK	11:8	0x0	Select port for MST_C_CLK counters
PERF0_PORT_SEL_SLV_R_CLK	15:12	0x0	Select port for SLV_R_CLK counters
PERF0_PORT_SEL_SLV_S_C_CLK	19:16	0x0	Select port for SLV_S_C_CLK counters
PERF0_PORT_SEL_SLV_NS_C_CLK	23:20	0x0	Select port for SLV_NS_C_CLK counters
PERF0_PORT_SEL_TXCLK2	27:24	0x0	Select port for 2nd TXCLK counters

Performance Counter 0 Port Select Register

PCIE_PERF_CNTL_EVENT1_PORT_SEL - RW - 32 bits - RCINDC_Reg:0x94			
Field Name	**Bits**	**Default**	**Description**
PERF1_PORT_SEL_TXCLK	3:0	0x0	Select port for TXCLK counters
PERF1_PORT_SEL_MST_R_CLK	7:4	0x0	Select port for MST_R_CLK counters
PERF1_PORT_SEL_MST_C_CLK	11:8	0x0	Select port for MST_C_CLK counters
PERF1_PORT_SEL_SLV_R_CLK	15:12	0x0	Select port for SLV_R_CLK counters
PERF1_PORT_SEL_SLV_S_C_CLK	19:16	0x0	Select port for SLV_S_C_CLK counters
PERF1_PORT_SEL_SLV_NS_C_CLK	23:20	0x0	Select port for SLV_NS_C_CLK counters
PERF1_PORT_SEL_TXCLK2	27:24	0x0	Select port for 2nd TXCLK counters

Performance Counter 1 Port Select Register

PCIE_PERF_CNTL_TXCLK2 - RW - 32 bits - RCINDC_Reg:0x95			
Field Name	**Bits**	**Default**	**Description**
EVENT0_SEL	7:0	0x0	Select event for Counter 0
EVENT1_SEL	15:8	0x0	Select event for Counter 1
COUNTER0_UPPER (R)	23:16	0x0	Counter 0 Upper Value (bits 39:32)
COUNTER1_UPPER (R)	31:24	0x0	Counter 1 Upper Value (bits 39:32)

Performance Counter Control - TXCLK domain (2nd set of TXCLK)

PCIE_PERF_COUNT0_TXCLK2 - R - 32 bits - RCINDC_Reg:0x96			
Field Name	**Bits**	**Default**	**Description**
COUNTER0	31:0	0x0	Counter 0 Value (bits 31:0)

Performance Counter 0 - TXCLK Domain

PCIE_PERF_COUNT1_TXCLK2 - R - 32 bits - RCINDC_Reg:0x97			
Field Name	**Bits**	**Default**	**Description**
COUNTER1	31:0	0x0	Counter 1 Value (bits 31:0)

Performance Counter 1 - TXCLK Domain

PCIE_PERF_MAS_ACC_START_LO - RW - 32 bits - RCINDC_Reg:0xA0			
Field Name	**Bits**	**Default**	**Description**
PERF_MAS_ACC_START_LO	31:2	0x0	Start addr value (bits 31:2)

Master access start addr (bits 31:2) for performance event only - master access outside aperture will be counted

PCIE_PERF_MAS_ACC_END_LO - RW - 32 bits - RCINDC_Reg:0xA1			
Field Name	**Bits**	**Default**	**Description**
PERF_MAS_ACC_END_LO	31:2	0x0	End addr value (bits 31:2)

Master access end addr (bits 31:2) aperture for performance event only - master access outside aperture will be counted

PCIE_PERF_MAS_ACC_START_END_HI - RW - 32 bits - RCINDC_Reg:0xA2			
Field Name	**Bits**	**Default**	**Description**
PERF_MAS_ACC_START_HI	7:0	0x0	Start addr upper bits (39:32)
PERF_MAS_ACC_END_HI	15:8	0x0	End addr upper bits (39:32)

Master access upper addr value for performance event only - master access outside aperture will be counted

PCIE_PERF_SLV_ACC_LO - RW - 32 bits - RCINDC_Reg:0xA3			
Field Name	**Bits**	**Default**	**Description**
PERF_SLV_ACC_LO	31:2	0x0	Addr lower bits (31:2)

Slave access addr value for performance counter only - slave access to defined addr will be counted

PCIE_PERF_SLV_ACC_HI - RW - 32 bits - RCINDC_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
PERF_SLV_ACC_HI	31:0	0x0	Upper addr bits(63:32)

Slave access addr value for performance counter only - slave access to defined addr will be counted

PCIE_STRAP_MISC - RW - 32 bits – RCINDC_Reg:0xC0			
Field Name	**Bits**	**Default**	**Description**
STRAP_LINK_CONFIG	3:0	0x0	Provides an override for STRAP_LINK_CONFIG
RESERVED1 (R)	4	0x0	
STRAP_BYPASS_SCRAMBLER	6	0x0	Provides an override for STRAP_BYPASS_SCRAMBLER
STRAP_PHY_RCVRDET_3NF	7	0x0	Provides an override for STRAP_PHY_RCVRDET_3NF

PCIE_STRAP_MISC - RW - 32 bits – RCINDC_Reg:0xC0			
Field Name	**Bits**	**Default**	**Description**
STRAP_F0_AER_EN	8	0x0	Provides an override for STRAP_F0_AER_EN
STRAP_F0_EN	9	0x0	Provides an override for STRAP_F0_EN
STRAP_F0_MSI_EN	10	0x0	Provides an override for STRAP_F0_MSI_EN
STRAP_F0_VC_EN	11	0x0	Provides an override for STRAP_F0_VC_EN
STRAP_F0_LEGACY_DEVICE_TYPE_EN	12	0x0	Provides an override for STRAP_F0_LEGACY_DEVICE_TYPE_EN
STRAP_FIRST_RCVD_ERR_LOG	23	0x0	Provides an override for STRAP_FIRST_RCVD_ERR_LOG 0=FIRST DETECTED ERROR LOGGING 1=FIRST RECEIVED ERROR LOGGING
STRAP_CLK_PM_EN	24	0x0	Provides an override for STRAP_CLK_PM_EN
STRAP_ECN1P1_EN	25	0x0	Provides an override for STRAP_ECN1P1_EN
STRAP_EXT_VC_COUNT	26	0x0	Provides an override for STRAP_EXT_VC_COUNT
RESERVED2 (R)	27	0x0	
STRAP_REVERSE_ALL	28	0x0	Provides an override for STRAP_REVERSE_ALL
STRAP_MST_ADR64_EN	29	0x0	Provides an override for STRAP_MST_ADR64_EN

Misc strap loadable register values

PCIE_STRAP_MISC2 - RW - 32 bits - RCINDC_Reg:0xC1			
Field Name	**Bits**	**Default**	**Description**
STRAP_LINK_BW_NOTIFICATION_CAP_EN	0	0x0	STRAP_LINK_BW_NOTIFICATION_CAP_EN
STRAP_GEN2_COMPLIANCE	1	0x0	Provides an override for STRAP_GEN2_COMPLIANCE
STRAP_MSTCPL_TIMEOUT_EN	2	0x0	Provides an override for STRAP_MSTCPL_TIMEOUT_EN

Misc strap loadable register values 2

PCIE_STRAP_PI - RW - 32 bits - RCINDC_Reg:0xC2			
Field Name	**Bits**	**Default**	**Description**
STRAP_QUICKSIM_START	0	0x0	Provides an override for STRAP_QUICKSIM_START
STRAP_BACKGROUND_IMP_CAL	1	0x0	Provides an override for STRAP_BACKGROUND_IMP_CAL
STRAP_IMP_MANUAL_OVERRIDE	2	0x0	Provides an override for STRAP_IMP_MANUAL_OVERRIDE
STRAP_PAD_RX_MANUAL_IMPEDANCE	6:3	0x0	Provides an override for STRAP_PAD_RX_MANUAL_IMPEDANCE
STRAP_PAD_TX_MANUAL_IMPEDANCE	10:7	0x0	Provides an override for STRAP_PAD_TX_MANUAL_IMPEDANCE
STRAP_STAGGER_CNTL	16:15	0x0	Provides an override for STRAP_STAGGER_CNTL
STRAP_TX_PDNB_MODE	17	0x0	Provides an override for STRAP_TX_PDNB_MODE
STRAP_VCO_MODE	19:18	0x0	Provides an override for STRAP_VCO_MODE
STRAP_INC_PLLCAL_PHASE	24:21	0x0	Provides an override for STRAP_INC_PLLCAL_PHASE
STRAP_PHY_RX_INCAL_FORCE	25	0x0	Provides an override for STRAP_PHY_RX_INCAL_FORCE

PCIE_STRAP_PI - RW - 32 bits - RCINDC_Reg:0xC2			
Field Name	**Bits**	**Default**	**Description**
STRAP_TEST_TOGGLE_PATTERN	28	0x0	Provides an override for STRAP_TEST_TOGGLE_PATTERN
STRAP_TEST_TOGGLE_MODE	29	0x0	Provides an override for STRAP_TEST_TOGGLE_MODE

Misc PI strap loadable register values

PCIE_B_P90_CNTL - RW - 32 bits - RCINDC_Reg:0xC3			
Field Name	**Bits**	**Default**	**Description**
B_P90IMP_BACKUP	3:0	0x0	Impedance Control Backup
B_P90PLL_BACKUP	7:4	0x0	PLL Control Backup

PHY90 Extra Control Registers

PCIE_STRAP_I2C_BD - RW - 32 bits - RCINDC_Reg:0xC4			
Field Name	**Bits**	**Default**	**Description**
STRAP_BIF_I2C_SLV_ADR	6:0	0x0	Provides an override for STRAP_BIF_I2C_SLV_ADR
STRAP_BIF_DBG_I2C_EN	7	0x0	Provides an override for STRAP_BIF_DBG_I2C_EN

I2C Straps

PCIE_P90RX_PRBS10_CNTL - RW - 32 bits - RCINDC_Reg:0xC6			
Field Name	**Bits**	**Default**	**Description**
P90RX_PRBS10_CLR	15:0	0x0	Clear PRBS10_ERRCNT on lane[x]
P90TX_PRBS10_EN	31:16	0x0	Enable PRBS10 checker on lane[x]

PRBS10 Control Register

PCIE_P90_BRX_PRBS10_ER - R - 32 bits - RCINDC_Reg:0xC7			
Field Name	**Bits**	**Default**	**Description**
P90_BRX_PRBS10_ER	15:0	0x0	Status bit indicates that a PRBS10 error has occurred on lane[x]

PRBS10 Error Counter Status

PCIE_PRBS_CLR - RW - 32 bits - RCINDC_Reg:0xC8			
Field Name	**Bits**	**Default**	**Description**
PRBS_CLR	15:0	0x0	Clear PRBS_ERRCNT_x on lane[x]
PRBS_CHECKER_DEBUG_BUS_SELECT	19:16	0x0	Select prbs_chk debug signals of different lanes. 0=Checker 0 debug bus 1=Checker 1 debug bus 2=etc

Clear PRBS Error Counters

PCIE_PRBS_STATUS1 - R - 32 bits - RCINDC_Reg:0xC9			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRSTAT	15:0	0x0	Status bit indicates that a PRBS23 error has occurred on lane[x]
PRBS_LOCKED	31:16	0x0	Status bit indicates that the PRBS pattern has locked on lane[x]

PRBS Status Register

PCIE_PRBS_STATUS2 - R - 32 bits - RCINDC_Reg:0xCA			
Field Name	**Bits**	**Default**	**Description**
PRBS_BITCNT_DONE	15:0	0x0	Indicate PRBS test finished in non-free-run mode for lane[x].

PRBS Status Register2

PCIE_PRBS_FREERUN - RW - 32 bits - RCINDC_Reg:0xCB			
Field Name	**Bits**	**Default**	**Description**
PRBS_FREERUN	15:0	0x0	The PRBS23 error checker is free running on lane[x]

PRBS Freerun Status Register

PCIE_PRBS_MISC - RW - 32 bits - RCINDC_Reg:0xCC			
Field Name	**Bits**	**Default**	**Description**
PRBS_EN	0	0x0	Enable the prbs generator and checkers 0=PRBS GEN disable 1=PRBS GEN enable
PRBS_TEST_MODE	2:1	0x0	Set different test modes: 0=00 - PRBS23 1=01 - PRBS31 2=10 - COUNTER 3=11 - USER DEFINED
PRBS_USER_PATTERN_TOGGLE	3	0x0	Toggle two 8-bit user-defined patterns in 8-bit mode, the 1st pattern is in PRBS_USER_PATTERN[7:0] and the 2nd pattern is in PRBS_USER_PATTERN[15:8]. 0=0 - Replicate user pattern1 1=1 - Toggle user pattern1 and pattern2
PRBS_8BIT_SEL	4	0x0	Set the 8bit and 10bit modes: 0=0 - 10 BIT 1=1 - 8 BIT
PRBS_COMMA_NUM	6:5	0x0	Program the number of COMMA symbols in prbs_gen for recovering bit lock in 8-bit mode. 0=00 - 4 1=01 - 8 2=10 - 16 3=11 - 32
PRBS_LOCK_CNT	11:7	0x0	Program the number of clock cycles for prbs checker to setup bit lock.
PRBS_GEN2_SPEED	15	0x0	Program the signal speed: 0=0 - GEN1 speed 1=1 - GEN2 speed
PRBS_CHK_ERR_MASK	31:16	0x0	Mask PRBS_CHK_ERR output of prbs_chk for lane[x].

PRBS Miscellaneous Control Register

PCIE_PRBS_USER_PATTERN - RW - 32 bits - RCINDC_Reg:0xCD			
Field Name	**Bits**	**Default**	**Description**
PRBS_USER_PATTERN	29:0	0x0	30-bit PRBS User Defined Pattern

PRBS User Defined Pattern

PCIE_PRBS_LO_BITCNT - RW - 32 bits - RCINDC_Reg:0xCE			
Field Name	**Bits**	**Default**	**Description**
PRBS_LO_BITCNT	31:0	0x0	Number of bits to check by the PRBS23 error checkers

PRBS23 Bit Counter Lane 1

PCIE_PRBS_HI_BITCNT - RW - 32 bits - RCINDC_Reg:0xCF			
Field Name	**Bits**	**Default**	**Description**
PRBS_HI_BITCNT	7:0	0x0	Number of bits to check by the PRBS23 error checkers

PRBS23 Bit Counter Lane 1

PCIE_PRBS_ERRCNT_0 - R - 32 bits - RCINDC_Reg:0xD0			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_0	31:0	0x0	Number of errors detected on lane 0

PRBS Error Counter Lane 0

PCIE_PRBS_ERRCNT_1 - R - 32 bits - RCINDC_Reg:0xD1			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_1	31:0	0x0	Number of errors detected on lane 1

PRBS Error Counter Lane 1

PCIE_PRBS_ERRCNT_2 - R - 32 bits - RCINDC_Reg:0xD2			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_2	31:0	0x0	Number of errors detected on lane 2

PRBS Error Counter Lane 2

PCIE_PRBS_ERRCNT_3 - R - 32 bits - RCINDC_Reg:0xD3			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_3	31:0	0x0	Number of errors detected on lane 3

PRBS Error Counter Lane 3

PCIE_PRBS_ERRCNT_4 - R - 32 bits - RCINDC_Reg:0xD4			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_4	31:0	0x0	Number of errors detected on lane 4

PRBS Error Counter Lane 4

PCIE_PRBS_ERRCNT_5 - R - 32 bits - RCINDC_Reg:0xD5			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_5	31:0	0x0	Number of errors detected on lane 5

PRBS Error Counter Lane 5

PCIE_PRBS_ERRCNT_6 - R - 32 bits - RCINDC_Reg:0xD6			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_6	31:0	0x0	Number of errors detected on lane 6

PRBS Error Counter Lane 6

PCIE_PRBS_ERRCNT_7 - R - 32 bits - RCINDC_Reg:0xD7			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_7	31:0	0x0	Number of errors detected on lane 7

PRBS Error Counter Lane 7

PCIE_PRBS_ERRCNT_8 - R - 32 bits - RCINDC_Reg:0xD8			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_8	31:0	0x0	Number of errors detected on lane 8

PRBS Error Counter Lane 8

PCIE_PRBS_ERRCNT_9 - R - 32 bits - RCINDC_Reg:0xD9			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_9	31:0	0x0	Number of errors detected on lane 9

PRBS Error Counter Lane 9

PCIE_PRBS_ERRCNT_10 - R - 32 bits - RCINDC_Reg:0xDA			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_10	31:0	0x0	Number of errors detected on lane 10

PRBS Error Counter Lane 10

PCIE_PRBS_ERRCNT_11 - R - 32 bits - RCINDC_Reg:0xDB			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_11	31:0	0x0	Number of errors detected on lane 11

PRBS Error Counter Lane 11

PCIE_PRBS_ERRCNT_12 - R - 32 bits - RCINDC_Reg:0xDC			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_12	31:0	0x0	Number of errors detected on lane 12

PRBS Error Counter Lane 12

PCIE_PRBS_ERRCNT_13 - R - 32 bits - RCINDC_Reg:0xDD			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_13	31:0	0x0	Number of errors detected on lane 13

PRBS Error Counter Lane 13

PCIE_PRBS_ERRCNT_14 - R - 32 bits - RCINDC_Reg:0xDE			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_14	31:0	0x0	Number of errors detected on lane 14

PRBS Error Counter Lane 14

PCIE_PRBS_ERRCNT_15 - R - 32 bits - RCINDC_Reg:0xDF			
Field Name	**Bits**	**Default**	**Description**
PRBS_ERRCNT_15	31:0	0x0	Number of errors detected on lane 15

PRBS Error Counter Lane 15

4.2.6 RCINDP Registers

Accessing RCINDP registers does not require second level of indirect procedures. Registers in these spaces are addressed through registers AB_INDX/AB_DATA.

To access an RCINDP register, the register address is first written to the RegAddr (AB_INDX[16:0]) and with RegSpace (AB_INDX[31:29]) set to 011. "PortNum" (AB_INDX[25:24]) need to be specified while accessing the RXINDP registers. The "PortNum" is defined to map with the fun-# of the PCIe® bridge that controls the specific GPP port. The specified RCINDP register is then accessed through a read or a write to AB_DATA. A programming example is provided below to illustrate this.

Example: Write TMP to RCINDP:A0h (PortB)

```
OUT AB_INDX, 610000A0h     // Set AB_INDX RegSpace=011, PortNum=01,
RCINDP=A0h
OUT TMP, AB_DATA           // Write TMP to RCINDP:A0h through AB_DATA.
```

Register Name	Address Offset
PCIEP_RESERVED	00h
PCIEP_SCRATCH	01h
PCIEP_HW_DEBUG	02h
PCIEP_PORT_CNTL	10h
PCIE_TX_CNTL	20h
PCIE_TX_REQUESTER_ID	21h
PCIE_TX_VENDOR_SPECIFIC	22h
PCIE_TX_REQUEST_NUM_CNTL	23h
PCIE_TX_SEQ	24h
PCIE_TX_REPLAY	25h
PCIE_TX_ACK_LATENCY_LIMIT	26h
PCIE_TX_CREDITS_ADVT_P	30h
PCIE_TX_CREDITS_ADVT_NP	31h
PCIE_TX_CREDITS_ADVT_CPL	32h
PCIE_TX_CREDITS_INIT_P	33h
PCIE_TX_CREDITS_INIT_NP	34h
PCIE_TX_CREDITS_INIT_CPL	35h
PCIE_TX_CREDITS_STATUS	36h
PCIE_TX_CREDITS_FCU_THRESHOLD	37h
PCIE_P_PORT_LANE_STATUS	50h
PCIE_FC_P	60h
PCIE_FC_NP	61h
PCIE_FC_CPL	62h
PCIE_ERR_CNTL	6Ah
PCIE_RX_CNTL	70h
PCIE_RX_EXPECTED_SEQNUM	71h
PCIE_RX_VENDOR_SPECIFIC	72h
PCIE_RX_CREDITS_ALLOCATED_P	80h
PCIE_RX_CREDITS_ALLOCATED_NP	81h
PCIE_RX_CREDITS_ALLOCATED_CPL	82h
PCIE_RX_CREDITS_RECEIVED_P	83h
PCIE_RX_CREDITS_RECEIVED_NP	84h
PCIE_RX_CREDITS_RECEIVED_CPL	85h
PCIE_LC_CNTL	A0h
PCIE_LC_TRAINING_CNTL	A1h

Register Name	Address Offset
PCIE_LC_LINK_WIDTH_CNTL	A2h
PCIE_LC_N_FTS_CNTL	A3h
PCIE_LC_SPEED_CNTL	A4h
PCIE_LC_STATE0	A5h
PCIE_LC_STATE1	A6h
PCIE_LC_STATE2	A7h
PCIE_LC_STATE3	A8h
PCIE_LC_STATE4	A9h
PCIE_LC_STATE5	AAh
PCIE_LC_CNTL2	B1h
PCIE_LC_BW_CHANGE_CNTL	B2h
PCIE_LC_CDR_CNTL	B3h
PCIE_LC_LANE_CNTL	B4h
PCIE_LC_CNTL3	B5h
PCIEP_STRAP_LC	C0h
PCIEP_STRAP_MISC	C1h

PCIEP_RESERVED - R - 32 bits - RCINDP_Reg:0x0			
Field Name	**Bits**	**Default**	**Description**
PCIEP_RESERVED	31:0	0xffffffff	RESERVED

Reserved

PCIEP_SCRATCH - RW - 32 bits - RCINDP_Reg:0x1			
Field Name	**Bits**	**Default**	**Description**
PCIEP_SCRATCH	31:0	0x0	Scratch Register

Scratch Register

PCIEP_HW_DEBUG - RW - 32 bits - RCINDP_Reg:0x2			
Field Name	**Bits**	**Default**	**Description**
HW_00_DEBUG	0	0x0	bit0
HW_01_DEBUG	1	0x0	bit1
HW_02_DEBUG	2	0x0	bit2
HW_03_DEBUG	3	0x0	bit3
HW_04_DEBUG	4	0x0	bit4
HW_05_DEBUG	5	0x0	bit5
HW_06_DEBUG	6	0x0	bit6
HW_07_DEBUG	7	0x0	bit7
HW_08_DEBUG	8	0x0	bit8
HW_09_DEBUG	9	0x0	bit9
HW_10_DEBUG	10	0x0	bit10
HW_11_DEBUG	11	0x0	bit11
HW_12_DEBUG	12	0x0	bit12
HW_13_DEBUG	13	0x0	bit13
HW_14_DEBUG	14	0x0	REGS_LC_NO_TSx_PAD_RCVD_DIS: Training sets can contain link and lane numbers set to PAD when transitioning from Polling.Active to Detect.Idle.
HW_15_DEBUG	15	0x0	REGS_LC_ALLOW_TX_L1_CONTROL: Allow TX to prevent LC from going to L1 when there are outstanding completions.

Hardware Debug Register

PCIEP_PORT_CNTL - RW - 32 bits - RCINDP_Reg:0x10			
Field Name	**Bits**	**Default**	**Description**
SLV_PORT_REQ_EN	0	0x1	Suspend all slave requests to client 0=Allow slave to be suspended 1=Ignore slave suspend signal
CI_SNOOP_OVERRIDE	1	0x0	Force all slave requests to be snoop requests 0=Do not force all slave requests to be snoop requests 1=Force all slave requests to be snoop requests
HOTPLUG_MSG_EN	2	0x0	Enable hot-plug messages 0=Disable hot-plug messages 1=Enable hot-plug messages
NATIVE_PME_EN	3	0x1	Enable native PME 0=Disable native PME 1=Enable native PME
PWR_FAULT_EN	4	0x0	Enable power fault detection. 0=Disable 1=Enable
PMI_BM_DIS	5	0x0	Disable bus master for power saving state. 0=Normal 1=Disable
SEQNUM_DEBUG_MODE	6	0x0	Enable debug sequence number 0=Normal operation 1=Enable debug sequence number test mode
CI_SLV_CPL_STATIC_ALLOC_LIMIT_S	14:8	0x0	Limit for outstanding Slave Snooped Non-Posted request to Slave, 0=128
CI_SLV_CPL_STATIC_ALLOC_LIMIT_NS	22:16	0x0	Limit for outstanding Slave Non-Snooped Non-Posted request to Slave, 0=128

Port Control Register

PCIE_TX_CNTL - RW - 32 bits - RCINDP_Reg:0x20			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM_COUNT (R)	9:0	0x0	TX Replay Number Counter - counter to keep track of the number of replays that have occurred
TX_SNR_OVERRIDE	11:10	0x0	Snoop Not Required Override - control of the Snoop bit for master requests 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_RO_OVERRIDE	13:12	0x0	Relaxed Ordering Override - control relaxed ordering bit for master requests 0=Generate bit as normal 1=Override equation, and always set bit 2=Override equation, and always clear bit 3=Invalid
TX_PACK_PACKET_DIS	14	0x0	Packet Packing Disable - back-to-back packing of TLP and DLLP 0=Place packets as close as allowable 1=Place STP/SDP in lane 0 only
TX_GAP_BTW_PKTS	18:16	0x0	Number of idle cycles between DLLP and TLP
TX_FLUSH_TLP_DIS	19	0x1	Disable flushing TLPs when Data Link is down 0=Normal 1=Disable
TX_CPL_PASS_P	20	0x1	Ordering rule: Let Completion Pass Posted 0=no pass 1=CPL pass

PCIE_TX_CNTL - RW - 32 bits - RCINDP_Reg:0x20			
Field Name	**Bits**	**Default**	**Description**
TX_NP_PASS_P	21	0x0	Ordering rule: Let Non-Posted Pass Posted 0=no pass 1=NP pass
TX_CLEAR_EXTRA_PM_REQS	22	0x1	Enable to clear excess PM DLLPs from pipe 0=Traditional PM request behaviour 1=Clear PM DLLPs from pipe when link transitions from L1_Entry or L23_Entry to Rcv_L0
TX_FC_UPDATE_TIMEOUT_SEL	25:24	0x2	To adjust the length of the timeout interval before sending out flow control update 0=Disable flow control 1=4x clock cycle 2=1024x clock cycle 3=4096x clock cycle
TX_FC_UPDATE_TIMEOUT	31:26	0x7	Interval length to send flow control update

TX Control Register

PCIE_TX_REQUESTER_ID - RW - 32 bits - RCINDP_Reg:0x21			
Field Name	**Bits**	**Default**	**Description**
TX_REQUESTER_ID_FUNCTION (R)	2:0	0x0	Function ID of Requester for Master transactions or Completer for Slave Completions
TX_REQUESTER_ID_DEVICE	7:3	0x0	Device ID of Requester for Master transactions or Completer for Slave Completions
TX_REQUESTER_ID_BUS	15:8	0x0	Bus ID of Requester for Master transactions or Completer for Slave Completions

TX Requester ID Register

PCIE_TX_VENDOR_SPECIFIC - RW - 32 bits - RCINDP_Reg:0x22			
Field Name	**Bits**	**Default**	**Description**
TX_VENDOR_DATA	23:0	0x0	Writing to this register generates a Vendor Specific DLLP using Vendor Data for the payload

TX Vendor Specific DLLP

PCIE_TX_REQUEST_NUM_CNTL - RW - 32 bits - RCINDP_Reg:0x23			
Field Name	**Bits**	**Default**	**Description**
TX_NUM_OUTSTANDING_NP	29:24	0x2	Number of Non-posted (VC0 and VC1) requests sent out before completion
TX_NUM_OUTSTANDING_NP_VC1_EN	30	0x0	Enable for number of Non-posted VC1 requests sent out before completion
TX_NUM_OUTSTANDING_NP_EN	31	0x0	Enable for number of Non-posted requests sent out before completion

TX Request Num Control Register

PCIE_TX_SEQ - R - 32 bits - RCINDP_Reg:0x24			
Field Name	**Bits**	**Default**	**Description**
TX_NEXT_TRANSMIT_SEQ	11:0	0x0	Next Transmit Sequence Number to send out
TX_ACKD_SEQ	27:16	0x0	Last Acknowledged Sequence Number

TX Sequence Register

PCIE_TX_REPLAY - RW - 32 bits - RCINDP_Reg:0x25			
Field Name	**Bits**	**Default**	**Description**
TX_REPLAY_NUM	9:0	0x3	Register to control Replay Number before Link goes to Retrain
TX_REPLAY_TIMER_OVERWRITE	15	0x0	Trigger for Replay Timer
TX_REPLAY_TIMER	31:16	0x90	Replay Timer - when expired do Replay

TX Replay Register

PCIE_TX_ACK_LATENCY_LIMIT - RW - 32 bits - RCINDP_Reg:0x26			
Field Name	**Bits**	**Default**	**Description**
TX_ACK_LATENCY_LIMIT	7:0	0x0	ACK Latency Limit for scheduling ACK DLLP transmission
TX_ACK_LATENCY_LIMIT_OVERWRITE	8	0x0	Use register value instead of hardware value from link width

TX ACK Latency Limit

PCIE_TX_CREDITS_ADVT_P - R - 32 bits - RCINDP_Reg:0x30			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_PD	11:0	0x0	Posted data credits
TX_CREDITS_ADVT_PH	23:16	0x0	Posted header credits

Posted advertised credits

PCIE_TX_CREDITS_ADVT_NP - R - 32 bits - RCINDP_Reg:0x31			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_NPD	11:0	0x0	Non-posted data credits
TX_CREDITS_ADVT_NPH	23:16	0x0	Non-posted header credits

Non-posted advertised credits

PCIE_TX_CREDITS_ADVT_CPL - R - 32 bits - RCINDP_Reg:0x32			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ADVT_CPLD	11:0	0x0	Completion data credits
TX_CREDITS_ADVT_CPLH	23:16	0x0	Completion header credits

Completion advertised credits

PCIE_TX_CREDITS_INIT_P - R - 32 bits - RCINDP_Reg:0x33			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_PD	11:0	0x0	Posted data credits
TX_CREDITS_INIT_PH	23:16	0x0	Posted header credits

Posted initial credits

PCIE_TX_CREDITS_INIT_NP - R - 32 bits - RCINDP_Reg:0x34			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_NPD	11:0	0x0	Non-posted data credits
TX_CREDITS_INIT_NPH	23:16	0x0	Non-posted header credits

Non-posted initial credits

PCIE_TX_CREDITS_INIT_CPL - R - 32 bits - RCINDP_Reg:0x35			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_INIT_CPLD	11:0	0x0	Completion data credits
TX_CREDITS_INIT_CPLH	23:16	0x0	Completion header credits

Completion initial credits

PCIE_TX_CREDITS_STATUS - RW - 32 bits - RCINDP_Reg:0x36			
Field Name	**Bits**	**Default**	**Description**
TX_CREDITS_ERR_PD	0	0x0	RW1C - Posted Data Credits Error
TX_CREDITS_ERR_PH	1	0x0	RW1C - Posted Header Credits Error
TX_CREDITS_ERR_NPD	2	0x0	RW1C - Non-posted Data Credits Error
TX_CREDITS_ERR_NPH	3	0x0	RW1C - Non-posted Header Credits Error
TX_CREDITS_ERR_CPLD	4	0x0	RW1C - Cpl Data Credits Error
TX_CREDITS_ERR_CPLH	5	0x0	RW1C - Cpl Header Credits Error
TX_CREDITS_CUR_STATUS_PD (R)	16	0x0	The current status of the posted data credits
TX_CREDITS_CUR_STATUS_PH (R)	17	0x0	The current status of the posted header credits
TX_CREDITS_CUR_STATUS_NPD (R)	18	0x0	The current status of the non-posted data credits
TX_CREDITS_CUR_STATUS_NPH (R)	19	0x0	The current status of the non-posted header credits
TX_CREDITS_CUR_STATUS_CPLD (R)	20	0x0	The current status of the cpl data credits
TX_CREDITS_CUR_STATUS_CPLH (R)	21	0x0	The current status of the cpl header credits

TX Credits status. When set to 1, remaining credits > init credits. Status bit will remain 1 until a 1 is written to it.

PCIE_TX_CREDITS_FCU_THRESHOLD - RW - 32 bits - RCINDP_Reg:0x37			
Field Name	**Bits**	**Default**	**Description**
TX_FCU_THRESHOLD_P_VC0	2:0	0x3	For VC0 posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1

PCIE_TX_CREDITS_FCU_THRESHOLD - RW - 32 bits - RCINDP_Reg:0x37			
Field Name	**Bits**	**Default**	**Description**
TX_FCU_THRESHOLD_NP_VC0	6:4	0x3	For VC0 non-posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_CPL_VC0	10:8	0x3	For VC0 completion header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_P_VC1	18:16	0x3	For VC1 posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_NP_VC1	22:20	0x3	For VC1 non-posted header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1
TX_FCU_THRESHOLD_CPL_VC1	26:24	0x3	For VC1 completion header/data credits, fraction of (pending flow control updates / total flow control credits) before urgent DLLP flag is set. 0=0 1=1/16 2=1/8 3=1/4 4=1/2 5=3/4 6=7/8 7=1

TX Credits Flow Control Update Threshold

PCIE_P_PORT_LANE_STATUS - RW - 32 bits - RCINDP_Reg:0x50			
Field Name	**Bits**	**Default**	**Description**
PORT_LANE_REVERSAL (R)	0	0x0	Reverse lanes and control signals associated with a port 0=Port Lane order is normal 1=Port Lane order is reversed
PHY_LINK_WIDTH (R)	6:1	0x0	Link Width 0=6'b00_0000 disabled 1=6'b00_0001 x1 2=6'b00_0010 x2 3=6'b00_0100 x4 4=6'b00_1000 x8 5=6'b01_0000 x12 6=6'b10_0000 x16

Port-Lane Status Register

PCIE_FC_P - RW - 32 bits - RCINDP_Reg:0x60			
Field Name	**Bits**	**Default**	**Description**
PD_CREDITS	7:0	0x8	Posted Data Flow Control Advertised Credits
PH_CREDITS	15:8	0x2	Posted Header Flow Control Advertised Credits

Posted Flow Control Registers

PCIE_FC_NP - RW - 32 bits - RCINDP_Reg:0x61			
Field Name	**Bits**	**Default**	**Description**
NPD_CREDITS	7:0	0x2	Non-Posted Data Flow Control Advertised Credits
NPH_CREDITS	15:8	0x2	Non-Posted Header Flow Control Advertised Credits

Non-Posted Flow Control Registers

PCIE_FC_CPL - RW - 32 bits - RCINDP_Reg:0x62			
Field Name	**Bits**	**Default**	**Description**
CPLD_CREDITS	7:0	0x0	Completion Data Flow Control Credits
CPLH_CREDITS	15:8	0x0	Completion Header Flow Control Credits

Completion Flow Control Registers

PCIE_ERR_CNTL - RW - 32 bits - RCINDP_Reg:0x6A			
Field Name	**Bits**	**Default**	**Description**
ERR_REPORTING_DIS	0	0x0	Disable PCI Express Advanced Error Reporting
TX_GENERATE_LCRC_ERR (W)	4	0x0	Generate LCRC error for the next transmitted TLP.
RX_GENERATE_LCRC_ERR (W)	5	0x0	Generate LCRC error for the next received TLP.
TX_GENERATE_ECRC_ERR (W)	6	0x0	Generate ECRC error for the next transmitted TLP.
RX_GENERATE_ECRC_ERR (W)	7	0x0	Generate ECRC error for the next received TLP.

Error Control Registers

PCIE_RX_CNTL - RW - 32 bits - RCINDP_Reg:0x70			
Field Name	**Bits**	**Default**	**Description**
RX_IGNORE_IO_ERR	0	0x0	Ignore Malformed I/O TLP Errors
RX_IGNORE_BE_ERR	1	0x0	Ignore Malformed Byte Enable TLP Errors
RX_IGNORE_MSG_ERR	2	0x0	Ignore Malformed Message Error

PCIE_RX_CNTL - RW - 32 bits - RCINDP_Reg:0x70			
Field Name	**Bits**	**Default**	**Description**
RX_IGNORE_CRC_ERR (R)	3	0x0	Ignore CRC Errors
RX_IGNORE_CFG_ERR	4	0x0	Ignore Malformed Configuration Errors
RX_IGNORE_CPL_ERR	5	0x0	Ignore Malformed Completion Errors
RX_IGNORE_EP_ERR	6	0x0	Ignore Malformed EP Errors
RX_IGNORE_LEN_MISMATCH_ERR	7	0x0	Ignore Malformed Length Mismatch Errors
RX_IGNORE_MAX_PAYLOAD_ERR	8	0x0	Ignore Malformed Maximum Payload Errors
RX_IGNORE_TC_ERR	9	0x0	Ignore Malformed Traffic Class Errors
RX_IGNORE_CFG_UR	10	0x0	RESERVED
RX_IGNORE_IO_UR	11	0x0	RESERVED
RX_IGNORE_VEND0_UR	12	0x0	Ignore Vendor Type 0 Messages
RX_NAK_IF_FIFO_FULL (R)	13	0x0	Send NAK if RX internal FIFO is full
RX_GEN_ONE_NAK	14	0x1	Generate NAK only for the first bad packet until replayed
RX_FC_INIT_FROM_REG	15	0x0	Flow Control Initialization from registers 0=Init FC from FIFO sizes 1=Init FC from registers
RX_RCB_CPL_TIMEOUT	18:16	0x0	RCB cpl timeout 0=Disable 1=50us 2=10ms 3=25ms 4=50ms 5=100ms 6=500ms 7=1ms
RX_RCB_CPL_TIMEOUT_MODE	19	0x0	RCB CPL timeout on link down
RX_PCIE_CPL_TIMEOUT_DIS	20	0x0	PCIe® CPL timeout on link down disable 1: Disable the timeout feature

RX Control Register

PCIE_RX_EXPECTED_SEQNUM - R - 32 bits - RCINDP_Reg:0x71			
Field Name	**Bits**	**Default**	**Description**
RX_EXPECTED_SEQNUM	11:0	0x0	Next expected sequence number

RX Next Expected Sequence Number Register

PCIE_RX_VENDOR_SPECIFIC - R - 32 bits - RCINDP_Reg:0x72			
Field Name	**Bits**	**Default**	**Description**
RX_VENDOR_DATA	23:0	0x0	Writing to this register will re-arm to capture the next Vendor Specific DLLP
RX_VENDOR_STATUS	24	0x0	Indicates that a Vendor Specific DLLP was decoded, and Vendor Data was captured

RX Vendor Specific DLLP

PCIE_RX_CREDITS_ALLOCATED_P - R - 32 bits - RCINDP_Reg:0x80			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_PD	11:0	0x0	For posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_PH	23:16	0x0	For posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256

RX Credits Allocated Register (Posted)

PCIE_RX_CREDITS_ALLOCATED_NP - R - 32 bits - RCINDP_Reg:0x81			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units granted to transmitter since initialization, modulo 256

RX Credits Allocated Register (Non-Posted)

PCIE_RX_CREDITS_ALLOCATED_CPL - R - 32 bits - RCINDP_Reg:0x82			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_ALLOCATED_CPLD	11:0	0x0	For completion TLP data, the number of FC units granted to transmitter since initialization, modulo 4096
RX_CREDITS_ALLOCATED_CPLH	23:16	0x0	For completion TLP header, the number of FC units granted to transmitter since initialization, modulo 256

RX Credits Allocated Register (Completion)

PCIE_RX_CREDITS_RECEIVED_P - R - 32 bits - RCINDP_Reg:0x83			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_PD	11:0	0x0	For posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096
RX_CREDITS_RECEIVED_PH	23:16	0x0	For posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256

RX Credits Received Register (Posted)

PCIE_RX_CREDITS_RECEIVED_NP - R - 32 bits - RCINDP_Reg:0x84			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_NPD	11:0	0x0	For non-posted TLP data, the number of FC units consumed by valid TLP received since initialization, modulo 4096
RX_CREDITS_RECEIVED_NPH	23:16	0x0	For non-posted TLP header, the number of FC units consumed by valid TLP received since initialization, modulo 256

RX Credits Received Register (Non-Posted)

PCIE_RX_CREDITS_RECEIVED_CPL - R - 32 bits - RCINDP_Reg:0x85			
Field Name	**Bits**	**Default**	**Description**
RX_CREDITS_RECEIVED_CPLD	11:0	0x0	For completion TLP data, the number of FC units consumed by valid TLP received since initialization, module 4096
RX_CREDITS_RECEIVED_CPLH	23:16	0x0	For completion TLP header, the number of FC units consumed by valid TLP received since initialization, module 256.

RX Credits Received Register (Completion)

PCIE_LC_CNTL - RW - 32 bits - RCINDP_Reg:0xA0			
Field Name	**Bits**	**Default**	**Description**
LC_CM_HI_ENABLE_COUNT	0	0x0	Enable count for CM_HIGH - when transmitter is to be turned on stop when the counter reaches CM_HI_COUNT_LIMIT_ON. If number of lanes = 1 or 2: CM_HI_COUNT_LIMIT_ON = 12 or 10. If number of lanes = 3 or 4: CM_HI_COUNT_LIMIT_ON = 10 or 12. If number of lanes > 4: CM_HI_COUNT_LIMIT_ON = 10 or 15.
LC_DONT_ENTER_L23_IN_D0	1	0x0	Do not enter L23 in D0 state.
LC_RESET_L_IDLE_COUNT_EN	2	0x0	Enable reset of electrical idle counter.
LC_RESET_LINK	3	0x0	Reset an individual link without resetting the other ports.
LC_16X_CLEAR_TX_PIPE	7:4	0x5	Adjust the time that the LC waits for the pipe to be idle. Setting this field to 0 results in the maximum time. Otherwise, the delay increases as this field is incremented.
LC_L0S_INACTIVITY	11:8	0x0	L0s inactivity timer setting 0=L0s is disabled 1=40ns 2=80ns 3=120ns 4=200ns 5=400ns 6=1us 7=2us 8=4us 9=10us 10=40us 11=100us 12=400us 13=1ms 14=4ms
LC_L1_INACTIVITY	15:12	0x0	L1 inactivity timer setting 0=L1 is disabled 1=1us 2=2us 3=4us 4=10us 5=20us 6=40us 7=100us 8=400us 9=1ms 10=4ms 11=10ms 12=40ms 13=100ms 14=400ms
LC_PMI_TO_L1_DIS	16	0x0	Disable the transition to L1 caused by programming PMI_STATE to non-D0
LC_INC_N_FTS_EN	17	0x0	Enable incrementing N_FTS for each transition to recovery
LC_LOOK_FOR_IDLE_IN_L1L23	19:18	0x0	Controls the number of clocks to wait for Electrical Idle set in L1, L23 0=250 1=100 2=10000 3=3000000
LC_FACTOR_IN_EXT_SYNC	20	0x0	Factor in the extended sync bit in the calculation for the replay timer adjustment

PCIE_LC_CNTL - RW - 32 bits - RCINDP_Reg:0xA0			
Field Name	**Bits**	**Default**	**Description**
LC_WAIT_FOR_PM_ACK_DIS	21	0x0	Disables waiting for PM_ACK in L23 ready entry handshake
LC_WAKE_FROM_L23	22	0x0	For upstream component, wake the link from L23 ready
LC_L1_IMMEDIATE_ACK	23	0x0	Always ACK an ASPM L1 entry DLLP (i.e. never generate PM_NAK)
LC_ASPM_TO_L1_DIS	24	0x0	Disable ASPM L1
LC_DELAY_COUNT	26:25	0x0	Controls minimum amount of time to stay in L0s or L1 0=255/ 4095 (Power-down) 1=1250 / 16383 (Power-down) 2=5000/ 65535 (Power-down) 3=25000 / 262143 (Power-down)
LC_DELAY_L0S_EXIT	27	0x0	Enable staying in L0s for a minimum time
LC_DELAY_L1_EXIT	28	0x0	Enable staying in L1 for a minimum time
LC_EXTEND_WAIT_FOR_EL_IDLE	29	0x1	Wait for Electrical idle in L1/L23 ready value
LC_ESCAPE_L1L23_EN	30	0x1	Enable L1/L23 entry escape arcs
LC_GATE_RCVR_IDLE	31	0x0	Ignore PHY Electrical idle detector 0=LC will look for PE_LC_IdleDetected 1=To gate off PE_LC_IdleDetected to LC, so that LC never sees receivers enter EIDLE

Link Control Register

PCIE_LC_TRAINING_CNTL - RW - 32 bits - RCINDP_Reg:0xA1			
Field Name	**Bits**	**Default**	**Description**
LC_TRAINING_CNTL	3:0	0x0	Training control bits in training sets - 0:Reserved, 1:Disable Link, 2:Loopback, 3:Disable Scrambling. The training control signal will be asserted in the TS when the associated bit is set to 1.
LC_COMPLIANCE_RECEIVE	4	0x0	Control for the Compliance Receive bit in Training Sequence 1 Ordered Sets.
LC_LOOK_FOR_MORE_NON_MATCHING_TS1	5	0x0	Look for more non-matching TS1 ordered sets.
LC_L0S_L1_TRAINING_CNTL_EN	6	0x0	Enable transition from L0s & L1 to Recovery if a Hot Reset or Link Disable is initiated.
LC_L1_LONG_WAKE_FIX_EN	7	0x1	Enable fix for FTS going to L1 problem
LC_POWER_STATE (R)	10:8	0x0	Link Power state
LC_DONT_GO_TO_L0S_IF_L1_ARMED	11	0x0	Prevent the LTSSM from going to Rcv_L0s if it has already acknowledged a request to go to L1 but it hasn't transitioned there yet.
LC_INIT_SPD_CHG_WITH_CSR_EN	12	0x1	Control PCIe® 2.0 clause that states that directed_speed_change should be set if the Retrain Link bit is set to 1 and the Target Link Speed is not equal to the current link speed. 0=Speed negotiation will not be initiated by RETRAIN_LINK Configuration bit. 1=Speed Negotiation can be initiated if RETRAIN_LINK is set and Target Link Speed does not equal the current link speed.
LC_EXTEND_WAIT_FOR_SKP	16	0x1	Extend the timer when in Rcv_L0s_Skp state. Bit is inverted before being used.
LC_AUTONOMOUS_CHANGE_OFF	17	0x0	'Autonomous Change' Data Rate Identifier Control 0='Autonomous Change' is reported as defined in the PCIE 2.0 specification. 1=Do not report 'Autonomous Change'.

PCIE_LC_TRAINING_CNTL - RW - 32 bits - RCINDP_Reg:0xA1			
Field Name	**Bits**	**Default**	**Description**
LC_UPCONFIGURE_CAP_OFF	18	0x0	'Upconfigure Capability' Data Rate Identifier Control 0='Upconfigure Capability' is reported as defined in the PCIE 2.0 specification. 1=Do not report 'Upconfigure Capability'.
LC_HW_LINK_DIS_EN	19	0x0	Control for the HW or Chip-induced Link Disable feature. Applies to RC only. 0=Allow chip to force link to Link Disable. 1=Turn off chip-induced Link Disable.
LC_LINK_DIS_BY_HW	20	0x0	HW or Chip-induced Link Disable status. Note that this bit is Sticky & RW1C. 0=Chip forced Link to the Link Disable state. 1=Chip-induced Link Disable cleared or never happened.
LC_STATIC_TX_PIPE_COUNT_EN	21	0x0	Use the same WAIT_FOR_EMPTY_PIPE values for all link widths when going to L1 or L23.
LC_ASPM_L1_NAK_TIMER_SEL	23:22	0x0	Select timer value to be used when a request to go to L1 is declined i.e. NAK is sent. 0=9.5us 1=3.2us 2=1.6us 3=0.8us
LC_DONT_DEASSERT_RX_EN_IN_R_SPEED	24	0x0	To prevent deassertion of RX_EN during Recovery.Speed.
LC_DONT_DEASSERT_RX_EN_IN_TEST	25	0x0	To prevent deassertion of RX_EN during Polling.Compliance and Loopback.
LC_RESET_ASPM_L1_NAK_TIMER	26	0x1	Prevent L1 Nak Counter from being continuously reset before it has expired (i.e. reached 9.5us) if additional ASPM L1 requests received. 0=Don't reset the 9.5us L1 Nak Counter if additional ASPM L1 requests received. 1=Reset the 9.5us L1 Nak Counter if additional ASPM L1 requests received before counter finishes.
LC_DEBUG_1	27	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_2	28	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_3	29	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_4	30	0x0	Added this bit in case fields needed after registers are frozen.
LC_DEBUG_5	31	0x0	Added this bit in case fields needed after registers are frozen.

LC Training Control Register

PCIE_LC_LINK_WIDTH_CNTL - RW - 32 bits - RCINDP_Reg:0xA2			
Field Name	**Bits**	**Default**	**Description**
LC_LINK_WIDTH	2:0	0x6	Link width required.
LC_LINK_WIDTH_RD (R)	6:4	0x0	Read back link width
LC_RECONFIG_ARC_MISSING_ESCAPE	7	0x0	Expedite transition from Recovery.Idle to Detect during a long reconfiguration.
LC_RECONFIG_NOW	8	0x0	Initiate link width change.
LC_RENEGOTIATION_SUPPORT (R)	9	0x0	Advertise link width renegotiation support. 0=Other end does not support link width renegotiation. 1=Other end does support link width renegotiation.
LC_RENEGOTIATE_EN	10	0x0	Enable re-negotiation.
LC_SHORT_RECONFIG_EN	11	0x0	Enable short reconfiguration.
LC_UPCONFIGURE_SUPPORT	12	0x0	Control for the PCIe® 2.0 defined link width change.
LC_UPCONFIGURE_DIS	13	0x0	Override all other control signals of the PCIe 2.0 defined link width change feature.

PCIE_LC_LINK_WIDTH_CNTL - RW - 32 bits - RCINDP_Reg:0xA2			
Field Name	**Bits**	**Default**	**Description**
LC_UPCFG_WAIT_FOR_RCVR_DIS	14	0x0	Disable waiting for all receivers during a link width upconfigure. 0=Enable 1=Disable
LC_UPCFG_TIMER_SEL	15	0x0	Time that state machine waits to receive TS on all receivers during a link width upconfigure. 0=1 msec 1=use LC_WAIT_FOR_LANES_IN_LW_NEG values
LC_DEASSERT_TX_PDNB	16	0x0	TX_PDNB Control for unused lanes 0=Keep TX_PDNB asserts for unused lanes. 1=Deassert TX_PDNB for unused lanes
LC_L1_RECONFIG_EN	17	0x0	Control for link width change in L1 state. 0=Link width reconfiguration can not be initiated from L1. 1=Link width reconfiguration can be initiated from L1.
LC_DYNLINK_MST_EN	18	0x0	HW initiated link width change feature. 0=Disable 1=Enable HW initiated link width change interface
LC_DUAL_END_RECONFIG_EN	19	0x0	Control Link Width Reconfiguration so that either end is allowed to initiate a link width change to the maximum supported width when the other end has initiated a change to a smaller link width. 0=Allow single end link reconfiguration 1=Allow link width reconfiguration to be simultaneously initiated by either end of the Link
LC_UPCONFIGURE_CAPABLE (R)	20	0x0	Represents upconfigure_capable variable defined in the PCIe® 2.0 specification. 0=PCIe 2.0 Upconfigure feature NOT supported by both ends. 1=PCIe 2.0 Upconfigure feature IS supported by both ends of the Link.

Link Width Control

PCIE_LC_N_FTS_CNTL - RW - 32 bits - RCINDP_Reg:0xA3			
Field Name	**Bits**	**Default**	**Description**
LC_XMIT_N_FTS	7:0	0xc	Number of FTS to override the strap value
LC_XMIT_N_FTS_OVERRIDE_EN	8	0x0	Enable the previous field to override the strap value.
LC_XMIT_FTS_BEFORE_RECOVERY	9	0x1	Transmit FTS before Recovery.
LC_XMIT_N_FTS_LIMIT	23:16	0xff	Limit that the number of FTS can increment to when incrementing is enabled.
LC_N_FTS (R)	31:24	0x0	Number of FTS captured from the other end of the link.

LC Number of FTS Control

PCIE_LC_SPEED_CNTL - RW - 32 bits - RCINDP_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_GEN2_EN_STRAP	0	0x0	PCIE Generation 2 enable bit. Strap Loadable. 0=Gen1 only support. 1=Gen2 supported.
LC_TARGET_LINK_SPEED_OVERRIDE_EN	1	0x0	Enable the overriding of the Target Link Speed configuration register. 0=Disable override. 1=Override Target Link Speed with LC_TARGET_LINK_SPEED_OVERRIDE.

PCIE_LC_SPEED_CNTL - RW - 32 bits - RCINDP_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_TARGET_LINK_SPEED_OVERRIDE	2	0x0	Value used instead of Target Link Speed when override enable is set. 0=Gen2 not supported when override is enabled. 1=Gen2 supported when override is enabled.
LC_FORCE_EN_SW_SPEED_CHANGE	3	0x0	Force the bif_core to allow speed changes initiated by private registers.
LC_FORCE_DIS_SW_SPEED_CHANGE	4	0x0	Disable speed changes initiated by the bif_core private registers.
LC_FORCE_EN_HW_SPEED_CHANGE	5	0x0	Force the bif_core to allow speed changes initiated by the chip interface (based on voltage levels).
LC_FORCE_DIS_HW_SPEED_CHANGE	6	0x1	Disable speed changes initiated by the chip interface (based on voltage levels).
LC_INITIATE_LINK_SPEED_CHANGE	7	0x0	Initiate speed negotiation when allowed by the register settings.
LC_SPEED_CHANGE_ATTEMPTS_ALLOWED	9:8	0x0	Determines the number of speed change attempts that are allowed.
LC_SPEED_CHANGE_ATTEMPT_FAILED (R)	10	0x0	Number of speed change attempts allowed has been reached. This bit and the related counter can be cleared using the LC_CLR_FAILED_SPD_CHANGE_CNT bit.
LC_CURRENT_DATA_RATE (R)	11	0x0	Current data rate of the Link. 0=Gen1 1=Gen2
LC_HW_VOLTAGE_IF_CONTROL	13:12	0x0	Control the chip/bif_core speed control interface. 0=Ignore CHIP/BIF voltage interface. Voltage level is always assumed to be high. 1=CHIP/BIF voltage interface is enabled. 2=CHIP only allowed to lower or raise the voltage when the BIF is running at Gen1 data rate. CHIP must be running at high voltage if BIF is running at Gen2 data rate.
LC_VOLTAGE_TIMER_SEL	17:14	0xa	Controls the circuit that filters noise out of the chip/bif_core voltage interface. 0=No Delay. 1=10ns 2=100ns 3=1us 4=10us 5=100us 6=1ms 7=10ms 8=100ms 9=500ms 10=1sec 11=2sec 12=5sec 13=10sec 14=15sec 15=20sec
LC_GO_TO_RECOVERY	18	0x0	Force the Link to Recovery. Only applicable when link in L0 state.
LC_N_EIE_SEL	19	0x0	Selects the number of EIE (K28.7) symbols that are going to be sent when running at Gen2 speed and the link is exiting L0s. 0=Send 4 EIE (K28.7) symbols before transmitting FTS when exiting L0s at Gen2 speed. 1=Send 8 EIE (K28.7) symbols before transmitting FTS when exiting L0s at Gen2 speed.

PCIE_LC_SPEED_CNTL - RW - 32 bits - RCINDP_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_DONT_CLR_TARGET_SPD_CHANGE_STATUS	20	0x0	Autonomous speed change control after a speed change attempt has failed. 0=Clear speed negotiation failure initiated by Target Link Speed in Detect. 1=Speed negotiation failure initiated by Target Link Speed is only allowed to fail once.
LC_CLR_FAILED_SPD_CHANGE_CNT	21	0x0	This field will clear the LC_SPEED_CHANGE_ATTEMPT_FAILED field when a '1' is written to it. 0=No Change 1=Clear LC_SPEED_CHANGE_ATTEMPT_FAILED register bit so that more SW or HW(Voltage) initiated speed negotiations can be initiated.
LC_1_OR_MORE_TS2_SPEED_ARC_EN	22	0x0	Enable transition from Recovery.RcvrCfg to Recovery.Speed when more than 1 but not all 8 TS2s (with required parameters for a speed change) are received. 0=Don't allow transition from Recovery.RcvrCfg to Recovery.Speed if 1 to 7 TS2s are received. 1=Allow the transition from Recovery.RcvrCfg to Recovery.Speed if 1 to 7 TS2s with speed_change are received.
LC_OTHER_SIDE_EVER_SENT_GEN2 (R)	23	0x0	Cumulative 5.0GT/s capability of the other end of the Link. 0=Other side of link has never advertised that it supports Gen2. 1=Other side of the link has ever advertised that it supports Gen2 - although it may not currently support Gen2.
LC_OTHER_SIDE_SUPPORTS_GEN2 (R)	24	0x0	Current 5.0GT/s capability of the other end of the Link. 0=Other side of the link does not currently advertise that it supports Gen2. 1=Other side of the link currently supports Gen2.
LC_AUTO_RECOVERY_DIS	25	0x1	Autonomous control of the speed advertised after a voltage change. 0=Automatically go to Recovery in order to advertise that a change in Gen2 support has occurred due to a voltage increase. 1=Do not automatically go to Recovery.
LC_SPEED_CHANGE_STATUS	26	0x0	This will gate a HW (i.e. voltage) initiated change to Gen2 when set to 1. 0=No status. 1=Tried to change to Gen2 speed and other end refused. Asserted when the other side no longer supports Gen2.
LC_DATA_RATE_ADVERTISED (R)	27	0x0	Data rate advertised by the port. 0=Only Gen1 support advertised. 1=Gen2 support advertised.
LC_CHECK_DATA_RATE	28	0x1	Determines if the LC is going to check the DATA RATE symbol if the LC_GEN2_EN_STRAP bit is not set. 0=Only check the DATA RATE identifiers when Gen2 is supported. 1=Always check the DATA RATE identifiers regardless of Gen2.

PCIE_LC_SPEED_CNTL - RW - 32 bits - RCINDP_Reg:0xA4			
Field Name	**Bits**	**Default**	**Description**
LC_MULT_UPSTREAM_AUTO_SPD_CHNG_EN	29	0x0	Allows the upstream component to initiate speed changes to the highest link speed supported by both ends of the link. Note that multiple speed changes are only allowed if there aren't any failures in previous speed change attempts. Also, note that the STRAP_BIF_AUTO_RC_SPEED_NEGOTIATION_DIS must be 0. 0=The upstream component will only try to automatically change the link to the highest link speed supported by both ends once - regardless of whether the change is successful or not. 1=The upstream component can automatically initiate multiple speed changes.
LC_INIT_SPEED_NEG_IN_L0s_EN	30	0x0	Speed negotiation during L0s control. 0=Do not allow a speed change to be initialized when in the L0s state. 1=Allow speed change negotiations to be initialized from L0s.
LC_INIT_SPEED_NEG_IN_L1_EN	31	0x0	Speed negotiation during L1 control. 0=Do not allow a speed change to be initialized when in the L1 state. 1=Allow speed change negotiations to be initialized from L1.

Data Rate Control

PCIE_LC_STATE0 - R - 32 bits - RCINDP_Reg:0xA5			
Field Name	**Bits**	**Default**	**Description**
LC_CURRENT_STATE	5:0	0x0	Current LC State
LC_PREV_STATE1	13:8	0x0	1st Previous LC State
LC_PREV_STATE2	21:16	0x0	2nd Previous LC State
LC_PREV_STATE3	29:24	0x0	3rd Previous LC State

Link Control State Register

PCIE_LC_STATE1 - R - 32 bits - RCINDP_Reg:0xA6			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE4	5:0	0x0	4th Previous LC State
LC_PREV_STATE5	13:8	0x0	5th Previous LC State
LC_PREV_STATE6	21:16	0x0	6th Previous LC State
LC_PREV_STATE7	29:24	0x0	7th Previous LC State

Link Control State Register

PCIE_LC_STATE2 - R - 32 bits - RCINDP_Reg:0xA7			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE8	5:0	0x0	8th Previous LC State
LC_PREV_STATE9	13:8	0x0	9th Previous LC State
LC_PREV_STATE10	21:16	0x0	10th Previous LC State
LC_PREV_STATE11	29:24	0x0	11th Previous LC State

Link Control State Register

PCIE_LC_STATE3 - R - 32 bits - RCINDP_Reg:0xA8			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE12	5:0	0x0	12th Previous LC State
LC_PREV_STATE13	13:8	0x0	13th Previous LC State
LC_PREV_STATE14	21:16	0x0	14th Previous LC State
LC_PREV_STATE15	29:24	0x0	15th Previous LC State

Link Control State Register

PCIE_LC_STATE4 - R - 32 bits - RCINDP_Reg:0xA9			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE16	5:0	0x0	16th Previous LC State
LC_PREV_STATE17	13:8	0x0	17th Previous LC State
LC_PREV_STATE18	21:16	0x0	18th Previous LC State
LC_PREV_STATE19	29:24	0x0	19th Previous LC State

Link Control State Register

PCIE_LC_STATE5 - R - 32 bits - RCINDP_Reg:0xAA			
Field Name	**Bits**	**Default**	**Description**
LC_PREV_STATE20	5:0	0x0	20th Previous LC State
LC_PREV_STATE21	13:8	0x0	21st Previous LC State
LC_PREV_STATE22	21:16	0x0	22nd Previous LC State
LC_PREV_STATE23	29:24	0x0	23rd Previous LC State

Link Control State Register

PCIE_LC_CNTL2 - RW - 32 bits - RCINDP_Reg:0xB1			
Field Name	**Bits**	**Default**	**Description**
LC_TIMED_OUT_STATE (R)	5:0	0x0	State that the LC was in when the deadman timer expired.
LC_STATE_TIMED_OUT	6	0x0	Deadman timer expired.
LC_LOOK_FOR_BW_REDUCTION	7	0x1	Enable check for bandwidth change when reporting Link Bandwidth Notification Status. 0=Do not check if bandwidth was reduced. 1=Check if bandwidth was reduced.
LC_MORE_TS2_EN	8	0x0	Send out 128 sets instead of 16.
LC_X12_NEGOTIATION_DIS	9	0x1	Disable x12 negotiation.
LC_LINK_UP_REVERSAL_EN	10	0x0	Allow reversal for a wider width in link up.
LC_ILLEGAL_STATE	11	0x0	The LC is in an illegal state.
LC_ILLEGAL_STATE_RESTART_EN	12	0x0	Enable the LC to be restarted when it is in an illegal state.
LC_WAIT_FOR_OTHER_LANES_MODE	13	0x0	Eliminate delay introduced by waiting for other lanes. 0=Identical Training Set based (wait time limited by counter) 1=Timer based
LC_ELEC_IDLE_MODE	15:14	0x0	Electrical Idle Mode for LC. 0=GEN1 - entry:PHY, exit:PHY ; GEN2 - entry:infer, exit:PHY 1=GEN1 - entry:infer, exit:PHY; GEN2 - entry:infer, exit PHY 2=GEN1 - entry:PHY, exit:PHY ; GEN2 - entry:PHY, exit:PHY 3=Reserved
LC_DISABLE_INFERRED_ELEC_IDLE_DET	16	0x0	Disable Inferred Electrical Idle detection. 0=Inferred Electrical Idle Detection is enabled 1=Inferred Electrical Idle Detection is disabled

PCIE_LC_CNTL2 - RW - 32 bits - RCINDP_Reg:0xB1			
Field Name	**Bits**	**Default**	**Description**
LC_ALLOW_PDWN_IN_L1	17	0x0	Set the BIF_CHIP_CLK_PDWN output to 1 when the LC is in the L1 state.
LC_ALLOW_PDWN_IN_L23	18	0x0	Set the BIF_CHIP_CLK_PDWN output to 1 when the LC is in the L23_Ready state.
LC_DEASSERT_RX_EN_IN_L0S	19	0x0	Turn off transmitters when the link is in L0s.
LC_BLOCK_EL_IDLE_IN_L0	20	0x0	Prevent the Electrical Idle from causing a transition from Rcv_L0 to Rcv_L0s.
LC_RCV_L0_TO_RCV_L0S_DIS	21	0x0	Disable transition from Rcv_L0 to Rcv_L0s
LC_ASSERT_INACTIVE_DURING_HOLD	22	0x0	Assert the INACTIVE_LANES signals when CHIP_BIF_hold_training is high.
LC_WAIT_FOR_LANES_IN_LW_NEG	24:23	0x0	Mode used to wait for TS on all lanes in link width negotiation.
LC_PWR_DOWN_NEG_OFF_LANES	25	0x1	Power down unused lanes.
LC_DISABLE_LOST_SYM_LOCK_ARCS	26	0x1	Control transition to Recovery.RcvrLock from Configuration.Idle or Recovery.Idle when a training set is received. Similar to 'idle_to_rlock_transitioned' variable.
LC_LINK_BW_NOTIFICATION_DIS	27	0x0	Control for the Link Bandwidth Notification Feature.
LC_ENABLE_RX_CR_EN_DEASSERTION	28	0x0	To enable deassertion of PG2RX_CR_EN to lock clock recovery parameter when lane is in electrical idle 0=CR_EN is always asserted 1=CR_EN is deasserted when RX_EN is deasserted during L0s/L1 and inactive lanes
LC_TEST_TIMER_SEL	30:29	0x0	State timeout select 0=LTSSM uses spec compliant timeout values. 1=LTSSM uses simulation timeout values. 2=LTSSM uses decreased timeout values for lab testing. 3=Reserved
LC_ENABLE_INFERRED_ELEC_IDLE_FOR_PI	31	0x1	Enable Inferred Electrical Idle Detection for PI (Physical Layer blocks) 0=Inferred Electrical Idle Detection is disabled for PI (Physical Layer block) 1=Inferred Electrical Idle Detection is enabled for PI (Physical Layer block)

Link Control Register 2

PCIE_LC_BW_CHANGE_CNTL - RW - 32 bits - RCINDP_Reg:0xB2			
Field Name	**Bits**	**Default**	**Description**
LC_BW_CHANGE_INT_EN	0	0x0	Enable Interrupt when the link bandwidth changes.
LC_HW_INIT_SPEED_CHANGE	1	0x0	Link speed changed due to a hardware-initiated speed negotiation.
LC_SW_INIT_SPEED_CHANGE	2	0x0	Link speed changed due to a software-initiated speed negotiation.
LC_OTHER_INIT_SPEED_CHANGE	3	0x0	Link speed changed due to a speed negotiation initiated by the other end of the link.
LC_RELIABILITY_SPEED_CHANGE	4	0x0	Link speed changed due to a reliability issue at the current speed.
LC_FAILED_SPEED_NEG	5	0x0	Link speed change failed and link speed was reverted to initial speed.
LC_LONG_LW_CHANGE	6	0x0	Link width was changed due to a long dynamic link width reconfiguration.

PCIE_LC_BW_CHANGE_CNTL - RW - 32 bits - RCINDP_Reg:0xB2			
Field Name	**Bits**	**Default**	**Description**
LC_SHORT_LW_CHANGE	7	0x0	Link width was changed due to a short dynamic link width reconfiguration.
LC_LW_CHANGE_OTHER	8	0x0	Link width changed and the change was initiated by the other end of the link.
LC_LW_CHANGE_FAILED	9	0x0	Link width change was initiated by the width was not changed.
LC_LINK_BW_NOTIFICATION_DETECT_MODE	10	0x0	Control Link Bandwidth Management for speed changes in Detect. 0=Disable Link Bandwidth Management Capabilities in Detect. 1=Update LINK_BW_MANAGEMENT_STATUS when speed changes in Detect.

LC Bandwidth Change Notification Control Register

PCIE_LC_CDR_CNTL - RW - 32 bits - RCINDP_Reg:0xB3			
Field Name	**Bits**	**Default**	**Description**
LC_CDR_TEST_OFF	11:0	0x60	Enable CDR Test Mode.
LC_CDR_TEST_SETS	23:12	0x18	Select the number of sets that are transmitted during CDR test mode.
LC_CDR_SET_TYPE	25:24	0x1	Select for the type of set that is transmitted during CDR test mode.

CDR Control Register

PCIE_LC_LANE_CNTL - RW - 32 bits - RCINDP_Reg:0xB4			
Field Name	**Bits**	**Default**	**Description**
LC_CORRUPTED_LANES (R)	15:0	0x0	Each bit indicates if that associated lane had trouble during training.
LC_LANE_DIS	31:16	0x0	Permanently disable associated lane.

Lane Status and Control Register

PCIE_LC_CNTL3 - RW - 32 bits - RCINDP_Reg:0xB5			
Field Name	**Bits**	**Default**	**Description**
LC_SELECT_DEEMPHASIS	0	0x0	Downstream De-Emphasis 0=-6dB De-emphasis required. 1=-3.5dB De-emphasis required.
LC_SELECT_DEEMPHASIS_CNTL	2:1	0x0	Upstream De-Emphasis control 0=Use De-emphasis from CSR. 1=Use De-emphasis from downstream component. 2=Use -6dB De-emphasis. 3=Use -3.5dB De-emphasis.
LC_RCVD_DEEMPHASIS (R)	3	0x0	De-emphasis setting advertised by other end.
LC_COMP_TO_DETECT	4	0x0	Modified Compliance Pattern control 0=No action taken. 1=Transition LTSSM from Polling.Compliance to Detect if sending out Modified Compliance Pattern due to receipt of TS1s.
LC_RESET_TSX_CNT_IN_RLOCK_EN	5	0x1	TS Ordered Set Counter Control in Recovery.RcvrLock 0=No change in Training Sequence counter when DIRECTED_SPEED_CHANGE asserted in Recovery.RcvrLock. 1=Reset Training Sequence counter when DIRECTED_SPEED_CHANGE is asserted in Recovery.RcvrLock.

PCIE_LC_CNTL3 - RW - 32 bits - RCINDP_Reg:0xB5			
Field Name	**Bits**	**Default**	**Description**
LC_AUTO_SPEED_CHANGE_ATTEMPTS_ALLOWED	7:6	0x0	Number of unsuccessful Autonomous Speed Changes that are allowed. N/A for downstream components. 0=1 1=2 2=3 3=4
LC_AUTO_SPEED_CHANGE_ATTEMPT_FAILED (R)	8	0x0	Number of maximum unsuccessful Autonomous Speed Change attempts reached. N/A for downstream components. 0=Autonomous changes by RC allowed. 1=Maximum allowable number of autonomous speed changes reached.
LC_CLR_FAILED_AUTO_SPD_CHANGE_CNT	9	0x0	Clear Autonomous Speed Change counter. N/A for downstream components. 0=No action taken. 1=Clear LC_AUTO_SPEED_CHANGE_ATTEMPT_FAILED register bit so that the RC can autonomously initiate more speed negotiations.

Link Control Register 3

PCIEP_STRAP_LC - RW - 32 bits - RCINDP_Reg:0xC0			
Field Name	**Bits**	**Default**	**Description**
STRAP_FTS_yTSx_COUNT	1:0	0x0	Provides an override for STRAP_FTS_yTSx_COUNT
STRAP_LONG_yTSx_COUNT	3:2	0x0	Provides an override for STRAP_LONG_yTSx_COUNT
STRAP_MED_yTSx_COUNT	5:4	0x0	Provides an override for STRAP_MED_yTSx_COUNT
STRAP_SHORT_yTSx_COUNT	7:6	0x0	Provides an override for STRAP_SHORT_yTSx_COUNT
STRAP_SKIP_INTERVAL	10:8	0x0	Provides an override for STRAP_SKIP_INTERVAL
STRAP_BYPASS_RCVR_DET	11	0x0	Provides an override for STRAP_BYPASS_RCVR_DET
STRAP_COMPLIANCE_DIS	12	0x0	Provides an override for STRAP_COMPLIANCE_DIS
STRAP_FORCE_COMPLIANCE	13	0x0	Provides an override for STRAP_FORCE_COMPLIANCE
STRAP_REVERSE_LC_LANES	14	0x0	Provides an override for STRAP_REVERSE_LC_LANES
STRAP_AUTO_RC_SPEED_NEGOTIATION_DIS	15	0x0	Provides an override for STRAP_AUTO_RC_SPEED_NEGOTIATION_DIS
STRAP_LANE_NEGOTIATION	18:16	0x0	Provides an override for STRAP_LANE_NEGOTIATION 0=Compliant mode, widest possible link 1=Compliant mode, fix missing lane 0 2=Compliant mode, reverse only 3=Compliant mode, reverse only, don't require the sets to be contiguous 4=Old mode, reverse only 5=Easy training mode, reverse only 6=Reliable mode, reverse only - means to reliably train, in a reliable system 7=Reserved

Misc LC strap loadable register value

PCIEP_STRAP_MISC - RW - 32 bits - RCINDP_Reg:0xC1			
Field Name	**Bits**	**Default**	**Description**
STRAP_EXIT_LATENCY	3:0	0x0	Provides an override for STRAP_EXIT_LATENCY
STRAP_REVERSE_LANES	4	0x0	Provides an override for STRAP_REVERSE_LANES

Misc port strap loadable register values

4.3 PCIe® Bridge Register Descriptions (Device 21, Function 0/1/2/3)

4.3.1 PCIe® Bridges

Hudson-1 provides 4 lanes for PCIe® Gen-2 connection, supporting up to 4 general purpose devices.

Supported configurations include:

- 1 port : 4 lanes
- 2 ports: 2 lanes each
- 3 ports: port-1 with 2 lanes and port-2 and port-3 with 1 lane each
- 4 ports: 1 lane each

Each port is controlled by one PCIe bridge. The number of PCIe bridges goes from 1 to 4, depending on the system configuration. System software needs to program the proper port configuration through ABCFG_Reg xC0 before enabling any of the PCIe ports.

Register Name	Address Offset
VENDOR_ID	00h
DEVICE_ID	02h
COMMAND	04h
STATUS	06h
REVISION_ID	08h
PROG_INTERFACE	09h
SUB_CLASS	0Ah
BASE_CLASS	0Bh
CACHE_LINE	0Ch
LATENCY	0Dh
HEADER	0Eh
BIST	0Fh
SUB_BUS_NUMBER_LATENCY	18h
IO_BASE_LIMIT	1Ch
SECONDARY_STATUS	1Eh
MEM_BASE_LIMIT	20h
PREF_BASE_LIMIT	24h
PREF_BASE_UPPER	28h
PREF_LIMIT_UPPER	2Ch
IO_BASE_LIMIT_HI	30h
IRQ_BRIDGE_CNTL	3Eh
CAP_PTR	34h
INTERRUPT_LINE	3Ch
INTERRUPT_PIN	3Dh
EXT_BRIDGE_CNTL	40h
PMI_CAP_LIST	50h
PMI_CAP	52h
PMI_STATUS_CNTL	54h
PCIE_CAP_LIST	58h

Register Name	Address Offset
PCIE_CAP	5Ah
DEVICE_CAP	5Ch
DEVICE_CNTL	60h
DEVICE_STATUS	62h
LINK_CAP	64h
LINK_CNTL	68h
LINK_STATUS	6Ah
SLOT_CAP	6Ch
SLOT_CNTL	70h
SLOT_STATUS	72h
ROOT_CNTL	74h
ROOT_CAP	76h
ROOT_STATUS	78h
DEVICE_CAP2	7Ch
DEVICE_CNTL2	80h
DEVICE_STATUS2	82h
LINK_CAP2	84h
LINK_CNTL2	88h
LINK_STATUS2	8Ah
SLOT_CAP2	8Ch
SLOT_CNTL2	90h
SLOT_STATUS2	92h
MSI_CAP_LIST	A0h
MSI_MSG_CNTL	A2h
MSI_MSG_ADDR_LO	A4h
MSI_MSG_ADDR_HI	A8h
MSI_MSG_DATA_64	ACh
MSI_MSG_DATA	A8h
SSID_CAP_LIST	B0h
SSID_ID	B4h
MSI_MAP_CAP_LIST	B8h
PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST	100h
PCIE_VENDOR_SPECIFIC_HDR	104h
PCIE_VENDOR_SPECIFIC1	108h
PCIE_VENDOR_SPECIFIC2	10Ch
PCIE_VC_ENH_CAP_LIST	110h
PCIE_PORT_VC_CAP_REG1	114h
PCIE_PORT_VC_CAP_REG2	118h
PCIE_PORT_VC_CNTL	11Ch
PCIE_PORT_VC_STATUS	11Eh
PCIE_VC0_RESOURCE_CAP	120h
PCIE_VC0_RESOURCE_CNTL	124h
PCIE_VC0_RESOURCE_STATUS	12Ah
PCIE_VC1_RESOURCE_CAP	12Ch
PCIE_VC1_RESOURCE_CNTL	130h
PCIE_VC1_RESOURCE_STATUS	136h
PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST	140h
PCIE_DEV_SERIAL_NUM_DW1	144h
PCIE_DEV_SERIAL_NUM_DW2	148h
PCIE_ADV_ERR_RPT_ENH_CAP_LIST	150h
PCIE_UNCORR_ERR_STATUS	154h
PCIE_UNCORR_ERR_MASK	158h
PCIE_UNCORR_ERR_SEVERITY	15Ch
PCIE_CORR_ERR_STATUS	160h
PCIE_CORR_ERR_MASK	164h
PCIE_ADV_ERR_CAP_CNTL	168h
PCIE_HDR_LOG0	16Ch
PCIE_HDR_LOG1	170h

Register Name	Address Offset
PCIE_HDR_LOG2	174h
PCIE_HDR_LOG3	178h
PCIE_ROOT_ERR_CMD	17Ch
PCIE_ROOT_ERR_STATUS	180h
PCIE_ERR_SRC_ID	184h
PCIE_ACS_ENH_CAP_LIST	190h
PCIE_ACS_CAP	194h
PCIE_ACS_CNTL	196h

VENDOR_ID - RW - 16 bits - pcieCfg0:0x0			
Field Name	**Bits**	**Default**	**Description**
VENDOR_ID (R)	15:0	1002	This field identifies the manufacturer of the device. 0FFFFh is an invalid value for Vendor ID.

Vendor Identification

DEVICE_ID - R - 16 bits - pcieCfg0:0x2			
Field Name	**Bits**	**Default**	**Description**
DEVICE_ID	15:0	43A0/ 43A1/ 43A2/ 43A3	This field identifies the particular device. This identifier is allocated by the vendor. fun-0: 43A0 fun-1: 43A1 fun-2: 43A2 fun-3: 43A3

Device Identification

COMMAND - RW - 16 bits - pcieCfg0:0x4			
Field Name	**Bits**	**Default**	**Description**
IO_ACCESS_EN	0	0x0	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses.State after RST# is 0. 0=Disable 1=Enable
MEM_ACCESS_EN	1	0x0	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0. 0=Disable 1=Enable
BUS_MASTER_EN	2	0x0	Controls the ability of a PCI Express® endpoint to issue Memory and I/O Read/Write Requests, and the ability of a Root or Switch Port to forward Memory and I/O Read/Write Requests in the upstream direction. 0=Disable 1=Enable
SPECIAL_CYCLE_EN (R)	3	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
MEM_WRITE_INVALIDATE_EN (R)	4	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
PAL_SNOOP_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable

COMMAND - RW - 16 bits - pcieCfg0:0x4			
Field Name	**Bits**	**Default**	**Description**
PARITY_ERROR_RESPONSE	6	0x0	Parity Error Response. Default value of this field is 0. 0=Disable 1=Enable
AD_STEPPING (R)	7	0x0	Address and Data Stepping. Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
SERR_EN	8	0x0	When set, enables reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. 0=Disable 1=Enable
FAST_B2B_EN (R)	9	0x0	Does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable
INT_DIS	10	0x0	Controls the ability of a PCI Express® device to generate INTx interrupt Messages. When set, devices are prevented from generating INTx interrupt Messages. Default value 0 0=Enable 1=Disable\

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles.

STATUS - RW - 16 bits - pcieCfg0:0x6			
Field Name	**Bits**	**Default**	**Description**
INT_STATUS (R)	3	0x0	Indicates that an INTx interrupt Message is pending internally to the device.
CAP_LIST (R)	4	0x1	Indicates the presence of an extended capability list item. Since all PCI Express® devices are required to implement the PCI Express capability structure, this bit must be set to 1.
PCI_66_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
UDF_EN (R)	6	0x0	User Defined Status Enable 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Does not apply to PCI Express. Hardwired to 0.
MASTER_DATA_PARITY_ERROR	8	0x0	This bit is set by Requestor if its Parity Error Enable bit is set and either of the following two conditions occurs: 1) Requestor receives a Completion marked poisoned 2) Requestor poisons a write Request 0=Inactive 1=Active
DEVSEL_TIMING (R)	10:9	0x0	Does not apply to PCI Express. Hardwired to 0.
SIGNAL_TARGET_ABORT	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status. 0=No Abort 1=Target Abort
RECEIVED_TARGET_ABORT	12	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
RECEIVED_MASTER_ABORT	13	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=Inactive 1=Active
SIGNALED_SYSTEM_ERROR	14	0x0	This bit must be set whenever the device asserts SERR#. 0=No Error 1=SERR assert

STATUS - RW - 16 bits - pcieCfg0:0x6			
Field Name	**Bits**	**Default**	**Description**
PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1.

The Status register is used to record status information for PCI bus related events.

REVISION_ID - R - 8 bits - pcieCfg0:0x8			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Major revision ID. Set by the vendor.
MAJOR_REV_ID	7:4	0x0	Minor revision ID. Set by the vendor.

Specifies a device specific revision identifier. The value is chosen by the vendor.

PROG_INTERFACE - R - 8 bits - pcieCfg0:0x9			
Field Name	**Bits**	**Default**	**Description**
PROG_INTERFACE	7:0	0x0	Unused, only in test environment

Register-Level Programming Interface Register

SUB_CLASS - R - 8 bits - pcieCfg0:0xA			
Field Name	**Bits**	**Default**	**Description**
SUB_CLASS	7:0	0x4	The Class Code register is read-only and is used with the Base Class Code to identify the specific type of device.

Sub Class Code Register

BASE_CLASS - R - 8 bits - pcieCfg0:0xB			
Field Name	**Bits**	**Default**	**Description**
BASE_CLASS	7:0	0x6	The Class Code register is read-only and is used to identify the generic function of the device.

Base Class Code Register

CACHE_LINE - RW - 8 bits - pcieCfg0:0xC			
Field Name	**Bits**	**Default**	**Description**
CACHE_LINE_SIZE	7:0	0x0	This read/write register specifies the system cacheline size in units of DWORDs.

Cache Line Size Register

LATENCY - RW - 8 bits - pcieCfg0:0xD			
Field Name	**Bits**	**Default**	**Description**
LATENCY_TIMER (R)	7:0	0x0	Primary/Master latency timer does not apply to PCI Express®. Register is hardwired to 0.

Master Latency Timer Register

HEADER - RW - 8 bits - pcieCfg0:0xE			
Field Name	**Bits**	**Default**	**Description**
HEADER_TYPE (R)	6:0	0x1	Type 0 or Type 1 Configuration Space
DEVICE_TYPE (R)	7	0x1	Single function or multi function device 0=Single-Function Device 1=Multi-Function Device

Configuration Space Header

BIST - RW - 8 bits - pcieCfg0:0xF			
Field Name	**Bits**	**Default**	**Description**
BIST_COMP (R)	3:0	0x0	A value of 0 means the device has passed its test. Non-zero values mean the device failed. Device-specific failure codes can be encoded in the non-zero value.
BIST_STRT (R)	6	0x0	Write a 1 to invoke BIST. Device resets the bit when BIST is complete. Software should fail the device if BIST is not complete after 2 seconds.
BIST_CAP (R)	7	0x0	This bit is read-only and returns 1 the bridge supports BIST, otherwise 0 is returned

Built In Self Test Register used for control and status of built-in self tests

SUB_BUS_NUMBER_LATENCY - RW - 32 bits - pcieCfg0:0x18			
Field Name	**Bits**	**Default**	**Description**
PRIMARY_BUS	7:0	0x0	Primary Bus Number register records the bus number of the PCI bus segment to which the primary interface of the bridge is connected.
SECONDARY_BUS	15:8	0x0	Secondary Bus Number register is used to record the bus number of the PCIE bus segment to which the secondary interface of the bridge is connected.
SUB_BUS_NUM	23:16	0x0	Subordinate Bus Number Register is used to record the bus number of the highest numbered PCI bus segment which is behind the bridge.
SECONDARY_LATENCY_TIMER (R)	31:24	0x0	Register does not apply to PCI Express®. Hardwired to 0.

Subordinate Bus Number Latency

IO_BASE_LIMIT - RW - 16 bits - pcieCfg0:0x1C			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_TYPE (R)	3:0	0x1	I/O Base Addressing Type 0=16-bit 1=32-bit
IO_BASE	7:4	0x0	I/O Base Register
IO_LIMIT_TYPE (R)	11:8	0x1	I/O Limit Addressing Type 0=16-bit 1=32-bit
IO_LIMIT	15:12	0x0	I/O Limit Register

I/O Base Register Limit is used by the bridge to determine when to forward I/O transactions from one interface to the other.

SECONDARY_STATUS - RW - 16 bits - pcieCfg0:0x1E			
Field Name	**Bits**	**Default**	**Description**
CAP_LIST (R)	4	0x0	Indicates the presence of an extended capability list item. Since all PCI Express® devices are required to implement the PCI Express capability structure, this bit must be set to 1.
PCI_66_EN (R)	5	0x0	Does not apply to PCI Express. Hardwired to 0.
UDF_EN (R)	6	0x0	User Defined Status Enable 0=Disable 1=Enable
FAST_BACK_CAPABLE (R)	7	0x0	Does not apply to PCI Express. Hardwired to 0.

SECONDARY_STATUS - RW - 16 bits - pcieCfg0:0x1E			
Field Name	**Bits**	**Default**	**Description**
MASTER_DATA_PARITY_ERROR	8	0x0	This bit is set by Requestor if its Parity Error Enable bit is set and either of the following two conditions occurs: 1) Requestor receives a Completion marked poisoned 2) Requestor poisons a write Request 0=No error 1=Parity error
DEVSEL_TIMING (R)	10:9	0x0	Does not apply to PCI Express®. Hardwired to 0.
SIGNAL_TARGET_ABORT	11	0x0	This bit is set when a device completes a Request using Completer Abort Completion Status. 0=No Abort 1=Target Abort asserted
RECEIVED_TARGET_ABORT	12	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=No CA Received 1=Received Completion Abort
RECEIVED_MASTER_ABORT	13	0x0	This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status. 0=No UR Received 1=Received Unsupported Request
RECEIVED_SYSTEM_ERROR	14	0x0	This bit reports the detection of an system error on the secondary interface of the bridge. 1 is asserted if a system error has been detected. 0=No Error 1=Sent Error Message
PARITY_ERROR_DETECTED	15	0x0	This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. 0=No Error 1=Received Poisoned TLP

Secondary Status Register. Its bits reflect status conditions of the secondary interface

MEM_BASE_LIMIT - RW - 32 bits - pcieCfg0:0x20			
Field Name	**Bits**	**Default**	**Description**
MEM_BASE_TYPE (R)	3:0	0x0	Memory Base Addressing Type 0=32-bit 1=64-bit
MEM_BASE_31_20	15:4	0x0	Memory Base Register
MEM_LIMIT_TYPE (R)	19:16	0x0	Memory Limit Addressing Type 0=32-bit 1=64-bit
MEM_LIMIT_31_20	31:20	0x0	Memory Limit Register

Memory Limit Register defines a memory mapped I/O address range which is used by the bridge to determine when to forward memory transactions from one interface to the other

PREF_BASE_LIMIT - RW - 32 bits - pcieCfg0:0x24			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_BASE_TYPE (R)	3:0	0x1	Prefetchable Memory Base Addressing Type 0=32-bit 1=64-bit
PREF_MEM_BASE_31_20	15:4	0x0	Prefetchable Memory Base Register
PREF_MEM_LIMIT_TYPE (R)	19:16	0x1	Prefetchable Memory Limit Addressing Type 0=32-bit 1=64-bit

PREF_BASE_LIMIT - RW - 32 bits - pcieCfg0:0x24			
Field Name	**Bits**	**Default**	**Description**
PREF_MEM_LIMIT_31_20	31:20	0x0	Prefetchable Memory Limit Register

Prefetchable Memory Base Limit indicates 64-bit addresses are supported.

PREF_BASE_UPPER - RW - 32 bits - pcieCfg0:0x28			
Field Name	**Bits**	**Default**	**Description**
PREF_BASE_UPPER	31:0	0x0	Upper 32 bits for 64-bit address.

Prefetchable Memory Base Upper 32 bits.

PREF_LIMIT_UPPER - RW - 32 bits - pcieCfg0:0x2C			
Field Name	**Bits**	**Default**	**Description**
PREF_LIMIT_UPPER	31:0	0x0	Upper 32 bits for 64-bit address.

Prefetchable Memory Limit Upper 32 bits.

IO_BASE_LIMIT_HI - RW - 32 bits - pcieCfg0:0x30			
Field Name	**Bits**	**Default**	**Description**
IO_BASE_31_16	15:0	0x0	Upper 16 bits for 32-bit address.
IO_LIMIT_31_16	31:16	0x0	Upper 16 bits for 32-bit address.

I/O Base and I/O Limit Upper 16 bits.

IRQ_BRIDGE_CNTL - RW - 16 bits - pcieCfg0:0x3E			
Field Name	**Bits**	**Default**	**Description**
PARITY_RESPONSE_EN	0	0x0	Parity Error Response Enable controls the response to Poisoned TLPs.
SERR_EN	1	0x0	System Error Enable controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary
ISA_EN	2	0x0	ISA Enable modifies the response by the bridge to ISA I/O addresses.
VGA_EN	3	0x0	VGA Enable modifies the response by the bridge to VGA compatible addresses.
VGA_DEC	4	0x0	Enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 kB.
MASTER_ABORT_MODE (R)	5	0x0	Master Abort Mode does not apply to PCI Express®. Hardwired to 0.
SECONDARY_BUS_RESET	6	0x0	Secondary Bus Reset triggers a hot reset on the corresponding PCI Express Port. 0=Run 1=Reset
FAST_B2B_EN (R)	7	0x0	Fast Back-to-Back Transactions Enable does not apply to PCI Express. Hardwired to 0. 0=Disable 1=Enable

Bridge Control Register

CAP_PTR - RW - 32 bits - pcieCfg0:0x34			
Field Name	**Bits**	**Default**	**Description**
CAP_PTR (R)	7:0	0x50	Pointer to a linked list of additional capabilities implemented by this device. 50=Point to PM Capability

Capability Pointer

INTERRUPT_LINE - RW - 8 bits - pcieCfg0:0x3C			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_LINE	7:0	0xff	Interrupt Line register communicates interrupt line routing information.

Interrupt Line Register

INTERRUPT_PIN - RW - 8 bits - pcieCfg0:0x3D			
Field Name	**Bits**	**Default**	**Description**
INTERRUPT_PIN	7:0	0x0	The Interrupt Pin is a read-only register that identifies the legacy interrupt Message(s) the device (or device function) uses NOTE: Bits 3:7 of this field are hardwired to ZERO.

Interrupt Pin Register

EXT_BRIDGE_CNTL - RW - 8 bits - pcieCfg0:0x40			
Field Name	**Bits**	**Default**	**Description**
IO_PORT_80_EN	0	0x0	Register to enable IO port 80 decoding.

External Bridge Control Register

PMI_CAP_LIST - R - 16 bits - pcieCfg0:0x50			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x1	Capability ID Must be set to 01h 1=PCIE Power Management Registers
NEXT_PTR	15:8	0x58	Next Capability Pointer

Power Management Capability List

PMI_CAP - RW - 16 bits - pcieCfg0:0x52			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	2:0	0x3	Version 3=PMI Spec 1.2
PME_CLOCK (R)	3	0x0	Does not apply to PCI Express®. Hardwired to 0.
DEV_SPECIFIC_INIT (R)	5	0x0	Device Specific Initialization
AUX_CURRENT	8:6	0x0	AUX Current
D1_SUPPORT (R)	9	0x0	D1 Support 1=Support D1 PM State.
D2_SUPPORT (R)	10	0x0	D2 Support 1=Support D2 PM State.
PME_SUPPORT (R)	15:11	0x0	For a device, this indicates the power states in which the device may generate a PME.

Power Management Capabilities Register

PMI_STATUS_CNTL - RW - 32 bits - pcieCfg0:0x54			
Field Name	**Bits**	**Default**	**Description**
POWER_STATE	1:0	0x0	Power State
NO_SOFT_RESET (R)	3	0x0	No Soft Reset
PME_EN	8	0x0	PME Enable
DATA_SELECT (R)	12:9	0x0	Data Select
DATA_SCALE (R)	14:13	0x0	Data Scale
PME_STATUS	15	0x0	PME Status
B2_B3_SUPPORT (R)	22	0x0	B2/B3 Support Does not apply to PCI Express®. Hardwired to 0.
BUS_PWR_EN (R)	23	0x0	Bus Power/Clock Control Enable Does not apply to PCI Express. Hardwired to 0.
PMI_DATA (R)	31:24	0x0	Data

Power Management Status/Control Register

PCIE_CAP_LIST - R - 16 bits - pcieCfg0:0x58			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x10	Indicates the PCI Express® Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure. 10=PCI Express capable
NEXT_PTR	15:8	0xa0	Next Capability Pointer -- The offset to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities.

The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 2.3 configuration space capability list.

PCIE_CAP - RW - 16 bits - pcieCfg0:0x5A			
Field Name	**Bits**	**Default**	**Description**
VERSION (R)	3:0	0x2	Indicates PCI-SIG defined PCI Express® capability structure version number. 0=PCI Express Cap Version
DEVICE_TYPE (R)	7:4	0x4	Indicates the type of PCI Express logical device. 0=PCI Express Endpoint 1=Legacy PCI Express Endpoint 4=PCI Express Root Complex
SLOT_IMPLEMENTED	8	0x0	This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot
INT_MESSAGE_NUM (R)	13:9	0x0	Interrupt Message Number.

The PCI Express Capabilities register identifies PCI Express device type and associated capabilities.

DEVICE_CAP - RW - 32 bits - pcieCfg0:0x5C			
Field Name	**Bits**	**Default**	**Description**
MAX_PAYLOAD_SUPPORT (R)	2:0	0x0	This field indicates the maximum payload size that the device can support for TLPs. 0=128B size
PHANTOM_FUNC (R)	4:3	0x0	This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers with the Tag identifier. 0=No Phantom Functions
EXTENDED_TAG (R)	5	0x1	This field indicates the maximum supported size of the Tag field as a Requester. 0=5 Bit Tag Supported 1=8 Bit Tag Supported

DEVICE_CAP - RW - 32 bits - pcieCfg0:0x5C			
Field Name	**Bits**	**Default**	**Description**
L0S_ACCEPTABLE_LATENCY (R)	8:6	0x0	This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state.
L1_ACCEPTABLE_LATENCY (R)	11:9	0x0	This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state.
ROLE_BASED_ERR_REPORTING (R)	15	0x0	This field indicates the function implements the functionality originally defined in the Error Reporting ECN for PCI Express® Base Specification 1.0a. 0=Role-Based Error Reporting Disabled 1=Role-Based Error Reporting Enabled
CAPTURED_SLOT_POWER_LIMIT (R)	25:18	0x0	(Upstream Ports only) In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot.
CAPTURED_SLOT_POWER_SCALE (R)	27:26	0x0	Specifies the scale used for the Slot Power Limit Value.
FLR_CAPABLE (R)	28	0x0	This field indicates that a device is capable of initiating Function Level Resets.

The Device Capabilities register identifies PCI Express device specific capabilities.

DEVICE_CNTL - RW - 16 bits - pcieCfg0:0x60			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_EN	0	0x0	This bit controls reporting of correctable errors. Default value of this field is 0. 0=Disable 1=Enable
NON_FATAL_ERR_EN	1	0x0	This bit controls reporting of Non-fatal errors. Default value of this field is 0. 0=Disable 1=Enable
FATAL_ERR_EN	2	0x0	This bit controls reporting of Fatal errors. Default value of this field is 0. 0=Disable 1=Enable
USR_REPORT_EN	3	0x0	This bit enables reporting of Unsupported Requests when set. Default value of this field is 0. 0=Disable 1=Enable
RELAXED_ORD_EN	4	0x1	If this bit is set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. Default value of this bit is 1. 0=Disable 1=Enable
MAX_PAYLOAD_SIZE (R)	7:5	0x0	This field sets maximum TLP payload size for the device. Default value of this field is 000b. 0=128B size
EXTENDED_TAG_EN	8	0x0	When set, this bit enables a device to use an 8-bit Tag field as a requester. If the bit is cleared, the device is restricted to a 5-bit Tag field. Default value of this field is 0. 0=Disable 1=Enable

DEVICE_CNTL - RW - 16 bits - pcieCfg0:0x60			
Field Name	**Bits**	**Default**	**Description**
PHANTOM_FUNC_EN (R)	9	0x0	When set, this bit enables a device to use unclaimed functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is cleared, the device is not allowed to use Phantom Functions. 0=Disable 1=Enable
AUX_POWER_PM_EN (R)	10	0x0	This bit when set enables a device to draw AUX power independent of PME AUX power. 0=Disable 1=Enable
NO_SNOOP_EN	11	0x1	If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Default value of this bit is 1. 0=Disable 1=Enable
MAX_REQUEST_SIZE (R)	14:12	0x0	This field sets the maximum Read Request size for the Device as a Requester. Default value of this field is 010b. 0=128B size
BRIDGE_CFG_RETRY_EN (R)	15	0x0	This field enables PCI Express® to PCI/PCI-X bridges to return Configuration Request Retry Status (CRS) in response to configuration requests that target devices below the bridge. 0=Disable 1=Enable

The Device Control register controls PCI Express device specific parameters.

DEVICE_STATUS - RW - 16 bits - pcieCfg0:0x62			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR	0	0x0	This bit indicates status of correctable errors detected.
NON_FATAL_ERR	1	0x0	This bit indicates status of Nonfatal errors detected.
FATAL_ERR	2	0x0	This bit indicates status of Fatal errors detected.
USR_DETECTED	3	0x0	This bit indicates that the device received an Unsupported Request.
AUX_PWR	4	0x0	Devices that require AUX power report this bit as set if AUX power is detected by the device.
TRANSACTIONS_PEND (R)	5	0x0	Endpoints: This bit when set indicates that the device has issued Non-Posted Requests which have not been completed. Root and Switch Ports: This bit when set indicates that a Port has issued Non-Posted Requests on its own behalf (using the Port's own Requester ID) which have not been completed.

The Device Status register provides information about PCI Express device specific parameters.

LINK_CAP - RW - 32 bits - pcieCfg0:0x64			
Field Name	**Bits**	**Default**	**Description**
LINK_SPEED (R)	3:0	0x1	This field indicates the maximum Link speed of the given PCI Express® link. 1=2.5 Gb/s 2=5.0 Gb/s

LINK_CAP - RW - 32 bits - pcieCfg0:0x64			
Field Name	**Bits**	**Default**	**Description**
LINK_WIDTH (R)	9:4	0x0	This field indicates the maximum width of the given PCI Express Link. 1=x1 2=x2 4=x4 8=x8 12=x12 16=x16 32=x32
PM_SUPPORT (R)	11:10	0x3	This field indicates the level of ASPM supported on the given PCI Express Link.\
L0S_EXIT_LATENCY (R)	14:12	0x1	This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
L1_EXIT_LATENCY (R)	17:15	0x2	This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
CLOCK_POWER_MANAGEMENT (R)	18	0x0	This field indicates in the component tolerates removal of REFCLK via the CLKREQ# mechanism when the Link is in L1 and L23Ready.
SURPRISE_DOWN_ERR_REPORTING (R)	19	0x0	This field indicates if the component supports the detecting and reporting of a Surprise Down error condition.
DL_ACTIVE_REPORTING_CAPABLE (R)	20	0x0	This field indicates if the component supports the reporting of DL_Active state of the DLLSM.
LINK_BW_NOTIFICATION_CAP (R)	21	0x0	This field indicates if the component supports the Link Bandwidth Notification status and interrupt mechanisms.
PORT_NUMBER (R)	31:24	0x0	This field indicates the PCI Express port number for the given PCI Express Link.

The Link Capabilities register identifies PCI Express Link specific capabilities.

LINK_CNTL - RW - 16 bits - pcieCfg0:0x68			
Field Name	**Bits**	**Default**	**Description**
PM_CONTROL	1:0	0x0	This field controls the level of ASPM supported on the given PCI Express® Link. Defined encodings are: 00b=Disabled 01b=L0s Entry Enabled 10b=L1 Entry Enabled 11b=L0s and L1 Entry Enabled
READ_CPL_BOUNDARY (R)	3	0x0	Read Completion Boundary. Indicates the RCB value for the Root Port 0=64 Byte 1=128 Byte
LINK_DIS	4	0x0	This bit disables the Link when set to 1b. Default value of this field is 0b.
RETRAIN_LINK (W)	5	0x0	A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. Reads of this bit always return 0b.
COMMON_CLOCK_CFG	6	0x0	This bit when set indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. Default value of this field is 0b.
EXTENDED_SYNC	7	0x0	This bit when set forces the transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set
CLOCK_POWER_MANAGEMENT_EN	8	0x0	This bit determines if device is permitted to use CLKREQ# signal to power manage link clock.

LINK_CNTL - RW - 16 bits - pcieCfg0:0x68			
Field Name	**Bits**	**Default**	**Description**
HW_AUTONOMOUS_WIDTH_DISABLE	9	0x0	When set to 1, this bit disables hardware from changing the link width for reasons other than attempting to correct unreliable link operation by reducing link width.
LINK_BW_MANAGEMENT_INT_EN	10	0x0	This bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set.
LINK_AUTONOMOUS_BW_INT_EN	11	0x0	This bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set.

The Link Control register controls PCI Express Link specific parameters.

LINK_STATUS - RW - 16 bits - pcieCfg0:0x6A			
Field Name	**Bits**	**Default**	**Description**
CURRENT_LINK_SPEED (R)	3:0	0x1	Indicates the negotiated Link speed of the given PCI Express Link 1=2.5 Gb/s 2=5.0 Gb/s
NEGOTIATED_LINK_WIDTH (R)	9:4	0x0	This field indicates the negotiated width of the given PCI Express Link. Defined encodings are: 000001b X1 000010b X2 000100b X4 001000b X8 001100b X12 010000b X16 100000b X32 All other encodings are reserved. 1=x1 2=x2 4=x4 8=x8 12=x12 16=x16 32=x32
LINK_TRAINING (R)	11	0x0	This read-only bit indicates that Link training is in progress (Physical Layer LTSSM in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
SLOT_CLOCK_CFG (R)	12	0x1	This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be clear. 0=Diff Clock 1=Same Clock
DL_ACTIVE (R)	13	0x0	This bit indicates the status of the Data Link Control and Management State Machine. It returns 1b to indicate DL_Active state, 0b otherwise.
LINK_BW_MANAGEMENT_STATUS	14	0x0	This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: -A-Link retraining has completed following a write of 1b to the Retrain Link bit. -Hardware has changed the Link speed of width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process.

LINK_STATUS - RW - 16 bits - pcieCfg0:0x6A			
Field Name	**Bits**	**Default**	**Description**
LINK_AUTONOMOUS_BW_STATUS	15	0x0	This bit is set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation.

The Link Status register provides information about PCI Express Link® specific parameters.

SLOT_CAP - RW - 32 bits - pcieCfg0:0x6C			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESENT	0	0x0	This bit when set indicates that an Attention Button is implemented on the chassis for this slot.
PWR_CONTROLLER_PRESENT	1	0x0	This bit when set indicates that a Power Controller is implemented for this slot.
MRL_SENSOR_PRESENT	2	0x0	This bit when set indicates that an Manually-operated Retention Latch Sensor is implemented on the chassis for this slot.
ATTN_INDICATOR_PRESENT	3	0x0	This bit when set indicates that an Attention Indicator is implemented on the chassis for this slot.
PWR_INDICATOR_PRESENT	4	0x0	This bit when set indicates that a Power Indicator is implemented on the chassis for this slot
HOTPLUG_SURPRISE	5	0x0	This bit when set indicates that a device present in this slot might be removed from the system without any prior notification.
HOTPLUG_CAPABLE	6	0x0	This bit when set indicates that this slot is capable of supporting Hot-Plug operations.
SLOT_PWR_LIMIT_VALUE	14:7	0x0	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot
SLOT_PWR_LIMIT_SCALE	16:15	0x0	Specifies the scale used for the Slot Power Limit Value
ELECTROMECH_INTERLOCK_PRESENT	17	0x0	This bit when set indicates that an Electromechanical Interlock is implemented on the chassis for this slot.
NO_COMMAND_COMPLETED_SUPPORTED	18	0x1	This bit when set indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller.
PHYSICAL_SLOT_NUM	31:19	0x0	This hardware initialized field indicates the physical slot number attached to this Port.

The Slot Capabilities register identifies PCI Express slot specific capabilities.

SLOT_CNTL - RW - 16 bits - pcieCfg0:0x70			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESSED_EN	0	0x0	This bit when set enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event.
PWR_FAULT_DETECTED_EN	1	0x0	This bit when set enables software notification on a power fault event.
MRL_SENSOR_CHANGED_EN	2	0x0	This bit when set enables software notification on a MRL sensor changes event.
PRESENCE_DETECT_CHANGED_EN	3	0x0	This bit when set enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event.
COMMAND_COMPLETED_INTR_EN	4	0x0	This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug Controller.
HOTPLUG_INTR_EN	5	0x0	This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.

SLOT_CNTL - RW - 16 bits - pcieCfg0:0x70			
Field Name	**Bits**	**Default**	**Description**
ATTN_INDICATOR_CNTL	7:6	0x0	Reads to this register return the current state of the Attention Indicator; writes to this register set the Attention Indicator.
PWR_INDICATOR_CNTL	9:8	0x0	Reads to this register return the current state of the Power Indicator; writes to this register set the Power Indicator.
PWR_CONTROLLER_CNTL	10	0x0	When read, this register returns the current state of the Power applied to the slot; when written sets the power state of the slot per the defined encodings.
ELECTROMECH_INTERLOCK_CNTL	11	0x0	If an Electromechanical Interlock is implemented, a write of 1b causes the state of the interlock to toggle.
DL_STATE_CHANGED_EN	12	0x0	If the Data Link Layer Link Active Capability is implemented, this bit when set enables software notification when Data Link Layer Link Active Reporting bit is changed.

The Slot Control register controls PCI Express Slot specific parameters.

SLOT_STATUS - RW - 16 bits - pcieCfg0:0x72			
Field Name	**Bits**	**Default**	**Description**
ATTN_BUTTON_PRESSED	0	0x0	This bit is set when the attention button is pressed.
PWR_FAULT_DETECTED	1	0x0	This bit is set when the power controller detected a power fault at this slot.
MRL_SENSOR_CHANGED	2	0x0	This bit is set when a MRL sensor state change is detected.
PRESENCE_DETECT_CHANGED	3	0x0	This bit is set when the value reported in the Presence Detect State bit is changed.
COMMAND_COMPLETED	4	0x0	This bit is set when the Hot-Plug Controller completes an issued command.
MRL_SENSOR_STATE (R)	5	0x0	This bit reports the status of the MRL sensor.
PRESENCE_DETECT_STATE (R)	6	0x0	This bit indicates the presence of an adapter in the slot.
ELECTROMECH_INTERLOCK_STATUS (R)	7	0x0	This bit indicates the status of the Electromechanical Interlock.
DL_STATE_CHANGED	8	0x0	This bit is set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed.

The Slot Status register provides information about PCI Express Slot specific parameters.

ROOT_CNTL - RW - 16 bits - pcieCfg0:0x74			
Field Name	**Bits**	**Default**	**Description**
SERR_ON_CORR_ERR_EN	0	0x0	System Error on Correctable Error Enable -- If set this bit indicates that a System Error should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_NONFATAL_ERR_EN	1	0x0	System Error on Non-Fatal Error Enable -- If set this bit indicates that a System Error should be generated if a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
SERR_ON_FATAL_ERR_EN	2	0x0	System Error on Fatal Error Enable -- If set this bit indicates that a System Error should be generated if a Fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
PM_INTERRUPT_EN	3	0x0	PME Interrupt Enable -- This bit when set enables interrupt generation upon receipt of a PME Message.

ROOT_CNTL - RW - 16 bits - pcieCfg0:0x74			
Field Name	**Bits**	**Default**	**Description**
CRS_SOFTWARE_VISIBILITY_EN	4	0x0	This bit when set enables the Root Port to return Configuration Request Retry Status Completion Status to software.

The Root Control register controls PCI Express Root Complex specific parameters.

ROOT_CAP - RW - 16 bits - pcieCfg0:0x76			
Field Name	**Bits**	**Default**	**Description**
CRS_SOFTWARE_VISIBILITY (R)	0	0x1	Indicates the Root Port is capable of returning Configuration Request Retry Status (CRS) Completion Status to software.

The Root Capabilities register identifies PCI Express Root Complex specific capabilities.

ROOT_STATUS - RW - 32 bits - pcieCfg0:0x78			
Field Name	**Bits**	**Default**	**Description**
PME_REQUESTOR_ID (R)	15:0	0x0	This field indicates the PCI requestor ID of the last PME requestor.
PME_STATUS	16	0x0	This bit indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field.
PME_PENDING (R)	17	0x0	This read-only bit indicates that another PME is pending when the PME Status bit is set.

The Root Status register provides information about PCI Express device specific parameters.

DEVICE_CAP2 - RW - 32 bits - pcieCfg0:0x7C			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_RANGE_SUPPORTED (R)	3:0	0x0	PCIe completion timeout range supported
CPL_TIMEOUT_DIS_SUPPORTED (R)	4	0x0	PCIe completion timeout disabled supported
ARI_FORWARDING_SUPPORTED (R)	5	0x0	ARI Forwarding supported

The Device Capabilities 2 register identifies PCI Express device specific capabilities.

DEVICE_CNTL2 - RW - 16 bits - pcieCfg0:0x80			
Field Name	**Bits**	**Default**	**Description**
CPL_TIMEOUT_VALUE	3:0	0x0	PCIE completion timeout value
CPL_TIMEOUT_DIS	4	0x0	Disable PCIE completion timeout
ARI_FORWARDING_EN	5	0x0	ARI Forwarding enable

The Device Control 2 register controls PCI Express device specific parameters.

DEVICE_STATUS2 - RW - 16 bits – pcieCfg0:0x82			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	Reserved

The Device Status 2 register provides information about PCI Express device specific parameters.

LINK_CAP2 - RW - 32 bits - pcieCfg0:0x84			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	Reserved

The Link Capabilities 2 register identifies PCI Express Link specific capabilities.

LINK_CNTL2 - RW - 16 bits - pcieCfg0:0x88			
Field Name	**Bits**	**Default**	**Description**
TARGET_LINK_SPEED	3:0	0x1	The upper limit on the operational speed. This field restricts the data rate values advertised by an upstream component.
ENTER_COMPLIANCE	4	0x0	This bit forces a port's transmitter to enter Compliance.
HW_AUTONOMOUS_SPEED_DISABLE	5	0x0	Controls the component's ability to autonomously direct changes in link speed.
SELECTABLE_DEEMPHASIS (R)	6	0x0	Selectable de-emphasis (in GEN 2 data rate) 0= -6dB 1= -3.6dB
XMIT_MARGIN	9:7	0x0	These bits control the value of the non-deemphasized voltage level at the transmitter pins.
ENTER_MOD_COMPLIANCE	10	0x0	LTSSM transmits modified compliance pattern in Polling.Compliance if this bit is set to 1.
COMPLIANCE_SOS	11	0x0	When set to 1, the LTSSM is required to send SOS periodically in between the (modified) compliance patterns.
COMPLIANCE_DEEMPHASIS	12	0x0	This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the `enter compliance' bit being 1b. When the link is operating at 2.5 GT/s, the setting of this bit has no effect. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. 0=-6 dB 1=-3dB

The Link Control 2 register controls PCI Express Link specific parameters.

LINK_STATUS2 - RW - 16 bits - pcieCfg0:0x8A			
Field Name	**Bits**	**Default**	**Description**
CUR_DEEMPHASIS_LEVEL (R)	0	0x0	When the link is operating at 5GT/s speed, this bit reflects the level of de-emphasis.

The Link Status 2 register provides information about PCI Express Link specific parameters.

SLOT_CAP2 - RW - 32 bits - pcieCfg0:0x8C			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	31:0	0x0	Reserved

The Slot Capabilities 2 register identifies PCI Express slot specific capabilities.

SLOT_CNTL2 - RW - 16 bits - pcieCfg0:0x90			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	Reserved

The Slot Control 2 register controls PCI Express Slot specific parameters.

SLOT_STATUS2 - RW - 16 bits - pcieCfg0:0x92			
Field Name	**Bits**	**Default**	**Description**
RESERVED (R)	15:0	0x0	Reserved

The Slot Status 2 register provides information about PCI Express Slot specific parameters.

MSI_CAP_LIST - R - 16 bits - pcieCfg0:0xA0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x5	Register identifies if a device function is MSI capable
NEXT_PTR	15:8	0xb0	Pointer to the next item on the capabilities list

Message Signaled Interrupt Capability Registers

MSI_MSG_CNTL - RW - 16 bits - pcieCfg0:0xA2			
Field Name	**Bits**	**Default**	**Description**
MSI_EN	0	0x0	Enable MSI messaging 0=Disable 1=Enable
MSI_MULTI_CAP (R)	3:1	0x0	Multiple Message Capable register is read to determine the number of requested messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_MULTI_EN	6:4	0x0	Multiple Message Enable register is written to indicate the number of allocated messages. 0=1 message allocated 1=2 messages allocated 2=4 messages allocated 3=8 messages allocated 4=16 messages allocated 5=32 messages allocated 6=Reserved 7=Reserved
MSI_64BIT (R)	7	0x0	Signifies if a device function is capable of generating a 64-bit message address 0=Not capable of generating 1 64-bit message address 1=Capable of generating 1 64-bit message address

Message Signaled Interrupts Control Register

MSI_MSG_ADDR_LO - RW - 32 bits - pcieCfg0:0xA4			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_LO	31:2	0x0	Message Lower Address - use lower 32-bits of address

Message Lower Address

MSI_MSG_ADDR_HI - RW - 32 bits - pcieCfg0:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_MSG_ADDR_HI	31:0	0x0	Message Upper Address - use upper 32-bit of address

Message Upper Address

MSI_MSG_DATA_64 - RW - 16 bits - pcieCfg0:0xAC			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA_64	15:0	0x0	Message Data. System specified.

64-bit MSI Message Data

MSI_MSG_DATA - RW - 32 bits - pcieCfg0:0xA8			
Field Name	**Bits**	**Default**	**Description**
MSI_DATA	15:0	0x0	Message Data. System specified.

MSI Message Data

SSID_CAP_LIST - R - 32 bits - pcieCfg0:0xB0			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0xd	Capability ID
NEXT_PTR	15:8	0xb8	Pointer to next capability register

Subsystem ID Capability List

SSID_ID - R - 32 bits - pcieCfg0:0xB4			
Field Name	**Bits**	**Default**	**Description**
SUBSYSTEM_VENDOR_ID	15:0	0x1002	Subsystem Vendor ID
SUBSYSTEM_ID	31:16	0x0	Subsystem ID

Subsystem ID

MSI_MAP_CAP_LIST - R - 32 bits - pcieCfg0:0xB8			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	7:0	0x8	Identifies this as a HyperTransport™ capability list item.
NEXT_PTR	15:8	0x0	Pointer to the next item in the capabilities list. Must be NULL for the final item in the list. This field is read only.
EN	16	0x1	Indicates if the mapping is active.
FIXD	17	0x1	Indicates if the programming address is fixed.
CAP_TYPE	31:27	0x15	Indicates this as the MSI Mapping Capability block.

MSI Mapping Capability Register

PCIE_VENDOR_SPECIFIC_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x100			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xb	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x110	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Vendor Specific Capability

PCIE_VENDOR_SPECIFIC_HDR - R - 32 bits - pcieCfg0:0x104			
Field Name	**Bits**	**Default**	**Description**
VSEC_ID	15:0	0x1	Vendor-defined ID number.
VSEC_REV	19:16	0x1	Vendor-defined revision number.
VSEC_LENGTH	31:20	0x10	Number of bytes in the entire VSEC structure.

Vendor Specific Header

PCIE_VENDOR_SPECIFIC1 - RW - 32 bits - pcieCfg0:0x108			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCIE scratch register.

Vendor-Specific Scratch Register 1

PCIE_VENDOR_SPECIFIC2 - RW - 32 bits - pcieCfg0:0x10C			
Field Name	**Bits**	**Default**	**Description**
SCRATCH	31:0	0x0	PCIE scratch register.

Vendor-Specific Scratch Register 2

PCIE_VC_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x110			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x2	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x140	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Virtual Channel Enhanced Capability Header

PCIE_PORT_VC_CAP_REG1 - R - 32 bits - pcieCfg0:0x114			
Field Name	**Bits**	**Default**	**Description**
EXT_VC_COUNT	2:0	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. This field is valid for all devices.
LOW_PRIORITY_EXT_VC_COUNT	6:4	0x0	Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC group.
REF_CLK	9:8	0x0	Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration.
PORT_ARB_TABLE_ENTRY_SIZE	11:10	0x0	Indicates the size (in bits) of Port Arbitration table entry in the device.

Port VC Capability Register 1

PCIE_PORT_VC_CAP_REG2 - R - 32 bits - pcieCfg0:0x118			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_CAP	7:0	0x0	Indicates the types of VC Arbitration supported by the device for the Low Priority Virtual Channel group.
VC_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the VC Arbitration Table.

Port VC Capability Register 2

PCIE_PORT_VC_CNTL - RW - 16 bits - pcieCfg0:0x11C			
Field Name	**Bits**	**Default**	**Description**
LOAD_VC_ARB_TABLE (R)	0	0x0	Used for software to update the VC Arbitration Table.
VC_ARB_SELECT	3:1	0x0	Used for software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes.

Port VC Control Register

PCIE_PORT_VC_STATUS - R - 16 bits - pcieCfg0:0x11E			
Field Name	**Bits**	**Default**	**Description**
VC_ARB_TABLE_STATUS	0	0x0	Indicates the coherency status of the VC Arbitration Table

Port VC Status Register

PCIE_VC0_RESOURCE_CAP - R - 32 bits - pcieCfg0:0x120			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC.
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting.
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.

VC0 Resource Capability Register

PCIE_VC0_RESOURCE_CNTL - RW - 32 bits - pcieCfg0:0x124			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x1	This field indicates the TCs that are mapped to the VC resource.
TC_VC_MAP_TC1_7	7:1	0x7f	This field indicates the TCs that are mapped to the VC resource.
LOAD_PORT_ARB_TABLE (R)	16	0x0	This bit, when set, updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	This field configures the VC resource to provide a particular Port Arbitration service.
VC_ID (R)	26:24	0x0	This field assigns a VC ID to the VC resource.
VC_ENABLE (R)	31	0x1	This field, when set, enables a Virtual Channel.

VC0 Resource Control Register

PCIE_VC0_RESOURCE_STATUS - R - 16 bits - pcieCfg0:0x12A			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	This bit indicates the coherency status of the Port Arbitration Table associated with the VC resource.
VC_NEGOTIATION_PENDING	1	0x1	This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state.

VC0 Resource Status Register

PCIE_VC1_RESOURCE_CAP - R - 32 bits - pcieCfg0:0x12C			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_CAP	7:0	0x1	Indicates types of Port Arbitration supported by the VC resource.
REJECT_SNOOP_TRANS	15	0x0	When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC.
MAX_TIME_SLOTS	21:16	0x0	Indicates the maximum number of time slots that the VC resource is capable of supporting.
PORT_ARB_TABLE_OFFSET	31:24	0x0	Indicates the location of the Port Arbitration Table associated with the VC resource.

VC1 Resource Capability Register

PCIE_VC1_RESOURCE_CNTL - RW - 32 bits - pcieCfg0:0x130			
Field Name	**Bits**	**Default**	**Description**
TC_VC_MAP_TC0 (R)	0	0x0	This field indicates the TCs that are mapped to the VC resource.
TC_VC_MAP_TC1_7	7:1	0x0	This field indicates the TCs that are mapped to the VC resource.
LOAD_PORT_ARB_TABLE (R)	16	0x0	This bit, when set, updates the Port Arbitration logic from the Port Arbitration Table for the VC resource.
PORT_ARB_SELECT	19:17	0x0	This field configures the VC resource to provide a particular Port Arbitration service.
VC_ID	26:24	0x0	This field assigns a VC ID to the VC resource.
VC_ENABLE	31	0x0	This field, when set, enables a Virtual Channel.

VC1 Resource Control Register

PCIE_VC1_RESOURCE_STATUS - R - 16 bits - pcieCfg0:0x136			
Field Name	**Bits**	**Default**	**Description**
PORT_ARB_TABLE_STATUS	0	0x0	This bit indicates the coherency status of the Port Arbitration Table associated with the VC resource.
VC_NEGOTIATION_PENDING	1	0x1	This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state.

VC1 Resource Status Register

PCIE_DEV_SERIAL_NUM_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x140			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x3	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x150	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Device Serial Number Enhanced Capability header

PCIE_DEV_SERIAL_NUM_DW1 - R - 32 bits - pcieCfg0:0x144			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_LO	31:0	0x0	Lower 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)

PCI-Express Device Serial Number (1st DW)

PCIE_DEV_SERIAL_NUM_DW2 - R - 32 bits - pcieCfg0:0x148			
Field Name	**Bits**	**Default**	**Description**
SERIAL_NUMBER_HI	31:0	0x0	Upper 32-bits of IEEE defined 64-bit extended unique identifier. (EUI-64)

PCI-Express Device Serial Number (2nd DW)

PCIE_ADV_ERR_RPT_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x150			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0x1	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.
NEXT_PTR	31:20	0x190	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

Advanced Error Reporting Enhanced Capability header

PCIE_UNCORR_ERR_STATUS - RW - 32 bits - pcieCfg0:0x154			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_STATUS	4	0x0	Data Link Protocol Error Status
SURPDN_ERR_STATUS (R)	5	0x0	Surprise Down Error Status
PSN_ERR_STATUS	12	0x0	Poisoned TLP Status
FC_ERR_STATUS (R)	13	0x0	Flow Control Protocol Error Status
CPL_TIMEOUT_STATUS	14	0x0	Completion Timeout Status
CPL_ABORT_ERR_STATUS	15	0x0	Completer Abort Status
UNEXP_CPL_STATUS	16	0x0	Unexpected Completion Status
RCV_OVFL_STATUS (R)	17	0x0	Receiver Overflow Status
MAL_TLP_STATUS	18	0x0	Malformed TLP Status
ECRC_ERR_STATUS	19	0x0	ECRC Error Status
UNSUPP_REQ_ERR_STATUS	20	0x0	Unsupported Request Error Status
ACS_VIOLATION_STATUS	21	0x0	ACS Violation Error Status

The Uncorrectable Error Status register reports error status of individual error sources on a PCI Express device.

PCIE_UNCORR_ERR_MASK - RW - 32 bits - pcieCfg0:0x158			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_MASK	4	0x0	Data Link Protocol Error Mask
SURPDN_ERR_MASK (R)	5	0x0	Surprise Down Error Mask
PSN_ERR_MASK	12	0x0	Poisoned TLP Mask
FC_ERR_MASK (R)	13	0x0	Flow Control Protocol Error Mask
CPL_TIMEOUT_MASK	14	0x0	Completion Timeout Mask
CPL_ABORT_ERR_MASK	15	0x0	Completer Abort Mask
UNEXP_CPL_MASK	16	0x0	Unexpected Completion Mask
RCV_OVFL_MASK (R)	17	0x0	Receiver Overflow Mask
MAL_TLP_MASK	18	0x0	Malformed TLP Mask
ECRC_ERR_MASK	19	0x0	ECRC Error Mask
UNSUPP_REQ_ERR_MASK	20	0x0	Unsupported Request Error Mask

PCIE_UNCORR_ERR_MASK - RW - 32 bits - pcieCfg0:0x158			
Field Name	**Bits**	**Default**	**Description**
ACS_VIOLATION_MASK	21	0x0	ACS Violation Mask

The Uncorrectable Error Mask register controls reporting of individual errors by the device to the PCI Express Root Complex via a PCI Express error Message.

PCIE_UNCORR_ERR_SEVERITY - RW - 32 bits - pcieCfg0:0x15C			
Field Name	**Bits**	**Default**	**Description**
DLP_ERR_SEVERITY	4	0x1	Data Link Protocol Error Severity
SURPDN_ERR_SEVERITY (R)	5	0x1	Surprise Down Error Severity
PSN_ERR_SEVERITY	12	0x0	Poisoned TLP Severity
FC_ERR_SEVERITY (R)	13	0x1	Flow Control Protocol Error Severity
CPL_TIMEOUT_SEVERITY	14	0x0	Completion Timeout Error Severity
CPL_ABORT_ERR_SEVERITY	15	0x0	Completer Abort Error Severity
UNEXP_CPL_SEVERITY	16	0x0	Unexpected Completion Error Severity
RCV_OVFL_SEVERITY (R)	17	0x1	Receiver Overflow Error Severity
MAL_TLP_SEVERITY	18	0x1	Malformed TLP Severity
ECRC_ERR_SEVERITY	19	0x0	ECRC Error Severity
UNSUPP_REQ_ERR_SEVERITY	20	0x0	Unsupported Request Error Severity
ACS_VIOLATION_SEVERITY	21	0x0	ACS Violation Severity

The Uncorrectable Error Severity register controls whether an individual error is reported as a Nonfatal or Fatal error.

PCIE_CORR_ERR_STATUS - RW - 32 bits - pcieCfg0:0x160			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_STATUS (R)	0	0x0	Receiver Error Status
BAD_TLP_STATUS	6	0x0	Bad TLP Status
BAD_DLLP_STATUS	7	0x0	Bad DLLP Status
REPLAY_NUM_ROLLOVER_STATUS	8	0x0	REPLAY_NUM Rollover Status
REPLAY_TIMER_TIMEOUT_STATUS	12	0x0	Replay Timer Timeout Status
ADVISORY_NONFATAL_ERR_STATUS	13	0x0	Advisory Non-Fatal Status

The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device.

PCIE_CORR_ERR_MASK - RW - 32 bits - pcieCfg0:0x164			
Field Name	**Bits**	**Default**	**Description**
RCV_ERR_MASK (R)	0	0x0	Receiver Error Mask
BAD_TLP_MASK	6	0x0	Bad TLP Mask
BAD_DLLP_MASK	7	0x0	Bad DLLP Mask
REPLAY_NUM_ROLLOVER_MASK	8	0x0	REPLAY_NUM Rollover Mask
REPLAY_TIMER_TIMEOUT_MASK	12	0x0	Replay Timer Timeout Mask

PCIE_CORR_ERR_MASK - RW - 32 bits - pcieCfg0:0x164			
Field Name	**Bits**	**Default**	**Description**
ADVISORY_NONFATAL_ERR_MASK	13	0x1	Advisory Non-Fatal Mask

The Correctable Error Mask register controls reporting of individual correctable errors by device to the PCI Express Root Complex via a PCI Express error Message.

PCIE_ADV_ERR_CAP_CNTL - RW - 32 bits - pcieCfg0:0x168			
Field Name	**Bits**	**Default**	**Description**
FIRST_ERR_PTR (R)	4:0	0x0	The First Error Pointer is a read-only register that identifies the bit position of the first error reported in the Uncorrectable Error Status register.
ECRC_GEN_CAP (R)	5	0x0	This bit indicates that the device is capable of generating ECRC.
ECRC_GEN_EN	6	0x0	This bit when set enables ECRC generation. Default value of this field is 0.
ECRC_CHECK_CAP (R)	7	0x0	This bit indicates that the device is capable of checking ECRC.
ECRC_CHECK_EN	8	0x0	This bit when set enables ECRC checking. Default value of this field is 0.

Advanced Error Capabilities and Control Register

PCIE_HDR_LOG0 - R - 32 bits - pcieCfg0:0x16C			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 1st DW

Header Log Register captures the Header for the TLP corresponding to a detected error;

PCIE_HDR_LOG1 - R - 32 bits - pcieCfg0:0x170			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 2nd DW

Header Log Register

PCIE_HDR_LOG2 - R - 32 bits – pcieCfg0:0x174			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 3rd DW

Header Log Register

PCIE_HDR_LOG3 - R - 32 bits – pcieCfg0:0x178			
Field Name	**Bits**	**Default**	**Description**
TLP_HDR	31:0	0x0	TLP Header 4th DW

Header Log Register

PCIE_ROOT_ERR_CMD - RW - 32 bits - pcieCfg0:0x17C			
Field Name	**Bits**	**Default**	**Description**
CORR_ERR_REP_EN	0	0x0	Correctable Error Reporting Enable -- When set this bit enables the generation of an interrupt when a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.

PCIE_ROOT_ERR_CMD - RW - 32 bits - pcieCfg0:0x17C			
Field Name	**Bits**	**Default**	**Description**
NONFATAL_ERR_REP_EN	1	0x0	Non-Fatal Error Reporting Enable -- When set this bit enables the generation of an interrupt when a Non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
FATAL_ERR_REP_EN	2	0x0	Fatal Error Reporting Enable -- When set this bit enables the generation of an interrupt when a Fatal error is reported by any of the devices in the hierarchy associated with this Root Port.

Root Error Command Register

PCIE_ROOT_ERR_STATUS - RW - 32 bits - pcieCfg0:0x180			
Field Name	**Bits**	**Default**	**Description**
ERR_CORR_RCVD	0	0x0	Set when a correctable error Message is received and this bit is not already set. Default value of this field is 0.
MULT_ERR_CORR_RCVD	1	0x0	Set when a correctable error Message is received and ERR_COR Received is already set. Default value of this field is 0.
ERR_FATAL_NONFATAL_RCVD	2	0x0	Set when either a Fatal or a Non-fatal error Message is received and this bit is not already set. Default value of this field is 0.
MULT_ERR_FATAL_NONFATAL_RCVD	3	0x0	Set when either a Fatal or a Non-fatal error is received and ERR_FATAL/NONFATAL Received is already set. Default value of this field is 0.
FIRST_UNCORRECTABLE_FATAL	4	0x0	Set to 1b when the first Uncorrectable error Message received is for a Fatal error. Default value of this field is 0.
NONFATAL_ERROR_MSG_RCVD	5	0x0	Set to 1b when one or more Non-Fatal Uncorrectable error Messages have been received. Default value of this field is 0.
FATAL_ERROR_MSG_RCVD	6	0x0	Set to 1b when one or more Fatal Uncorrectable error Messages have been received. Default value of this field is 0.
ADV_ERR_INT_MSG_NUM (R)	31:27	0x0	Advanced Error Interrupt Message Number

Root Error Status Register

PCIE_ERR_SRC_ID - RW - 32 bits - pcieCfg0:0x184			
Field Name	**Bits**	**Default**	**Description**
ERR_COR_SRC_ID (R)	15:0	0x0	Loaded with the Requestor ID indicated in the received ERR_COR Message when the ERR_COR Received register is not already set. Default value of this field is 0.
ERR_FATAL_NONFATAL_SRC_ID (R)	31:16	0x0	Loaded with the Requestor ID indicated in the received ERR_FATAL or ERR_NONFATAL Message when the ERR_FATAL/NONFATAL Received register is not already set. Default value of this field is 0.

The Error Source Identification register identifies the source (Requestor ID) of first correctable and uncorrectable (Non-fatal/Fatal) errors reported in the Root Error Status register.

PCIE_ACS_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x190			
Field Name	**Bits**	**Default**	**Description**
CAP_ID	15:0	0xd	This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability.
CAP_VER	19:16	0x1	This field is a PCI-SIG defined version number that indicates the version of the capability structure present.

PCIE_ACS_ENH_CAP_LIST - R - 32 bits - pcieCfg0:0x190			
Field Name	**Bits**	**Default**	**Description**
NEXT_PTR	31:20	0x0	This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.

ACS Enhanced Capability header

PCIE_ACS_CAP - R - 16 bits - pcieCfg0:0x194			
Field Name	**Bits**	**Default**	**Description**
SOURCE_VALIDATION	0	0x0	When set, it indicates that the component implements ACS Source Validation.
TRANSLATION_BLOCKING	1	0x0	When set, it indicates that the component implements ACS Translation Blocking.
P2P_REQUEST_REDIRECT	2	0x0	When set, it indicates that the component implements ACS P2P Request Redirect.
P2P_COMPLETION_REDIRECT	3	0x0	When set, it indicates that the component implements ACS P2P Completion Redirect.
UPSTREAM_FORWARDING	4	0x0	When set, it indicates that the component implements ACS Upstream Forwarding.
P2P_EGRESS_CONTROL	5	0x0	When set, it indicates that the component implements ACS P2P Egress Control.
DIRECT_TRANSLATED_P2P	6	0x0	When set, it indicates that the component implements ACS Direct Translated P2P.
EGRESS_CONTROL_VECTOR_SIZE	15:8	0x0	Encodings 01h-FFh directly indicate the number of applicable bits in the Egress Control Vector; the encoding 00h indicates 256 bits.

ACS Capability register

PCIE_ACS_CNTL - RW - 16 bits - pcieCfg0:0x196			
Field Name	**Bits**	**Default**	**Description**
SOURCE_VALIDATION_EN	0	0x0	When set, the component validates the Bus Number from the Requester ID of Upstream Requests against the secondary / subordinate Bus Numbers.
TRANSLATION_BLOCKING_EN	1	0x0	When set, the component blocks all Upstream Memory Requests whose Address Translation field is not set to the default value.
P2P_REQUEST_REDIRECT_EN	2	0x0	In conjunction with ACS P2P Egress Control and ACS Direct Translated P2P mechanisms, determines when the component redirects P2P Requests Upstream.
P2P_COMPLETION_REDIRECT_EN	3	0x0	Determines when the component redirects P2P Completions Upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
UPSTREAM_FORWARDING_EN	4	0x0	When set, the component forwards Upstream any Request or Completion TLPs it receives that were redirected Upstream by a component lower in the hierarchy.
P2P_EGRESS_CONTROL_EN (R)	5	0x0	In conjunction with the Egress Control Vector plus the ACS P2P Request Redirect and ACS Direct Translated P2P mechanisms, determines when to allow, disallow, or redirect P2P Requests.
DIRECT_TRANSLATED_P2P_EN	6	0x0	When set, overrides the ACS P2P Request Redirect and ACS P2P Egress Control mechanisms with P2P Memory Requests whose Address Translation field indicates a Translated address.

ACS Control register

Chapter 5 Integrated Micro-Controller Registers

The IMC message registers are designed as a logical device in the FCH that complies with the Plug and Play ISA Specification. The device number of the message device is 9 and it is set up through the following global and local configuration registers.

5.1 Global Configuration Registers

Address	Type	Port Name
0x02	WO	Configuration Control Set bit 0 to cause Soft Reset. No need to clear. Deactivates the devices and resets the global and device registers to their default values.
0x07	R/W	Logical Device Number This register is for selecting the current logical device.
0x20	RO	Device ID
0x21	RO	Revison ID

5.2 Local Configuration Registers

Address	Register Name	Type	Register Description
0x30	Activate	R/W	Set bit 0 to activate this logical device
0x60	MSG9 Base Addr High Byte	R/W	MESSAGE9_BASE (high byte)
0x61	MSG9 Base Addr Low Byte	R/W	MESSAGE9_BASE (low byte) Bit 0 is read-only 0.
0x70	MSG Interrupt Type Byte	R/W	Type of interrupt sent to host when IMC firmware writes the MSG_IMC_TO_SYS register: 00b: SMI (default) 01b: No Interrupt 10b: IRQ – the specific IRQ is programmed in ACPI register space. 11b: No interrupt

5.3 Message Registers

Since the activation of Logical Device Number 9 and the address assignment of the message registers are handled by CIMx during the IMC enabling process, the host software needs only to read the value of MESSAGE9_BASE register (local configuration register 0x60 & 0x61) in order to access the IMC message registers.

There are 16 message registers available in the message register device, each with a unique index value

for access through the Message Base register using the index and data register addressing mechanism.

Index	Register Name	System Type	Register Description
0x80	MSG_SYS_TO_IMC	R/W	System to IMC Message data
0x81	MSG_IMC_TO_SYS	RO	IMC to System Message data
0x82	MSG_REG0	R/W	IMC Message storage 82
0x83	MSG_REG1	R/W	IMC Message storage 83
0x84	MSG_REG2	R/W	IMC Message storage 84
0x85	MSG_REG3	R/W	IMC Message storage 85
0x86	MSG_REG4	R/W	IMC Message storage 86
0x87	MSG_REG5	R/W	IMC Message storage 87
0x88	MSG_REG6	R/W	IMC Message storage 88
0x89	MSG_REG7	R/W	IMC Message storage 89
0x8A	MSG_REG8	R/W	IMC Message storage 8A
0x8B	MSG_REG9	R/W	IMC Message storage 8B
0x8C	MSG_REGA	R/W	IMC Message storage 8C
0x8D	MSG_REGB	R/W	IMC Message storage 8D
0x8E	MSG_REGC	R/W	IMC Message storage 8E
0x8F	MSG_REGD	R/W	IMC Message storage 8F